HEWLETT PACKARD

Service Manual

HP 5361B
Pulse/CW Microwave Counter

Certification and Warranty

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology (formerly National Bureau of Standards), to the extent allowed by that organization's calibration facility, and to the calibration facilities of other International Standards Organization members.

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For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

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For any assistance, contact your nearest Hewlett-Packard Sales and Support Office. Addresses are provided at the back of this manual.

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SERVICE MANUAL

HP 5361B

Pulse/CW Microwave Counter

(Also applies to the HP 5361A 20 GHz Pulse/CW Microwave Counter)

SERIAL NUMBER PREFIX: 3023

This manual applies to instruments with serial numbers prefixed 3023, unless accompanied by a Manual Change Sheet indicating otherwise. For additional information about serial numbers, refer to the subsection INSTRUMENTS COVERED BY THIS MANUAL in the section titled "HOW TO USE THIS MANUAL". (These sections are in the HP 5361B Operating and Programming Manual.)

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HEWLETT® PACKARD

MANUAL PART NUMBER 05361-90028

Safety Considerations

GENERAL

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

This product is a Safety Class I instrument (provided with a protective earth terminal).

BEFORE APPLYING POWER

Verify that the product is set to match the available line voltage and the correct fuse is installed. Refer to instructions in this appendix.

SAFETY EARTH GROUND

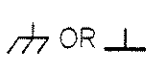
An uninterruptible safety earth ground must be provided from the mains power source to the product input wiring terminals or supplied power cable.

Safety Symbols

Instruction manual symbol; the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual.

Indicates hazardous voltages.

Indicates earth (ground) terminal.



Indicates terminal is connected to chassis when such connection is not apparent.

Alternating current.

Direct current.

WARNING

THIS DENOTES A HAZARD. IT CALLS ATTENTION TO A PROCEDURE, PRACTICE, OR THE LIKE, WHICH, IF NOT CORRECTLY PERFORMED OR ADHERED TO, COULD RESULT IN PERSONAL INJURY. DO NOT PROCEED BEYOND A *WARNING* SIGN UNTIL THE INDICATED CONDITIONS ARE FULLY UNDERSTOOD AND MET.

CAUTION

This denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a *CAUTION* sign until the indicated conditions are fully understood and met.

Safety Information

WARNING

Any interruption of the protective grounding conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury. (Grounding one conductor of a two conductor outlet is not sufficient protection.)

Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

If this instrument is to be energized via an autotransformer (for voltage reduction) make sure the common terminal is connected to the earthed pole terminal (neutral) of the power source.

Instructions for adjustments while covers are removed and for servicing are for use by service-trained personnel only. To avoid dangerous electric shock, do not perform such adjustments or servicing unless qualified to do so.

For continued protection against fire, replace the line fuse(s) only with 250V fuse(s) of the same current rating and type (for example, normal blow, time delay). Do not use repaired fuses or short circuited fuseholders.

When measuring power line signals, be extremely careful and always use a step-down isolation transformer whose output voltage is compatible with the input measurement capabilities of this product. This product's front and rear panels are typically at earth ground, so NEVER TRY TO MEASURE AC POWER LINE SIGNALS WITHOUT AN ISOLATION TRANSFORMER.

Safety Information (Continued)

ACOUSTIC NOISE EMISSION:	LpA 47dB at operator position, at normal operation, tested per ISO 7779. All data are the results from type test.
GERAeUSCHEMISSION:	LpA 47 dB am Arbeits platz, normaler Betrieb, geprueft nach DIN 45635 Teil 19. Die Anbagen beruhen auf Ergebnissen von Typpruefungen.

1

PERFORMANCE TESTS

1-1. SECTION GUIDE

This section provides you with procedures for testing the electrical performance of the HP 5361B Pulse/CW Microwave Counter, by using the specifications listed in Appendix A as performance standards. Three kinds of testing are described: operation verification, HP-IB verification, and complete performance testing.

1-2. Where to Find Important Topics

1-3. Section Summary

1-4. OPERATION VERIFICATION

If you suspect the HP 5361B is not working correctly, you may perform the operation verification procedure. This procedure is an abbreviated set of tests that give a high degree of confidence the instrument is operating properly without performing the complete Performance Test. An Operation Verification would be useful for incoming inspection, routine maintenance, and after instrument repair.

1-5. HP-IB VERIFICATION

The HP-IB verification program, allows you to exercise the instrument through most of its command set via the HP-IB interface. The program is written for a Series 300 HP 9000 as the controller. If the instrument successfully completes all phases of the verification program, there is a very high probability the HP-IB interface and the counter are working properly. The HP-IB program is available on a disk, HP Part No. 05361-13501 (3 1/2" media) and 05361-13052 (5 1/4" media).

1-6. COMPLETE PERFORMANCE TESTING

The complete Performance Test procedures begin immediately following the HP-IB verification subsection. All tests can be performed without access to the inside of the instrument.

1-7. EQUIPMENT REQUIRED

The equipment required for all test procedures in this section is listed in Appendix B (Recommended Test Equipment). Any equipment that satisfies the required characteristics given in the table may be substituted for the recommended models.

1-8. CALIBRATION CYCLE

The HP 5361B requires periodic verification of correct operation. You should use the operation verification procedure at least once every year, depending on environment and use. A full calibration procedure, including adjustments and a full performance test, should be performed at least once every 6 months for instruments equipped with the standard TCXO timebase, at least once a year for instruments equipped with the Option 001 Oven Oscillator Timebase, and once every 5 years for instruments equipped with the Option 010 High Stability Timebase. When you use these calibration cycles, kHz accuracy of the HP 5361B is ensured.

1-9. Test Specifications with Option 006

All test and verification procedures described in this section are intended for testing of the standard HP 5361B. If Option 006 (Limiter) is installed the sensitivity specifications of the counter will be different from the standard instrument. If your HP 5361B is so equipped, use the same procedures as for the standard instrument, but observe the option specifications listed in Appendix A, *Table A-1,* as performance standards.

NOTE

The following operation verification and performance test procedures require measurement of the actual input sensitivity of the 5361B. The actual sensitivity MUST be measured as follows:

1. Before measuring, be sure to calibrate the power meter according to the frequency calibration data provided on the power sensor to be used in the test.

2. To measure actual sensitivity, decrease the input level to the counter until it stops counting, then slowly increase the input level until the counter measures the input properly (as defined by the particular procedure being performed).

1-10. OPERATION VERIFICATION PROCEDURE

1-11. Power-Up Self Check

1. Before connecting the power cord and switching on the instrument, be sure that the line voltage selector is properly set, the correct fuse is installed, and all safety precautions have been observed.

2. Set the POWER switch to the ON position and verify the Power-up Self Check routine, as follows:

   a. Immediately after switching the power on, the counter performs a starburst display test in which all segments of the liquid crystal display are turned on.

The display should remain in this state for about three seconds. Check that no segments are missing.

b. If any of the internal tests fail, the results of the first test failing will be displayed after the display test and EFUN 54 display. Pressing the RESET/LOCAL key will display the next test, if any, failing. When all failing tests have been displayed, the HP-IB address will be displayed for about two seconds. If all tests pass, the HP-IB address will be displayed immediately after the display test.

c. After the HP-IB address is displayed, the counter should go into the measurement mode last selected (if the counter had previously been left in Standby), or into the Auto mode with defaults set as described in Section 2 (if AC power had previously been disconnected from the counter).

d. If a FAIL message is displayed during the Power-Up Self-Test, refer to troubleshooting procedures in Section 5, Service, for information about specific diagnostic failures.

3. Enter results of the Power-Up Self-Test on the Operation Verification Record (*Table C-3*).

1-12. INPUT 2, CW Counting Check

1. Set the counter to the Input 2, 50 Ω impedance mode by pressing the 50 Ω key.

2. Connect the rear panel 10MHZ OUT BNC to the front panel INPUT 2. Verify that the instrument displays: 10 000 000 (±1 Hz).

3. Enter results on the Operation Verification Record.

1-13. INPUT 2, 10 Hz - 525 MHz CW Input Sensitivity Test

The following test is in two parts, Setup 1 for 50 MHz to 525 MHz, and Setup 2 for 10 Hz to 20 MHz.

Specification: 50 Ω: 10 MHz - 525 MHz, 25 mV rms
1 M Ω: 10 Hz - 80 MHz, 25 mV rms

Description: The counter is set to the 10 MHz - 525 MHz range, 50 Ω impedance, and a 25 mV rms (–19.3 dBm) signal is applied to Input 2 as shown in *Figure 1-1*. The test generator is set to selected frequencies and the 5361B is checked for proper

counting. The counter is next set for 1MΩ impedance, a 25 mV rms (–19.3 dBm) 80 MHz signal is applied to INPUT 2 through a 50 Ω feedthrough, and the counter is checked for proper counting. The test setup is changed to Setup 2 to test the 10 Hz - 20 MHz range as shown in *Figure 1- 2.*

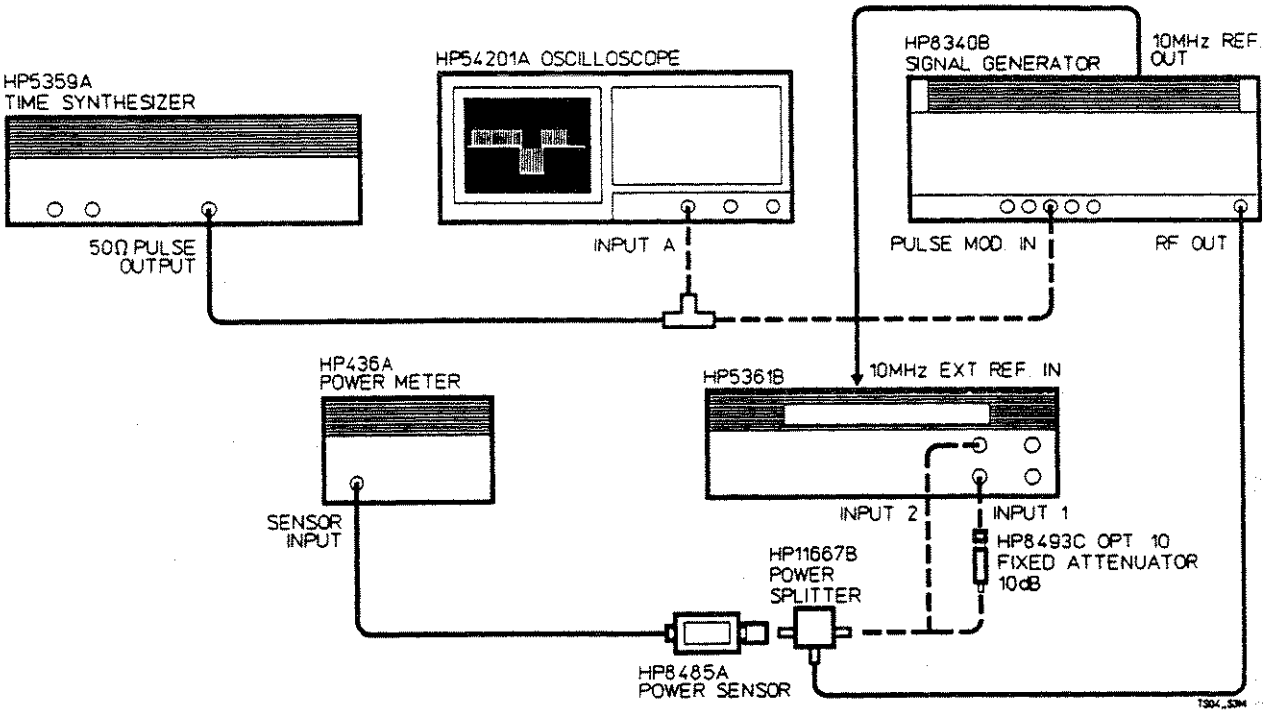


Figure 1-1. Setup 1: CW/Pulse, 10 MHz - 26.5 MHz

1. Set the counter to the 10 MHz - 525 MHz range, 50 Ω impedance, by pressing the 50 Ω key.

2. Set the 8340B to 50 MHz and an output level of 25 mV rms (–19.3 dBm) as measured on the 436A Power Meter. Measure actual sensitivity and verify that the 5361B counts properly at 50 MHz, 100 MHz, 250 MHz, and 525 MHz. Enter the results in the Operation Verification Record (*Table 1-2*).

3. Insert a 50 Ω feedthrough between the 11667B power splitter and INPUT 2 of the counter. Press the 1M Ω key on the counter to select the 1M Ω impedance, 10 Hz - 80 MHz input.

4. Set the 8340B to 80 MHz and a level of 25 mV rms (–19.3 dBm) as measured on the 436A Power Meter.

5. Verify that the 5361B counts properly at 80 MHz at 25 mV rms, and enter the result in the Operation Verification Record.

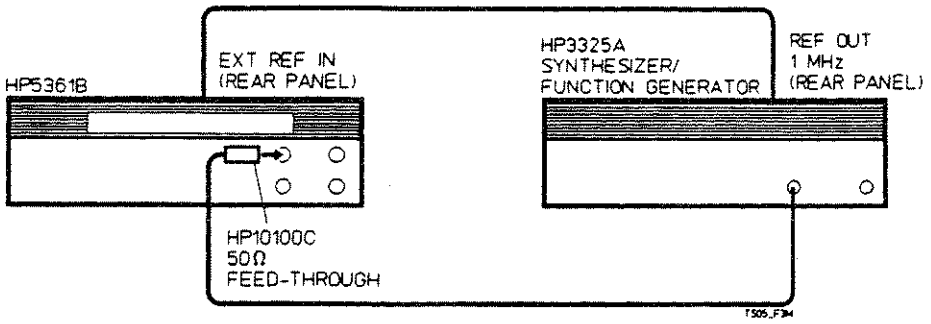


Figure 1-2. Setup 2: INPUT 2, 10 Hz - 20 MHz

6. 5361B settings are the same as in the 80 MHz test (INPUT 2, 1M Ω).

7. Connect the 3325A to INPUT 2 of the counter via a 50 Ω feedthrough. Set the 3325A for an output of 25 mV rms (–19.3 dBm) at 10 Hz.

8. Verify that the counter counts properly at 10 Hz, 50 kHz, 1 MHz, 10 MHz, and 20 MHz. Enter results in the Operation Verification Record.

1-14. INPUT 1, 500 MHz - MAX GHz CW Input Sensitivity Test

The following procedure checks the input sensitivity of input 1 for CW signals.

Specifications: Refer to *Table 1-2*, Operation Verification Record, on page 1-15 for CW input sensitivity specifications.

Description: The counter is set to the 500 MHz - MAX GHz range and the appropriate input signal is applied to INPUT 1 as shown in *Figure 1-1*. The generator is set to various frequencies/levels and the actual sensitivity of the HP 5361B is then measured.

1. Set the counter to INPUT 1, Automatic mode by pressing the AUTO key.

2. Connect the equipment as shown in *Figure 1-1* (INPUT 1 path). Do not install the 10 dB attenuator pad for CW measurement.

3. Set the 8340B to 500 MHz, –28 dBm (–20 dBm for Opt. 026/040), as measured on the 436A.

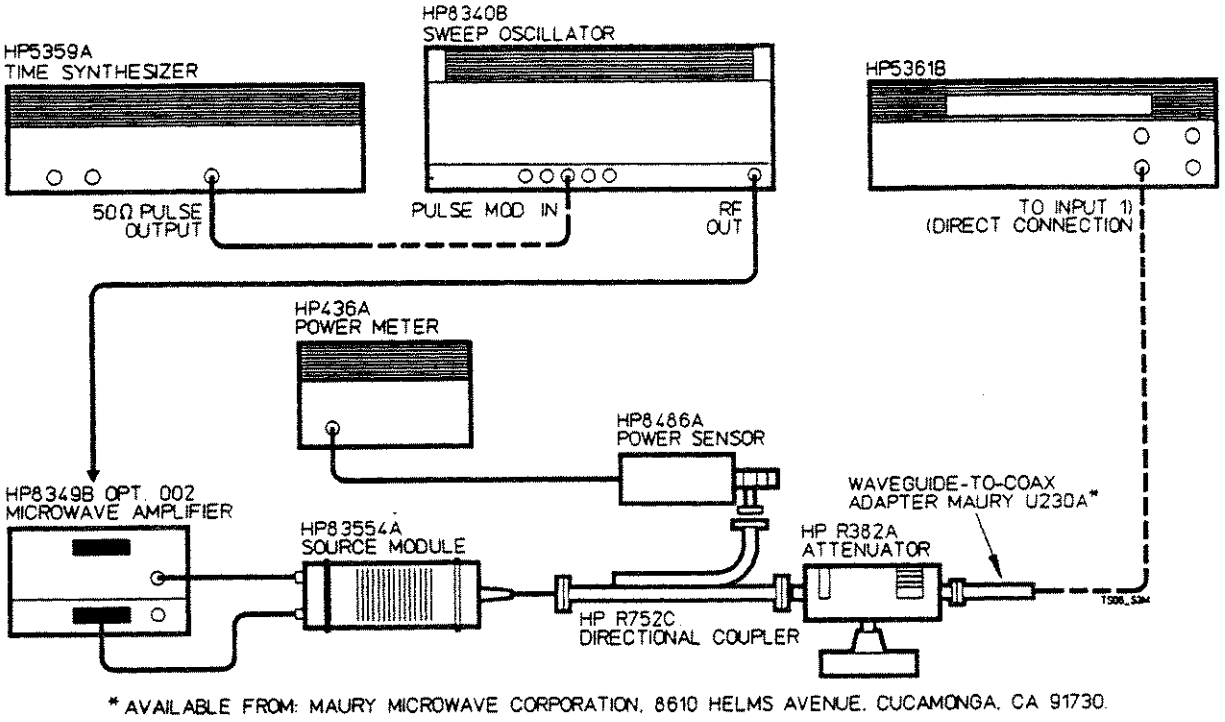


Figure 1-3. Setup 3: CW/Pulse 26.5 MHz - 40 GHz

4. Measure the actual sensitivity at 500 MHz, 1 GHz, 5 GHz, and 12.4 GHz. (Verify the signal level with the 436A Power Meter at each of these frequencies.) Enter the actual sensitivity result in the Operation Verification Record.

5. Set the 8340B to 18 GHz, –23 dBm (–20 dBm for Opt. 026/040), as measured on the 436A.

6. Measure the actual sensitivity at 18 GHz and 20 GHz. (Verify the signal level with the 436A Power Meter at each of these frequencies.) Enter the actual sensitivity result in the Operation Verification Record.

7. If the counter under test has option 026/040 installed, measure the actual sensitivity at 22 GHz and 26.5 GHz. (Verify the signal level with the 436A Power meter at each of these frequencies.) Enter the actual sensitivity results in the Operation Verification Record.

8. If the counter under test has option 040 installed, continue with the following test steps and refer to *Figure 1-3*. Connect the equipment as shown in *Figure 1-3*. For CW mesurements DO NOT pulse-modulate the 8340B with the HP 5359A.

9. Set the 5361B to INPUT 1, Automatic mode by pressing the AUTO key.

10. Measure the actual sensitivity at 30 GHz, 34 GHz, and 40 GHz as follows:

    a. Set the 8340B to 15 GHz, and set the level for +17 dBm output from the 8349B Amplifier (as indicated on the 8349B front panel display).

    b. Add attenuation by adjusting the R382A Precision Attenuator until the counter stops measuring, then decrease attenuation until the counter begins correct measurement.

    c. Note the doubled frequency (30 GHz) power reading on the 436A, add +10 dB to the reading, and subtract the value of the R382A attenuator setting to obtain the sensitivity level of the counter.

    d. Repeat the above steps at 34 GHz and 40 GHz (17 and 20 GHz input to the source module, respectivly).

11. Enter the actual sensitivity result in the Operation Verification Record.

1-15. INPUT 1, 500 MHz - MAX GHz Pulse Input Sensitivity Test

Peak pulse power cannot be directly read from a power meter. Therefore, the following pulsed RF amplitude power relationship is presented as an example of how to interpret pulsed RF power readings. Refer to *Figure 1-4* for amplitude/time waveform relationship.

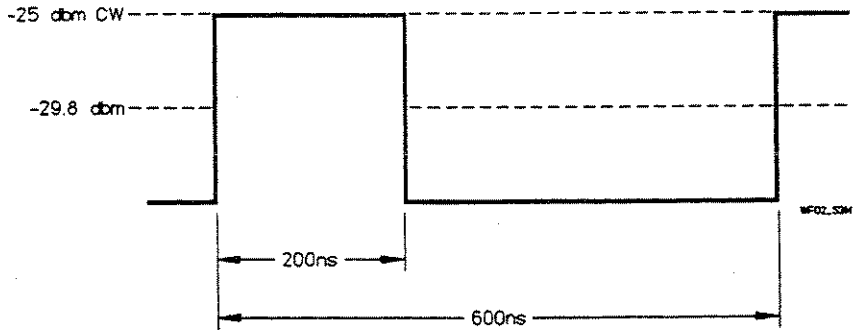


Figure 1-4. Pulsed RF Amplitude/Time Relationship

For pulsed RF signals having the same peak power level as an equivalent CW signal, a power meter will average the pulse power level and display a lower reading. This must be taken into account to arrive at the required peak pulse power when setting up the source power level. The relationship is as follows:

$$\text{Power Meter Reading} = \text{Required Input Power} + 10 \log \frac{\text{Pulse Width}}{\text{Pulse Repetition Interval}}$$

The example in *Figure 1-4* works out as follows:

$$\text{Power meter reading} = -25\ \text{dBm} + 10 \log \frac{200}{600}$$

$$= -25\ \text{dBm} + (-4.8\ \text{dBm})$$

$$= -29.8\ \text{dBm}$$

–29.8 dBm is what the power meter will read if the above signal conditions are used.

INPUT 1 PULSED RF SENSITIVITY TEST (500 MHz - MAX GHz)

The following specifications, setup illustration, and test steps describe the INPUT 1 pulsed RF sensitivity for the HP 5361B within 500 MHz - MAX GHz frequency range. *Figure 1-1* shows the test setup.

Specifications: Refer to *Table 1-2*, Operation Verification Record, on page 1-15 for pulse input sensitivity specifications.

1. Connect the 5359A output to the 8340B Pulse Modulation input.
2. Set the HP 5359A for a pulse width of 200 ns and a pulse period of 600 ns. Set the polarity to norm. and pos.; amplitude to midrange, and offset to off.
3. View the pulse on the oscilloscope to make final adjustment. The waveform time relationships should match those shown in *Figure 1-4* with pulse amplitude at 2.0V nominal.
4. Set the HP 436A Power Meter for auto range (Range Hold button OUT and dBm Mode).
5. Set the HP 8340B Synthesizer to 500 MHz and output power level for a reading of –22.8 dBm (–14.8 dBm for Opt. 026/040) on the 436A power meter, remember that:

$$\text{Power meter reading} = -28\ \text{dBm} + 10 \log \frac{200}{600} + 10\ \text{dB}$$

$$= -28\ \text{dBm} + (-4.8\ \text{dBm}) + 10\ \text{dB}$$

$$= -22.8\ \text{dBm}$$

6. Power-up the HP 5361B counter and observe automatic selection/display of pulse mode and measurement. If Option 040 is installed, select the Low Band by pressing the SET/ENTER then FREQUENCY keys so that "LOWER FREQ BAND" is displayed.

7. Verify that the HP 5361B counts correctly at 500 MHz, 1 GHz, 5 GHz, and 12.4 GHz.

NOTE

The count accuracy of the HP 5361B is shown in Graphs 2 and 3, Resolution and Gate Error, of the Appendix A Specifications for a 200 ns pulse when the counter is phase-locked to a house standard.

8. Change the power level from –22.8 dBm to –17.8 dBm (–14.8 dBm for Opt. 026/040) and verify that the HP 5361B counts correctly at 18 GHz and 20 GHz.

9. Enter the actual sensitivity results in the Operation and Verification Record.

10. If the counter under test has option 026/040 installed, measure the actual sensitivity at 22 GHz and 26.5 GHz and change the power level to –14.8 dBm as measured with the 436A power meter.

11. Enter the actual sensitivity result in the Operation Verification Record.

12. If the counter under test has option 040 installed, refer to *Figure 1-3* for the test setup.

13. Pulse modulate the 8340B with the output of the 5359A for a pulse width of 200 ns and a pulse period of 600 ns.

14. Set the polarity to NORM. and POS.; pulse amplitude to 2V and offset to OFF.

15. View the pulse on an oscilloscope to make final adjustment. The waveform time relationship should match that shown in *Figure 1-4* with a pulse amplitude of 2V.

16. Set the counter to INPUT 1, Automatic mode by pressing the AUTO key. If Option 040 is installed, select the High Band by pressing the SET/ENTER then FREQUENCY keys so that "HIGHER FREQ BAND" is displayed.

17. Measure the actual sensitivity at 30 GHz, 34 GHz, and 40 GHz as follows:

    a. Set the 8340B to 15 GHz, and set the level for a +17 dBm output from the 8349B amplifier (as indicated on the 8349B front panel display).

    b. Add attenuation by adjusting the R382A Precision Attenuator until the counter stops measuring, then decrease attenuation until the counter begins correct measurement.

    c. Note the doubled frequency (30 GHz) power reading on the 436A, add +10 dB to the reading, and subtract the value of the R382A attenuator setting to obtain the sensitivity level of the counter.

d. Repeat the above steps at 34 GHz and 40 GHz (17 and 20 GHz input to the source module, respectively).

18. Enter the actual sensitivity result in the Operation Verification Record.

1-16. HP-IB VERIFICATION

The program listed at the end of this appendix exercises the HP 5361B through various operating modes via the counter's HP-IB interface. If the counter successfully completes all phases of the verification program, there is a high probability that the HP-IB interface (A11 Assembly) is operating correctly. You'll need to pass all check points of the verification program. Refer to the *Figure 1-5.*

This program is not intended to be an automated test system for operation verification of the entire counter, but rather an aid to verify that the HP-IB interface is handshaking properly, sending valid data to the controller, and controlling the counter properly. If the HP 5361B does not respond as described, refer to A11 HP-IB Interface Assembly troubleshooting in Section 5 of the Service manual.

To perform the verification, set up the HP 5361B, HP 9000 Series 200/300 Controller, and signal source as shown in *Figure 1-5.* The program will function with any valid HP-IB address set for the counter. The first setup is for CW signal verification only and is used for program check points 12, 13, 14, and 15. The second setup is a minor variation of the CW setup that verifies pulse signal operation for program check point 16.

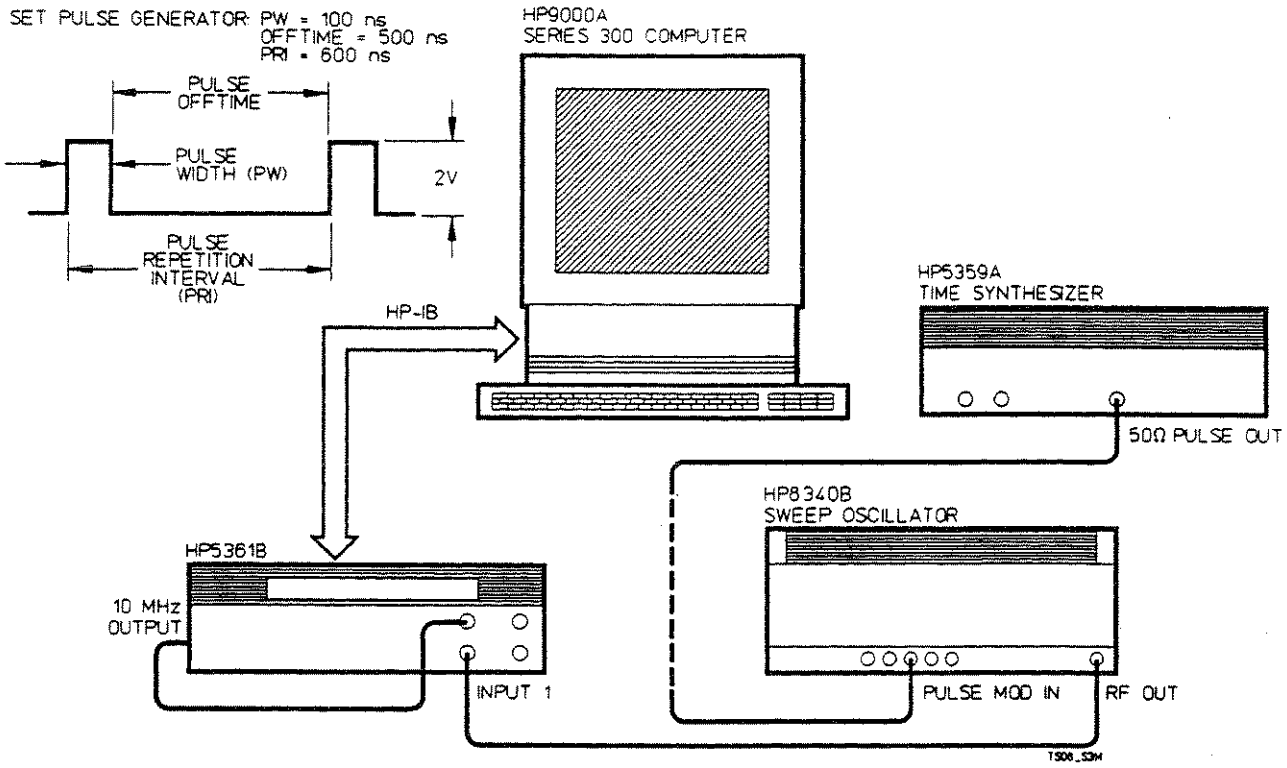


Figure 1-5. Setup: HP-IB Verification, CW/Pulse

1. HP-IB CW verification procedure.

   a. Set the HP 8340B sweep oscillator for 1 GHz at 0 dBm.

   b. (Do not pulse modulate the HP 8340B at this time.)

   c. Begin program execution, enter "5361A/B", and press RUN.

2. HP-IB Pulse verification procedure.

   a. Set the HP 8340B sweep oscillator for 1 GHz at 0 dBm.

   b. Set the HP 5359A for a pulse width of 100 ns and a pulse period of 600 ns. Set the polarity to norm. and pos.; amplitude to midrange, and offset to off.

   c. Observe the pulse signal on the oscilloscope using a 50 Ω termination for final adjustment. The waveform should conform to the one defined in *Figure 1-5*.

   d. When the pulse is correctly set, continue the program to check point 16.

e. The program is listed at the end of this appendix may be keyed into the Controller, or may be loaded from an HP-IB Verification Diskette, HP P/N 05361-13502 (5 1/4" media) and 05361-13501 (3 1/2" media). To run the program on the disk, insert the diskette into the Controller, load the program "5361A/B", and press RUN.

The program goes through 17 checkpoints, including a test to verify remote response at all legal addresses (Checkpoint 17). At the conclusion of each checkpoint, the operator is requested to enter the results of the current checkpoint. These results are stored and can be printed upon completion of the program. *Table 1-1* is a sample of the results of the HP-IB Verification program. The actual printed results should be attached to the Operation Verification Record (*Table 1-2*).

Various checkpoints throughout the program ask the operator to verify that the counter's OPEN annunciator is on, as well as other annunciators. Note that if a signal is present at the appropriate input, the OPEN annunciator should be flashing at a rate proportional to the sample rate.

Table 1-1. Sample HP-IB Verification Listing

CHECKPOINT SUMMARY:		HP-IB VERIFICATION RESULTS:	
1	Remote, Local Lockout, Local	CHECKPOINT	RESULTS
2	Self Check ('TEST?')	1	PASS
3	'DISPLAY'	2	PASS
4	'INIT' & 'RESET'	3	PASS
5	'REF' & 'OVEN'	4	PASS
6	'ERR?'	5	PASS
7	'SET' & 'SET?'	6	PASS
8	'LOWZ' & 'HIGHZ'	7	NOT PERFORMED
9	'SAMPLE' & 'TRIGGER'	8	PASS
10	'RESOL' & 'HIRESOL'	9	PASS
11	'OFFSET', 'SCALE' & 'SMOOTH'	10	PASS
12	'AUTO' & 'MANUAL'	11	PASS
13	'FMRATE'	12	PASS
14	'SRQMASK'	13	PASS
15	'DUMP'	14	PASS
16	'PULSE MEASUREMENT'	15	PASS
17	CHECK ALL ADDRESSES	16	NOT PERFORMED
		17	PASS

Table 1-2. Operation Verification Record

Hewlett-Packard Model 5361B
Pulse/CW Microwave Counter

Repair/Work Order No. _____

Serial Number: _____

Temperature: _____

Test Performed By: _____

Relative Humidity: _____

Date: _____

Post Calibration Test: ☐

Notes: _____

Pre Calibration Test: ☐

TEST	TEST RESULTS	SPECIFICATION		
Power-Up Self Test	Pass___ Fail___			
INPUT 2, Counting Check	Pass___ Fail___			
INPUT 2, 10 Hz-525 MHz Input Sensitivity Test (50 Ω/1M Ω):	(record actual sensitivity)			
50 Ω: 50 MHz	_____	25 mV rms (–19.3 dBm)		
100 MHz	_____			
250 MHz	_____			
525 MHz	_____			
1M Ω: 10 Hz	_____			
50 kHz	_____			
1 MHz	_____			
10 MHz	_____			
20 MHz	_____			
80 MHz	_____			
INPUT 1, 500 MHz - MAX GHz CW Input Sensitivity Test:		**20 GHz**	**26.5 GHz (Opt. 026)**	**40 GHz (Opt. 040)**
500 MHz	_____	–28 dBm	–20 dBm	–20 dBm
1 GHz	_____			
5 GHz	_____			
12.4 GHz	_____			
18 GHz	_____	–23 dBm		
20 GHz	_____	–23 dBm		
22 GHz	_____			
26.5 GHz	_____		–20 dBm	–20 dBm
30 GHz	_____	N/A		–18.7 dBm
34 GHz	_____			–17.2 dBm
40 GHz	_____			–15 dBm
HP-IB Verification	Pass___ Fail___			

Table 1-2. Operation Verification Record (Continued)

Hewlett-Packard Model 5361B Pulse/CW Microwave Counter				
TEST	**TEST RESULTS**	**SPECIFICATION**		
INPUT 1, 500 MHz - MAX GHz Pulse Input Sensitivity Test:		**20 GHz**	**26.5 GHz (Opt. 026)**	**40 GHz (Opt. 040)**
500 MHz	_____	–28 dBm	–20 dBm	–20 dBm
1 GHz	_____			
5 GHz	_____			
12.4 GHz	_____			
18 GHz	_____	–23 dBm		
20 GHz	_____	–23 dBm		
22 GHz	_____			
26.5 GHz	_____		–20 dBm	–20 dBm
30 GHz	_____	N/A		–18.7 dBm
34 GHz	_____			–17.2 dBm
40 GHz	_____			–15 dBm

Table 1-3. Performance Test Record (Page 1 of 2)

Hewlett-Packard Model 5361B
Pulse/CW Microwave Counter

Repair/Work Order No. _____

Serial Number: _____

Temperature: _____

Test Performed By: _____

Relative Humidity: _____

Date: _____

Post Calibration Test: ☐

Notes: _____

Pre Calibration Test: ☐

TEST	TEST RESULTS	SPECIFICATION		
INPUT 2, 10 MHz-525 MHz				
Input Sensitivity (50 Ω):				
50 MHz	_____	25 mV rms (–19.3 dBm)		
100 MHz	_____			
200 MHz	_____			
400 MHz	_____			
INPUT 2, 10 Hz-80 MHz				
Input Sensitivity (1M Ω):				
10 Hz	_____	25 mV rms (–19.3 dBm)		
1 kHz	_____			
500 kHz	_____			
1 MHz	_____			
10 MHz	_____			
50 MHz	_____			
80 MHz	_____			
INPUT 1, 500 MHz - MAX GHz				
CW Input Sensitivity:		**20 GHz**	**26.5 GHz (Opt. 026)**	**40 GHz (Opt. 040)**
500 MHz	_____	–28 dBm	–20 dBm	–20 dBm
1 GHz	_____			
2.5 GHz	_____			
5 GHz	_____			
10 GHz	_____			
12.4 GHz	_____	–23 dBm		
16 GHz	_____			
18 GHz	_____			
19 GHz	_____			
20 GHz	_____	–23 dBm		
22 GHz	_____			
24 GHz	_____			
26.5 GHz	_____		–20 dBm	–20 dBm
30 GHz	_____	N/A		–18.7 dBm
34 GHz	_____			–17.2 dBm
40 GHz	_____			–15 dBm

Table 1-3. Performance Test Record (Page 2 of 2)

Hewlett-Packard Model 5361B
Pulse/CW Microwave Counter

TEST	TEST RESULTS	SPECIFICATION		
		20 GHz	26.5 GHz (Opt. 026)	40 GHz (Opt. 040)
INPUT 1, 500MHz - MAX GHz Pulse Input Sensitivity Test:				
500 MHz	_____	–28 dBm	–20 dBm	–20 dBm
1 GHz	_____			
2.5 GHz	_____			
5 GHz	_____			
10 GHz	_____			
12.4 GHz	_____			
16 GHz	_____	–23 dBm		
18 GHz	_____			
19 GHz	_____			
20 GHz	_____	–23 dBm		
22 GHz	_____			
24 GHz	_____			
26.5 GHz	_____		–20 dBm	–20 dBm
30 GHz	_____	N/A		–18.7 dBm
34 GHz	_____			–17.2 dBm
40 GHz	_____			–15 dBm
Pulse Frequency Profile	Pass___ Fail___			
FM Rate Tolerance: Normal Rate (1 kHz)	Pass___ Fail___			
Low Rate (45 Hz)	Pass___ Fail___			
Trafck Rate (300 kHz)	Pass___ Fail___			
INPUT 1, Pulse Width/Repetition Frequency test:				
Auto Mode, 100 ns, 2 MHz PRF	Pass___ Fail___			
Manual Mode, 90 ns, 2 MHz PRF	Pass___ Fail___			
Autol Mode, 2 ms, 50 Hz PRF	Pass___ Fail___			
External Arm/Gate tests:				
External Arm mode	Pass___ Fail___			
External Gate mode	Pass___ Fail___			
HP-IB Verification	Pass___ Fail___			

1-17. PERFORMANCE TEST PROCEDURES

1-18. INPUT 2, 10 Hz - 525 MHz CW Input Sensitivity Test

The following test is in two parts, Setup 1 for 50 MHz to 525 MHz, and Setup 2 for 10 Hz to 10 MHz.

Specification: 50 Ω: 10 MHz - 525 MHz, 25 mV rms
1 M Ω: 10 Hz - 80 MHz, 25 mV rms

Description: The counter is set to the 10 MHz - 525 MHz range, 50 Ω impedance, and a 25 mV rms (–19.3 dBm) signal is applied to Input 2 as shown in *Figure 1-1*. The test generator is set to selected frequencies and the 5361B is checked for proper counting. The counter is next set for 1MΩ impedance, a 25 mV rms (–19.3 dBm) 80 MHz signal is applied to INPUT 2 through a 50 Ω feedthrough, and the counter is checked for proper counting. The test setup is changed to Setup 2 to test the 10 Hz - 20 MHz range as shown in *Figure 1- 2*.

1. Set the counter to the 10 MHz - 525 MHz range, 50 Ω impedance, by pressing the 50 Ω key.

2. Set the 8340B to 50 MHz and an output level of 25 mV rms (–19.3 dBm) as measured on the 436A Power Meter. Measure actual sensitivity and verify that the 5361B counts properly at 50 MHz, 100 MHz, 200 MHz, 400 MHz, and 525 MHz. Enter the results in the Performance Test Record (*Table 1-3*).

3. Insert a 50 Ω feedthrough between the 11667B power splitter and INPUT 2 of the counter. Press the 1M Ω key on the counter to select the 1M Ω impedance, 10 Hz - 80 MHz input.

4. Set the 8340B to 80 MHz and a level of 25 mV rms (–19.3 dBm) as measured on the 436A Power Meter.

5. Verify that the 5361B properly counts 50 MHz and 80 MHz at 25 mV rms, and enter the result in the Performance Test Record.

Change to test setup 2 to check the 10 Hz-20 MHz range with the following procedure.

1. 5361B settings are the same as in the 50 MHz and 80 MHz test (INPUT 2, 1M Ω).

2. Connect the 3325A to INPUT 2 of the counter via a 50 Ω feedthrough. Set the 3325A for an output of 25 mV rms (–19.3 dBm) at 10 Hz.

3. Verify that the counter counts properly at 10 Hz, 1 kHz, 500 kHz, 1 MHz, and 10 MHz. Enter results in the Performance Test Record.

1-19. INPUT 1, 500 MHz - MAX GHz CW Input Sensitivity Test

The following procedure checks the input sensitivity of input 1 for CW signals.

Specifications: Refer to *Table 1-3*, Performance Test Record, on page 1-17 for CW input sensitivity specifications.

Description: The counter is set to the 500 MHz - MAX GHz range and the appropriate input signal is applied to INPUT 1 as shown in *Figure 1-1*. The generator is set to various frequencies/levels and the actual sensitivity of the HP 5361B is then measured.

1. Set the counter to INPUT 1, Automatic mode by pressing the AUTO key.
2. Connect the equipment as shown in Figure C-1 (INPUT 1 path). Do not install the 10 dB attenuator pad for CW measurement.
3. Set the 8340B to 500 MHz, –28 dBm (–20 dBm for Opt. 026/040), as measured on the 436A.
4. Measure the actual sensitivity at 500 MHz, 1 GHz, 2.5 GHz, 5 GHz, 10 GHz, and 12.4 GHz. (Verify the signal level with the 436A Power Meter at each of these frequencies.) Enter the actual sensitivity result in the Performance Test Record.
5. Set the 8340B to 16 GHz, –23 dBm (–20 dBm for Opt. 026/040), as measured on the 436A.
6. Measure also the actual sensitivity at 18 GHz, 19 GHz, and 20 GHz. (Verify the signal level with the 436A Power Meter at each of these frequencies.) Enter the actual sensitivity result in the Performance Test Record.
7. If the counter under test has option 026/040 installed, measure the actual sensitivity at 22 GHz, 24 GHz, and 26.5 GHz. (Verify the signal level with the 436A Power meter at each of these frequencies.) Enter the actual sensitivity results in the Performance Test Record.
8. If the counter under test has option 040 installed, continue with the following test steps. (Refer to *Figure 1-3*.) Connect the equipment as shown in *Figure 1-3*. For CW mesurements DO NOT pulse-modulate the 8340B.
9. Set the 5361B to INPUT 1, Automatic mode by pressing the AUTO key.

10. Measure the actual sensitivity at 30 GHz, 34 GHz, and 40 GHz as follows:

    a. Set the 8340B to 15 GHz, and set the level for +17 dBm output from the 8349B Amplifier (as indicated on the 8349B front panel display).

    b. Add attenuation by adjusting the R382A Precision Attenuator until the counter stops measuring, then decrease attenuation until the counter begins correct measurement.

    c. Note the doubled frequency (30 GHz) power reading on the 436A, add +10 dB to the reading, and subtract the value of the R382A attenuator setting to obtain the sensitivity level of the counter.

    d. Repeat the above steps at 34 GHz and 40 GHz (17 and 20 GHz input to the source module, respectivly).

11. Enter the actual sensitivity result in the Performance Test Record.

1-20. INPUT 1, 500 MHz - MAX GHz Pulse Input Sensitivity Test

Peak pulse power cannot be directly read from a power meter. Therefore, the following pulsed RF amplitude power relationship is presented as an example of how to interpret pulsed RF power readings. Refer to *Figure 1-4* for amplitude/time waveform relationship.

For pulsed RF signals having the same peak power level as an equivalent CW signal, a power meter will average the pulse power level and display a lower reading. This must be taken into account to arrive at the required peak pulse power when setting up the source power level. The relationship is as follows:

$$\text{Power Meter Reading} = \text{Required Input Power} + 10 \log \frac{\text{Pulse Width}}{\text{Pulse Repetition Interval}}$$

The example in *Figure 1-4* works out as follows:

$$\text{Power meter reading} = -25 \text{ dBm} + 10 \log \frac{200}{600}$$

$$= -25 \text{ dBm} + (-4.8 \text{ dBm})$$

$$= -29.8 \text{ dBm}$$

–29.8 dBm is what the power meter will read if the above signal conditions are used.

INPUT 1 PULSED RF SENSITIVITY TEST (500 MHz - MAX GHz)

The following specifications, setup illustration, and test steps describe the INPUT 1 pulsed RF sensitivity for the HP 5361B within 500 MHz - MAX GHz frequency range. *Figure 1-1* shows the test setup.

Specifications: Refer to *Table 1-3*, Performance Test Record, on page 1-17 for CW input sensitivity specifications.

1. Connect the 5359A output to the 8340B Pulse Modulation input.
2. Set the HP 5359A for a pulse width of 200 ns and a pulse period of 600 ns. Set the polarity to norm. and pos.; amplitude to midrange, and offset to off.
3. View the pulse on the oscilloscope to make final adjustment. The waveform time relationships should match those shown in *Figure 1-4* with pulse amplitude at 2.0V nominal.
4. Set the HP 436A Power Meter for auto range (Range Hold button OUT and dBm Mode).
5. Set the HP 8340B Synthesizer to 500 MHz and output power level for a reading of –22.8 dBm (–14.8 dBm for Opt. 026/040) on the 436A power meter, remember that:

$$\text{Power meter reading} = -28\ \text{dBm} + 10 \log \frac{200}{600} + 10\ \text{dB}$$

$$= -28\ \text{dBm} + (-4.8\ \text{dBm}) + 10\ \text{dB}$$

$$= -22.8\ \text{dBm}$$

6. Power-up the HP 5361B counter and observe automatic selection/display of pulse mode and measurement. If Option 040 is installed, select the Low Band by pressing the SET/ENTER then FREQUENCY keys so that "LOWER FREQ BAND" is displayed.
7. Verify that the HP 5361B counts correctly at 500 MHz, 1 GHz, 2.5 GHz, 5 GHz, 10 GHz, and 12.4 GHz.

NOTE

The count accuracy of the HP 5361B is shown in Graphs 2 and 3, Resolution and Gate Error, of the Appendix A Specifications for a 200 ns pulse when the counter is phase-locked to a house standard.

8. Change the power level from –22.8 dBm (–14.8 dBm for Opt. 026/040) to –17.8 dBm and verify that the HP 5361B counts correctly at 16 GHz, 18 GHz, 19 GHz, and 20 GHz.

9. Enter the actual sensitivity results in the Performance Test Record.

10. If the counter under test has option 026/040 installed, measure the actual sensitivity at 22 GHz, 24 GHz, and 26.5 GHz and change the power level to –14.8 dBm as measured with the 436A power meter.

11. Enter the actual sensitivity result in the Performance Test Record.

12. If the counter under test has option 040 installed, refer to *Figure 1-3* for the test setup.

13. Pulse modulate the 8340B with the output of the 5359A for a pulse width of 200 ns and a pulse period of 600 ns.

14. Set the polarity to NORM. and POS.; pulse amplitude to 2V and offset to OFF.

15. View the pulse on an oscilloscope to make final adjustment. The waveform time relationship should match that shown in *Figure 1-4* with a pulse amplitude of 2V.

16. Set the counter to INPUT 1, Automatic mode by pressing the AUTO key. If Option 040 is installed, select the High Band by pressing the SET/ENTER then FREQUENCY keys so that "Higher FREQ BAND" is displayed.

17. Measure the actual sensitivity at 30 GHz, 34 GHz, and 40 GHz as follows:

    a. Set the 8340B to 15 GHz, and set the level for a +17 dBm output from the 8349B amplifier (as indicated on the 8349B front panel display).

    b. Add attenuation by adjusting the R382A Precision Attenuator until the counter stops measuring, then decrease attenuation until the counter begins correct measurement.

    c. Note the doubled frequency (30 GHz) power reading on the 436A, add +10 dB to the reading, and subtract the value of the R382A attenuator setting to obtain the sensitivity level of the counter.

    d. Repeat the above steps at 34 GHz and 40 GHz (17 and 20 GHz input to the source module, respectively).

18. Enter the actual sensitivity result in the Performance Test Record.

1-21. Pulse Frequency Profile Test

Specifications: Pass/Fail

Description: The Profile function for pulse frequency is exercised and evaluated for Pass/Fail.

Procedure: Refer to the procedure below, and use the pulse signal setup for the previous pulse performance sensitivity test at 12.4 GHz.

1. Set up the 8340B and 5359A as shown in *Figure 1-1.*
2. Set the 8340B for a frequency of 12.4 GHz and the 5359A for a pulse width of 200 ns with a pulse period of 600 ns as in the previous pulse sensitivity test.
3. Set the sample rate to HOLD by pressing SET/ENTER, SAMPLE RATE, DEC, keys until "HOLD" is displayed, then press SET/ENTER.
4. Connect a cable (model 10833A, 1 metre) from the HP-IB connecftor on the rear of the 5361B to one of the compatable printers.
5. Set the printer to Listen Only Mode. This is done by setting the HP-IB address switch to "Listen Always" on the back of the printer, then cycling ac power.
6. Now set the 5361B to Talk Only by setting HP-IB address to 31. This can be done through the front panel using the key sequency SET/ENTER, HP-IB Address, 3, 1, SET/ENTER.
7. Press the FREQUENCY/PROFILE key once.
8. When you want to begin the profiling process, press the TRIGGER key and observe the printer for output of a hardcopy profile plot.
9. If the printer produces a hardcopy profile plot, then the counter has passed this test.

1-22. FM Tolerance Test (CW Only)

Specifications: 20 MHz maximum peak-to-peak deviation
12 MHz maximum peak-to-peak deviation for Opt. 040.

Description: The FM peak-to-peak deviation specification is the worst case FM deviation that can be present on a carrier that the instrument can acquire and count. The counter averages out the deviations and displays a carrier frequency. In addition, the HP 5361B offers a choice of FM rate modes. This test will verify that the counter performs properly in all three modes. Test setup is shown in *Figure 1-6.*

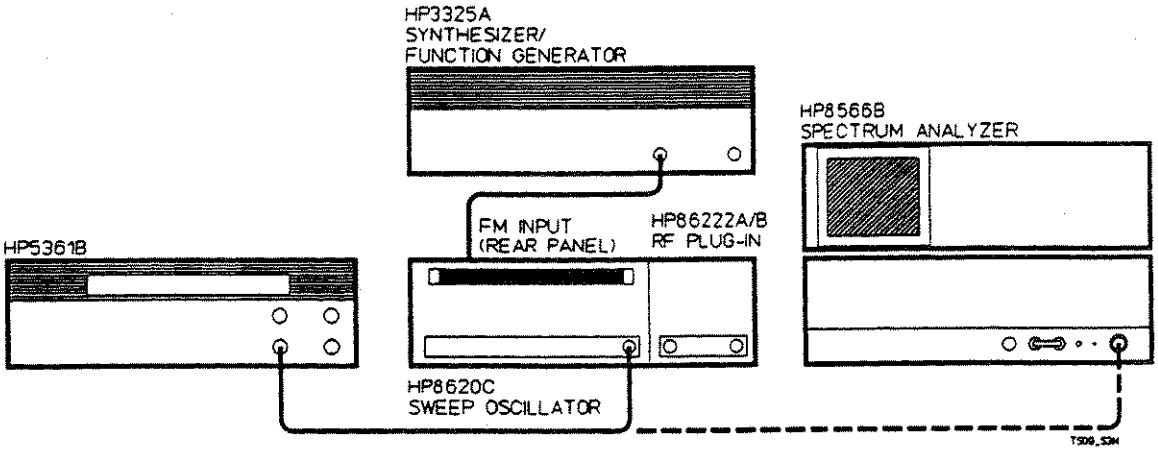


Figure 1-6. Setup: FM Tolerance Test

1. Set the 8620C to 1 GHz.
2. Set the 86222A/B to –5 dBm.
3. Set the 3325A to 1 kHz.
4. Set the output amplitude of the 3325A to achieve a peak-to-peak width of 20 MHz. To set the amplitude, use the 8565A Spectrum Analyzer to verify the width of the FM deviation at the output of the 86222A/B.
5. Verify that the counter acquires and correctly counts the modulated input. Enter the result in the Performance Test Record.
6. Set the 5361B to extended function 6 by pressing the following key sequence: SET/ENTER, EXTEND FUNCT, 6, SET/ENTER. The counter will display the harmonic number, including the fractional portion.

7. Verify that the displayed fractional portion does not deviate more than 0.30 from the integer value. For example, a harmonic number of 3 should not deviate to less than 2.70 or greater than 3.30.

8. Set the 3325A to 45 Hz.

9. Set the 5361B to Low FM Rate by pressing the FM RATE/TRACK key. The LOW annunciator will turn on.

10. Verify that the fractional portion of the harmonic number still does not deviate more than 0.30 from the integer value.

11. Press the RESET/LOCAL key and verify that the displayed count matches that of the normal FM rate mode (step 5). Enter the result in the Performance Test Record.

12. Set the 3325A to 300 kHz.

13. Set the 5361B to Track rate by pressing the FM RATE/TRACK key. The TRACK annunciator will turn on.

14. Set the 5361B to extended function 6 by pressing the EXTEND FUNCT key.

15. Verify that the fractional portion of the harmonic number still does not deviate more than 0.30 from the integer value.

16. Press the RESET/LOCAL key and verify that the displayed count matches that of the normal FM rate mode (step 5).

17. Enter the results in the Performance Test Record.

If the counter fails the FM tolerance test, refer to Section 2, Adjustments in the Service manual, and verify the A6 IF Amplifier/Detector Assembly adjustments. If the adjustments are correct and the counter continues to fail, refer to the troubleshooting information in Section 5 in the Service manual for procedures to diagnose and repair the following assemblies:

A6 IF Amplifier/Detector Assembly
Microwave Module (A12 Microwave Assembly/U1 Sampler)

1-23. INPUT 1 Pulse Width/Repetition Frequency Test

The following test is in three parts, test one for 100 ns pulse width, test two for manual mode, 90 ns, 2 MHz PRF, and test three for auto mode, 2 ms, 50 Hz PRF.

Specifications: Test 1 - Auto Mode, 100 ns, 2 MHz PRF: Pass/Fail
Test 2 - Manual Mode, 90 ns, 2 MHz PRF: Pass/Fail
Test 3 - Auto Mode, 2 ms, 50 Hz PRF: Pass/Fail

Description: The counter is set to the 500 MHz - MAX GHz range and the appropriate input signal is applied to INPUT 1 as shown in *Figure 1-1*. The synthesized signal generator is set to 10 GHz, and the actual sensitivity of the 5361B is observed for the three pulse mode test cases listed above.

AUTO MODE, 100 ns, 2 MHz PRF

The referenced setup illustration and test steps describe the INPUT 1, 100 ns pulse width test for the HP 5361B 10 GHz. *Figure 1-1* shows the test setup.

1. Configure the HP 5359A to output a square wave with a 100 ns width, 500 ns pulse period, and amplitude of 2.0 volts. (Refer to *Figure 1-4* for a general profile of the waveform.)

2. Set the power switch of the HP 5361B to ON, enable Auto mode, and select 1 kHz resolution.

3. Set the HP 436A power meter for auto range (Range Hold button out) and dBm mode.

4. Set the HP 8340B synthesized signal generator to 10 GHz and output power level to for a power meter (436A) reading of –25 dBm:

$$\text{Power meter reading} = -28\ \text{dBm} + 10 \log \frac{100}{500} + 10\ \text{dB}$$

$$= -28\ \text{dBm} + (-7\ \text{dBm}) + 10\ \text{dB}$$

$$= -25\ \text{dBm}$$

5. Verify that the 5361B counts correctly at 10 GHz to the accuracy shown in Graph 1 of the Appendix A Specifications with a 100 ns pulse.

NOTE

The count accuracy of the HP 5361B is shown in Graphs 2 and 3, Resolution and Gate Error, of the Appendix A Specifications when the counter is phase-locked to a house standard.

6. Record the test results on the Performance Test Record.

MANUAL MODE, 90 ns, 2 MHz PRF

The referenced setup illustration and test steps describe the INPUT 1, 90 ns pulse width test for the HP 5361B 10 GHz. *Figure 1-1* shows the test setup.

1. Configure the HP 5359A to output a square wave with a 90 ns width, 500 ns pulse period, and amplitude of 2.0 volts. (Refer to *Figure 1-4* for a general profile of the waveform.)

2. Set the power switch of the HP 5361B to ON, enable Auto mode, and select 1 kHz resolution.

3. Set the HP 436A power meter for auto range (Range Hold button out) and dBm mode.

4. Set the HP 8340B synthesized signal generator to 10 GHz and output power level to for a power meter (436A) reading of –25.45 dBm:

$$\text{Power meter reading} = -28\ \text{dBm} + 10 \log \frac{90}{500} + 10\ \text{dB}$$

$$= -28\ \text{dBm} + (-7.45\ \text{dBm}) + 10\text{dB}$$

$$= -25.45\ \text{dBm}$$

5. Set the counter to Manual mode with a center frequency of 10 GHz by pressing the following keys: SET/ENTER, MANUAL, 1, 0, GHz, SET/ENTER.

6. Set the counter to extended function 93 by pressing the following keys: SET/ENTER, EXTEND FUNCT, 9, 3, SET/ENTER.

7. Verify that the 5361B counts correctly at 10 GHz to the accuracy shown in Graph 1 of the Appendix A Specifications.

NOTE

The count accuracy of the HP 5361B is shown in Graphs 2 and 3, Resolution and Gate Error, of the Appendix A Specifications when the counter is phase-locked to a house standard.

8. Record the test results on the Performance Test Record.

9. Turn-off extended function 93 before conducting any further tests by pressing SET/ENTER, EXTENDED FUNCTION, 9, 3, SET/ENTER.

AUTO MODE, 2 ms, 50 Hz PRF

The referenced setup illustration and test steps describe the INPUT 1, Auto mode 50 Hz PRF test for the HP 5361B at 10 GHz. *Figure 1-1* shows the test setup.

1. Configure the HP 5359A to output a square wave with a 2 ms width, 20 ms pulse period, and amplitude of 2.0 volts. (Refer to *Figure 1-4* for a general profile of the waveform.)

2. Set the HP 5361B to 100 Hz resolution and enable Auto mode.

3. Set the HP 436A power meter for auto range (Range Hold button out) and dBm mode.

4. Set the HP 8340B synthesized signal generator to 10 GHz and output power level for a power meter (436A) reading of –28 dBm:

$$\text{Power meter reading} = -28\ \text{dBm} + 10 \log \frac{2\ \text{ms}}{20\ \text{ms}} + 10\ \text{dB}$$

$$= -28\ \text{dBm} + (-10\ \text{dBm}) + 10\ \text{dB}$$

$$= -38\ \text{dBm} + 10\ \text{dB}$$

$$= -28\ \text{dBm}$$

5. Verify the following pulse envelope parameters with the 5361B:

PRF	=	50 Hz
PRI	=	20 ms
OFFTIME	=	18 ms
PW	=	2 ms

6. Verify that the 5361B counts correctly at 10 GHz to the accuracy shown in Graph 1 of the Appendix A Specifications for a 2 ms pulse.

NOTE

The count accuracy of the HP 5361B is shown in Graphs 2 and 3, Resolution and Gate Error, of the Appendix A Specifications when the counter is phase-locked to a house standard.

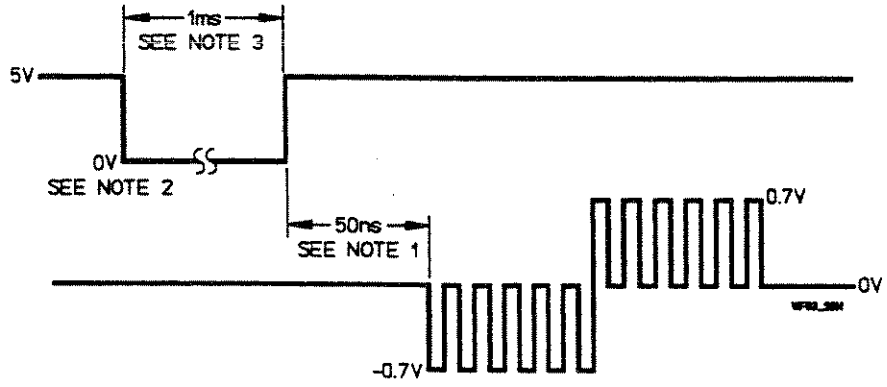
7. Record the test results on the Performance Test Record.

1-24. External Gate/Arm In Test

The following specifications, setup illustration, and test steps describe the External Gate/Arm In test for the HP 5361B at 10 GHz.

Specification: Pass/Fail

Description: This test checks for proper operation of the external front panel Gate/Arm input. An active low TTL signal edge is applied at the front panel GATE/ARM IN connector. This enables the counter to make a measurement on the next RF pulse burst. The arming active-low edge must occur at least 50 ns prior to the pulse burst of interest. The counter must correctly count the 10 GHz carrier at the specified power. *Figure 1-7* shows the test waveforms.



NOTES
1. ADJUST GATE PULSE NO CLOSER THAN 50ns AHEAD OF PULSE SIGNAL.
2. ADJUST 8012B OFFSET VERNIER TO ENSURE THAT THE BASELINE OF THE SQUARE WAVE IS AT 0 VOLTS.
3. ADJUST 8012B PULSE WIDTH VERNIER FOR PULSE WIDTH OF 1ms.
4. TIME DIMENSIONS ARE NOT DRAWN TO SCALE.

Figure 1-7. External Arm/Gate Mode Test Waveforms

The following procedure describes the External Arm Mode test for the HP 5361B at 10 GHz. *Figure 1-8* shows the test setup.

1. Set the HP 5359A for a pulse width of 2 ms, 1 ns delay, with the external trigger level at +2 volts. Set the polarity to norm. and pos.; amplitude to 2.5 volts, and offset to off.

2. Set the following parameters on the 8012B pulse generator:

   a. PULSE PERIOD . . . . . 10 ms - 1 ms
   b. PULSE PERIOD VERNIER . . . . . adjust for 20 ms PRI
   c. PULSE SWITCH . . . . . Normal
   d. DELAY . . . . . 0.1 ms - 10 ms
   e. PULSE WIDTH SWITCH . . . . . 0.1 ms - 10 ms
   f. PULSE WIDTH VERNIER . . . . . adjust for 1 ms (see *Figure 1-7*)
   g. TRANSITION TIME . . . . . N/A
   h. LEADING AND TRAILING EDGES . . . . . ccw
   i. AMPLITUDE SWITCH . . . . . 5V (Max)
   j. AMPLITUDE VERNIER . . . . . Max
   k. OFFSET SWITCH . . . . . ON
   l. PULSE POLARITY . . . . . Negative
   m. OUTPUT SWITCH . . . . . Normal
   n. INT. LOAD . . . . . In

3. Ensure that the above signal parameters are correct by observing the waveform on an oscilloscope with 50 Ω termination for final adjustment. The signal should appear as shown in the top waveform of *Figure 1-7* with a 5 volt amplitude.

4. The most critical setting is the offset vernier. Make this adjustment so that the base line of the square wave is at 0 V. To move the pulse signal left or right, adjust the 8012B delay vernier as needed.

5. Set the HP 436A Power Meter for auto range (Range Hold button OUT and dBm Mode).

6. Set the HP 8340B Synthesizer to 10 GHz and output power level for a reading of –20 dBm on the 436A power meter.

7. Power-up the HP 5361B counter, select 1 kHz resolution, and set the gate mode to Internal. If the counter is not energized from the STBY state, allow at least 30 minutes for complete warm-up. If Option 040 is installed, select the Low Band by pressing the SET/ENTER then FREQUENCY keys so that "LOWER FREQ BAND" is displayed.

8. Adjust the 8012B pulse delay vernier so the oscilloscope display conforms to the waveform shown in *Figure 1-7* (When using an analog scope, place the vertical display in chop position and internal trigger in channel B. Channel A - dc coupling, channel B - ac coupling.)

9. Verify the following pulse envelope parameters with the HP 5361B while set to the Internal Gate mode:

   PRF = 50 Hz
   PRI = 20 ms
   OFFTIME = 18 ms
   PW = 2 ms

   (Make the necessary adjustments to either the 5359A or 8012B to obtain the above values. Pulse width can be adjusted from the 5359A. PRI can be adjusted from the 8012B pulse period Vernier.)

10. Verify that the HP 5361B counts correctly at 10 GHz while set to Internal gate mode.

11. Set the gate mode to ARM and verify only that the HP 5361B counts the RF frequency correctly at 10 GHz while in external ARM gate mode.

    (Review *Figure 1-7* carefully and make additional fine tune adjustments to the offset and delay vernier for proper counter operation in the external ARM gate mode.)

12. Record the results on the Performance Test Record.

NOTE

The count accuracy of the HP 5361B is shown in Graphs 2 and 3, Resolution and Gate Error, of the Appendix A Specifications for a 200 ns Pulse when the counter is phase-locked to a house standard.

1-25. External Gate Mode Test

The following specifications, setup illustration, and test steps describe the External Gate mode test for the HP 5361B at 10 GHz.

Specification: Pass/Fail

Description: This test checks for proper operation of the External Gate mode. An active low TTL signal is applied at the front panel GATE/ARM IN connector from a pulse generator. The duration of this signal determines when the counter will make a measurement on the input RF pulse. The counter must correctly count the 10 GHz carrier at the specified power and display gate position relative to pulse onset/end via the front panel SCOPE-VIEW output.

The following procedure describes the External Gate Mode test for the HP 5361B at 10 GHz. *Figure 1-8* shows the test setup.

1. Set the HP 5359A for a pulse width of 2 ms, 1 ns delay, with the external trigger level at +2 volts. Set the polarity to norm. and pos.; amplitude to 2.5 volts, and offset to off.

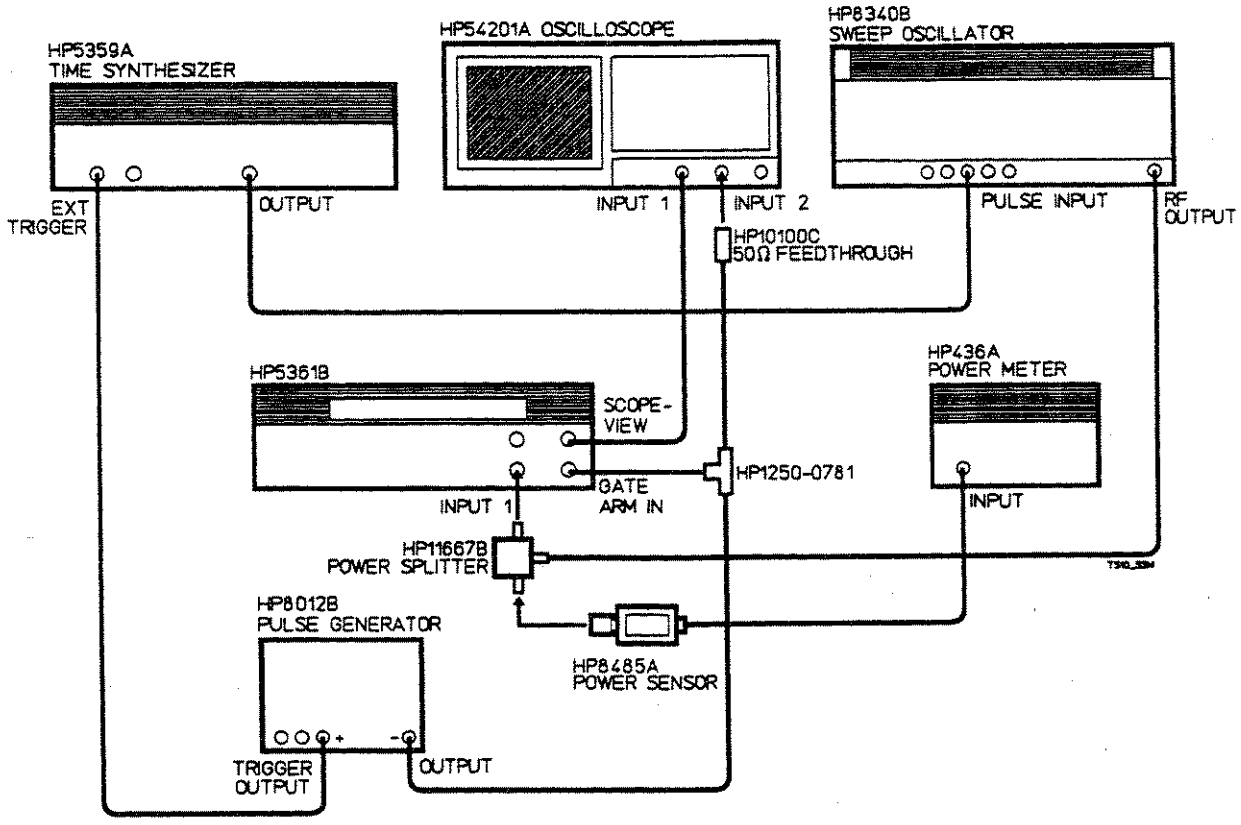


Figure 1-8. External Gate Mode Test and External Arm Mode Test

2. Set the following parameters on the 8012B pulse generator:

a. PULSE PERIOD . . . . . 10 ms - 1 ms
b. PULSE PERIOD VERNIER . . . . . adjust for 20 ms PRI
c. PULSE SWITCH . . . . . Normal
d. DELAY . . . . . 0.1 ms - 10 ms
e. PULSE WIDTH SWITCH . . . . . 0.1 ms - 10 ms
f. PULSE WIDTH VERNIER . . . . . adjust for 1 ms (see *Figure 1-9*)
g. TRANSITION TIME . . . . . N/A
h. LEADING AND TRAILING EDGES . . . . . ccw
i. AMPLITUDE SWITCH . . . . . 5V (Max)
j. AMPLITUDE VERNIER . . . . . Max

k. OFFSET SWITCH . . . . . ON
l. PULSE POLARITY . . . . . Negative
m. OUTPUT SWITCH . . . . . Normal
n. INT. LOAD . . . . . In

3. Ensure that the above signal parameters are correct by observing the waveform on an oscilloscope with 50 Ω termination for final adjustment. The signal should appear as shown in the top waveform of *Figure 1-9/A* with a 5 volt amplitude.

4. The most critical setting is the offset vernier. Adjust this control so that the square wave baseline is at 0 V. To move the square wave left or right, adjust the 8012B delay vernier.

5. Set the HP 436A Power Meter for auto range (Range Hold button OUT and dBm Mode).

6. Set the HP 8340B Synthesizer to 10 GHz and output power level for a reading of –20 dBm on the 436A power meter.

7. Power-up the HP 5361B counter, select 1 kHz resolution, and set the gate mode to Internal. If the counter is not energized from the STBY state, allow at least 30 minutes for complete warm-up. If Option 040 is installed, select the Low Band by pressing the SET/ENTER then FREQUENCY keys so that "LOWER FREQ BAND" is displayed.

8. Adjust the 8012B pulse delay vernier so the oscilloscope display conforms to the waveform shown in *Figure 1-9/B* (When using an analog scope, place the vertical display in chop position and internal trigger in channel B. Channel A - dc coupling, channel B - ac coupling.)

9. Verify the following pulse envelope parameters with the HP 5361B while set to Internal Gate mode:

   PRF = 50 Hz
   PRI = 20 ms
   OFFTIME = 18 ms
   PW = 2 ms

   (Make the necessary adjustments to either the 5359A or 8012B to obtain the above values. Pulse width can be adjusted from the 5359A. PRI can be adjusted from the 8012B pulse period Vernier.)

10. Verify that the HP 5361B counts correctly at 10 GHz with Internal gate mode.

11. Set the gate mode to External and verify that the HP 5361B counts correctly at 10 GHz with External gate mode. Review *Figure 1-9* carefully and make additional fine tune adjustments to the 8012B offset or delay vernier settings for proper counter operation while in External gate mode.

    The External Gate mode should be used to measure the RF frequency only, and not the pulse envelope parameters.

12. Record the results on the Performance Test Record.

NOTE

The count accuracy of the HP 5361B is shown in Graphs 2 and 3, Resolution and Gate Error, of the Appendix A Specifications for a 2 ms Pulse when the counter is phase-locked to a house standard.

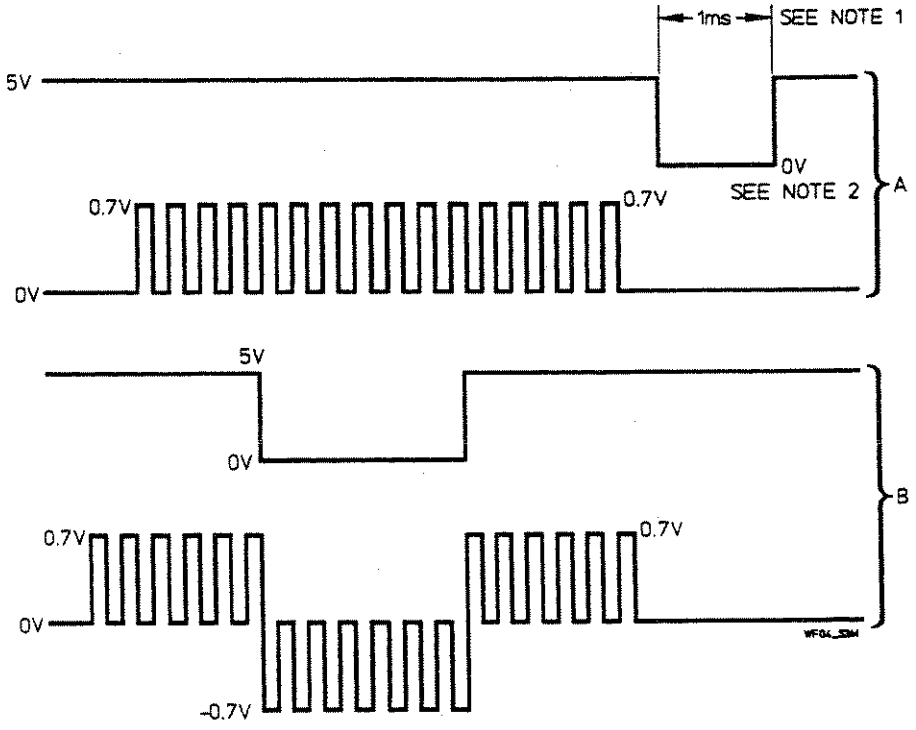


Figure 1-9. External Gate Mode Test Waveforms

1-26. HP 9000 Program Listing

```
10      !HP5361A/B MICROWAVE FREQUENCY PULSE COUNTER
20      !THIS PROGRAM IS DESIGNED TO WORK ON A SERIES 200 COMPUTER. TO CONVERT
30      !IT FOR ANOTHER COMPUTER, MAKE SURE THE MASK BIT IS PROPERLY SET IN CHECK PO40 !INT 14.
40      !
50      !THIS VERSION ALSO ALLOWS USERS TO CHANGE THE HP-IB ADDRESS OF THE PRINTER
60      ! HP-IB OPERATIONAL VERIFICATION PROGRAM
70      ! AJ
80      ! DATE: 890525
90      ! REVISION A
100     ! This program exercises the 5361A/B through the majority of its command
110     ! code set via HP-IB. The program consists of 17 checkpoints, and
120     ! provides the user with the ability to execute and repeat these tests
130     ! in any order. Also provided are options to print the checkpoint
140     ! summary and results. The program relies on subroutines in addition
150     ! to arrays and simple variables.
160     !
170     OPTION BASE 1
180     DIM Ascii_data$[24],Horiz_line$[80],Inst_id$[7]
190     DIM Setup$[76],Title$[80]
200     DIM Fail_address(30),Pass_address(30),Test_results$(20)[13]
210     INTEGER Test_number
220     Initialize:                             !
230     ON ERROR GOTO Error_exit
240     PRINTER IS CRT
250     CONTROL KBD,1;0
260     CONTROL KBD,2;2
270     OUTPUT KBD;CHR$(255)&"K";               ! Clear screen + home cursor
280     GRAPHICS OFF
290     ALPHA ON
300     CONTROL 1,12;1                  ! Key labels off
310     RESET 7
320     Test_number=0
330     Checkpoint=0
340     Ascii_data$=""
350     Inst_id$=""
360     Horiz_line$="********************************************************************************"
370     !Initialize test results array to "NOT PERFORMED"
380     FOR I=1 TO 17
390     Test_results$(I)="NOT PERFORMED"
400     NEXT I
410     PRINT " "
420     Title$="HP 5361A/B HP-IB OPERATIONAL VERIFICATION PROGRAM"
430     GOSUB Sub_title
440     PRINT Horiz_line$
450     PRINT "The HP-IB address of the printer is assumed to be 701. Would"
460     PRINT "you like to change that?"
470     PRINT
480     PRINT "CAUTION! Do not set printer address the same as the counter's address."
490     GOSUB Clear_keys
500     ON KEY 1 LABEL "YES" GOTO Change_add
510     ON KEY 6 LABEL "    " GOTO Change_add
520     ON KEY 4 LABEL " NO" GOTO Same_add
530     ON KEY 9 LABEL "    " GOTO Same_add
540     GOSUB Wait_for_key
550     Same_add:                               ! ASSUME PRINTER ADDRESS TO BE 701
560     Ptr_add=701
570     GOTO Start_program
580     Change_add:                             ! CHANGE THE ADDRESS OF THE PRINTER FROM 701
590     CONTROL 1,12;1
600     INPUT "PLEASE ENTER THE CORRECT ADDRESS OF THE PRINTER.",Ptr_add
```

```
610     IF (Ptr_add<(700) OR Ptr_add>(731) OR Ptr_add=(721)) THEN GOTO Bad_add
620     Start_program:!
630     OUTPUT KBD;CHR$(255)&"K";
640     Title$="HP 5361A/B HP-IB OPERATIONAL VERIFICATION PROGRAM"
650     GOSUB Sub_title
660     PRINT Horiz_line$
670     PRINT
680     GOSUB Menu
690     IF VAL(SYSTEM$("PRINTER IS"))=Ptr_add THEN GOTO Already_printed     ! ***** 701
700     PRINT
710     PRINT "Would you like a hardcopy of the checkpoint summary?"
720     PRINT
730     PRINT "YES - Press K1 to receive a hardcopy, or"
740     PRINT "NO - Press K4 to continue."
750     GOSUB Clear_keys
760     ON KEY 1 LABEL "YES" GOTO Printer_setup
770     ON KEY 6 LABEL " " GOTO Printer_setup
780     ON KEY 4 LABEL "NO" GOTO Already_printed
790     ON KEY 9 LABEL " " GOTO Already_printed
800     GOSUB Wait_for_key
810     Printer_setup:                                  ! Yes, printout
820     GOSUB Keys_off
830     OUTPUT KBD;CHR$(255)&"K";
840     PRINTER IS Ptr_add
850     ON ERROR GOTO Bad_add
860     ON TIMEOUT Ptr_add DIV 100,1 GOTO Prnt_broke
870     OUTPUT Ptr_add USING "#,K";" "                  !TEST FOR A RESPONSE
880     OFF TIMEOUT
890     OFF ERROR
900     GOSUB Menu
910     GOTO Already_printed
920     Bad_add:                                        !
930     DISP Ptr_add;"IS INVALID. TRY AGAIN."
940     BEEP 600,.3
950     WAIT 2
960     OFF ERROR
970     OFF TIMEOUT
980     GOTO Change_add
990     Prnt_broke:                                     !
1000    CONTROL 1,12;1 !key labels off
1010    DISP (Ptr_add);"NOT RESPONDING. CHECK PRINTER IS ON, & ADDRESS & HOOKUP IS CORRECT."
1020    BEEP 600,.3
1030    WAIT 3
1040    GOTO Initialize
1050    PRINTER IS CRT
1060    Already_printed:                                !
1070    GOSUB Keys_off
1080    PRINTER IS CRT
1090    OUTPUT KBD;CHR$(255)&"K";
1100    Title$="MAKE THE CONNECTIONS"
1110    GOSUB Sub_title
1120    PRINT Horiz_line$
1130    PRINT
1140    PRINT "Connect the HP-IB Interface to the rear panel of the counter and turn on the"
1150    PRINT "power. A source capable of outputting 1GHz from -10 to +20 dBm will also be"
1160    PRINT "needed later to complete this verification. For pulse testing, set-up the"
1170    PRINT "test equipment as outlined in the manual."
1180    PRINT
1190    PRINT "Consult the counter Operating and Service manual for additional information."
1200    GOSUB Ready_start
1210    !
1220    GOSUB Begin_search
```

```
1230    GOTO First_check
1240    !*****************************************************************
1250    !               START OF CHECKPOINT TESTS
1260    !*****************************************************************
1270    !
1280    Chk1:                                   !
1290    Test_number=1
1300    Title$="'REMOTE', 'LOCAL LOCKOUT', AND 'LOCAL'"
1310    GOSUB Print_title
1320    PRINT "Checkpoint 1 tests the REMOTE, LOCAL LOCKOUT, and LOCAL HP-IB commands."
1330    PRINT "Each command will be programmed and the operator will be prompted as to"
1340    PRINT "what conditions should be verified."
1350    PRINT
1360    GOSUB Ready_start
1370    !
1380    LOCAL Address
1390    REMOTE Address
1400    OUTPUT Address;"INIT"
1410    PRINT
1420    Title$="REMOTE"
1430    GOSUB Sub_title
1440    PRINT
1450    PRINT "Verify that the INT, REM, LSN, FM NORM, and AUTO annunciators are on."
1460    PRINT
1470    GOSUB Ready_start
1480    PRINT
1490    Title$="LOCAL LOCKOUT"
1500    GOSUB Sub_title
1510    PRINT
1520    PRINT "Verify that pressing any of the front panel keys other than POWER will"
1530    PRINT "not affect the ";Inst_id$;"."
1540    PRINT
1550    LOCAL LOCKOUT 7
1560    GOSUB Ready_start
1570    PRINT
1580    Title$="LOCAL"
1590    GOSUB Sub_title
1600    PRINT
1610    PRINT "Verify that the REM annunciator is no longer on, and the ";Inst_id$
1620    PRINT "responds to front panel entries."
1630    LOCAL 7
1640    PRINT
1650    GOSUB Ready_start
1660    REMOTE Address
1670    GOTO Record_results
1680    ! End of Chk1
1690    !
1700    Chk2:                                   !
1710    Test_number=2
1720    Title$="SELF CHECK ('TEST?')"
1730    GOSUB Print_title
1740    PRINT "Checkpoint 2 tests the 'TEST?' HP-IB command. The results of the SELF CHECK"
1750    PRINT "will be sent over the bus and displayed on the controller CRT."
1760    PRINT
1770    GOSUB Ready_start
1780    REMOTE Address
1790    OUTPUT Address;"INIT"
1800    OUTPUT Address;"TEST?"
1810    ENTER Address;Ascii_data$
1820    PRINT "The results of SELF CHECK are: ";TRIM$(Ascii_data$)
1830    PRINT
1840    IF Ascii_data$[1,4]="PASS" THEN GOTO Pass_test1
```

```
1850   PRINT "The ";Inst_id$;" failed the SELF CHECK. It is recommended that the fault on"
1860   PRINT "the ";TRIM$(Ascii_data$[18,19]);" or associated assemblies be corrected"
1870   PRINT "before continuing with the HP-IB verification."
1880   PRINT
1890   Pass_test1:                                    !
1900   GOTO Record_results
1910   ! End of Chk2
1920   !
1930   Chk3:!
1940   Test_number=3
1950   Title$="'DISPLAY'"
1960   GOSUB Print_title
1970   PRINT "Checkpoint 3 tests the 'DISPLAY' HP-IB command."
1980   PRINT
1990   GOSUB Ready_start
2000   OUTPUT Address;"INIT"
2010   OUTPUT Address;"DISPLAY, 'HP-IBVERIFICATION'"
2020   PRINT "Verify that the ";Inst_id$;" display shows 'HP-IB VERIFICATION'."
2030   PRINT
2040   GOSUB Ready_start
2050   OUTPUT Address;"DISPLAY,''"
2060   GOTO Record_results
2070   ! End of Chk3
2080   !
2090   Chk4:!
2100   Test_number=4
2110   Title$="'INIT' and 'RESET'"
2120   GOSUB Print_title
2130   PRINT "Checkpoint 4 tests the 'INIT' and 'RESET' HP-IB commands."
2140   PRINT
2150   GOSUB Ready_start
2160   OUTPUT Address;"INIT"
2170   ! SET UP INSTRUMENT STATE TO BE INITIALIZED
2180   OUTPUT Address;"OFFSET,ON;SCALE,ON;SMOOTH,ON"
2190   REMOTE Address
2200   OUTPUT Address;"INIT"
2210   Title$="'INIT'"
2220   GOSUB Sub_title
2230   PRINT
2240   PRINT "Verify that the INT, REM, LSN, FM NORM and AUTO annunicators are"
2250   PRINT "on that the display shows: 00 000 000 000 CW without an input."
2260   PRINT
2270   GOSUB Ready_start
2280   !SET UP ERROR CONDITION - MANUAL FREQ 9E+99 IS OUT OF RANGE
2290   OUTPUT Address;"MANUAL,9E+99"
2300   Title$="'RESET'"
2310   GOSUB Sub_title
2320   PRINT
2330   PRINT "Verify that the ";Inst_id$[1,7];" shows: OUT OF RANGE 3 ERROR ."
2340   PRINT
2350   PRINT "Press ENTER to send the 'RESET' command. Verify that the error message is"
2360   PRINT "cleared and the INT, REM, LSN, FM NORM and AUTO annunciators are on."
2370   GOSUB Ready_start
2380   OUTPUT Address;"RESET"
2390   PRINT
2400   GOTO Record_results
2410   ! End of Chk4
2420   !
2430   Chk5:!
2440   Test_number=5
2450   Title$="'OVEN?' and 'REF?'"
2460   GOSUB Print_title
```

```
2470    PRINT "Checkpoint 5 tests the 'OVEN?' and 'REF?' HP-IB commands."
2480    PRINT
2490    GOSUB Ready_start
2500    Title$="'REF?'"
2510    GOSUB Sub_title
2520    PRINT
2530    PRINT "Disconnect the external reference if one is connected."
2540    PRINT
2550    GOSUB Ready_start
2560    REMOTE Address
2570    OUTPUT Address;"INIT"
2580    OUTPUT Address;"REF?"
2590    ENTER Address;Ascii_data$ ! Enter the status of the reference
2600    PRINT
2610    PRINT "Verify that the EXT REF annunciator is off."
2620    PRINT
2630    GOSUB Ready_start
2640    PRINT
2650    PRINT "The ";Inst_id$;" has returned its timebase reference status as ";
2660    PRINT TRIM$(Ascii_data$);"ERNAL."
2670    PRINT
2680    IF Ascii_data$="INT" THEN GOTO Okay1
2690    PRINT "RETURNED HP-IB DATA INCORRECT";CHR$(7)
2700    PRINT
2710    Okay1:!
2720    GOSUB Ready_start
2730    Title$="'REF?'"
2740    GOSUB Sub_title
2750    PRINT
2760    PRINT "Connect an external timebase to the external reference on the rear panel."
2770    PRINT
2780    GOSUB Ready_start
2790    OUTPUT Address;"REF?"
2800    ENTER Address;Ascii_data$
2810    PRINT
2820    PRINT "Verify that the EXT REF annunciator is on. The ";Inst_id$;" has returned"
2830    PRINT "a reference status of ";TRIM$(Ascii_data$);"ERNAL."
2840    PRINT
2850    IF TRIM$(Ascii_data$)="EXT" THEN GOTO Okay2
2860    PRINT "RETURNED HP-IB DATA INCORRECT"
2870    Okay2:!
2880    GOSUB Ready_start
2890    OUTPUT KBD;CHR$(255)&"K";
2900    Title$="'OVEN?'"
2910    GOSUB Sub_title
2920    PRINT
2930    PRINT "Disconnect the external timebase. If the ";Inst_id$;" has Option 001 or"
2940    PRINT "010 (ovenized oscillators), the returned status is meaningful. If the"
2950    PRINT "counter does not have these options, the returned status will always"
2960    PRINT "be 'WARM'."
2970    PRINT
2980    GOSUB Ready_start
2990    OUTPUT Address;"OVEN?"
3000    ENTER Address;Ascii_data$
3010    PRINT
3020    PRINT "The oven status is ";Ascii_data$;"."
3030    PRINT
3040    GOTO Record_results
3050    ! End of Chk5
3060    !
3070    Chk6:!
3080    Test_number=6
```

```
3090    Title$="'ERR?'"
3100    GOSUB Print_title
3110    OUTPUT Address;"INIT"
3120    PRINT "Checkpoint 6 tests the 'ERR?' HP-IB command. An error state will be"
3130    PRINT "programmed and the type of error will read back to the controller."
3140    PRINT
3150    GOSUB Ready_start
3160    OUTPUT Address;"MANUAL,9E99" ! Out of range, error guaranteed
3170    OUTPUT Address;"ERR?"
3180    ENTER Address;Ascii_data$
3190    PRINT "Verify that the ";Inst_id$;" displays OUT OF RANGE 3 ERROR."
3200    PRINT
3210    IF Ascii_data$[18,18]="3" THEN GOTO Okay3
3220    PRINT "RETURNED HP-IB DATA INCORRECT."
3230    PRINT
3240    Okay3:!
3250    PRINT "Press ENTER to RESET the ";Inst_id$;"."
3260    GOSUB Ready_start
3270    OUTPUT Address;"RESET"
3280    GOTO Record_results
3290    ! End of Chk6
3300    !
3310    Chk7:!
3320    Test_number=7
3330    Title$="'SET' and 'SET?'"
3340    GOSUB Print_title
3350    PRINT "Checkpoint 7 tests the 'SET' and 'SET?' HP-IB commands. A configuration"
3360    PRINT "will be programmed and then saved using the 'SET?' command. The ";
3370    PRINT Inst_id$
3380    PRINT "will be set to the initial power-on condition and then reprogrammed"
3390    PRINT "using the 'SET' command."
3400    PRINT
3410    GOSUB Ready_start
3420    REMOTE Address
3430    OUTPUT Address;"INIT"
3440    OUTPUT Address;"SMOOTH,ON;SCALE,1,ON;FMRATE,LOW" ! Test setup
3450    PRINT "The front panel set-up to be stored has the SCALE, SMOOTH, INT, REM, LSN,"
3460    PRINT "FM LOW, and AUTO annunciators on."
3470    PRINT
3480    PRINT "Verify these annunciators."
3490    GOSUB Ready_start
3500    OUTPUT Address;"SET?"
3510    ! STORE THE SET-UP IN SETUP$
3520    ENTER Address;Setup$
3530    OUTPUT Address;"INIT"
3540    PRINT
3550    PRINT
3560    PRINT "This configuration is now stored and the ";Inst_id$;" is initialized."
3570    PRINT
3580    PRINT
3590    PRINT "Verify that the INT, REM, LSN, FM NORM, and AUTO annunciators are on."
3600    PRINT
3610    GOSUB Ready_start
3620    OUTPUT Address;"SET,'";Setup$;"'"
3630    PRINT "Verify that the SCALE, SMOOTH, INT, REM, LSN, FM LOW, and AUTO annunciators"
3640    PRINT "are on again."
3650    PRINT
3660    GOSUB Ready_start
3670    GOTO Record_results
3680    ! End of Chk7
3690    !
3700    Chk8:!
```

```
3710   Test_number=8
3720   Title$="'LOWZ' and 'HIGHZ'"
3730   GOSUB Print_title
3740   PRINT "Checkpoint 8 tests the 'LOWZ'and 'HIGHZ' HP-IB commands. Connect the"
3750   PRINT "rear panel 10   MHz OUT to Input 2 of the ";Inst_id$;"."
3760   PRINT
3770   GOSUB Ready_start
3780   REMOTE Address
3790   OUTPUT Address;"INIT"
3800   OUTPUT Address;"LOWZ"
3810   ENTER Address;Meas_data
3820   OUTPUT KBD;CHR$(255)&"K";
3830   Title$="'LOWZ'"
3840   GOSUB Sub_title
3850   PRINT
3860   PRINT "Verify that the 50 ohm annunciator is on as well as the INT, REM and TLK"
3870   PRINT "annunciators. The OPEN annunciator should be flashing. The display should"
3880   PRINT "read: 10 000 000 CW IN2"
3890   PRINT
3900   IF Meas_data=10000000 THEN GOTO Okay4
3910   PRINT "RETURNED HP-IB DATA INCORRECT: ";Meas_data
3920   Okay4:!
3930   PRINT
3940   GOSUB Ready_start
3950   OUTPUT Address;"HIGHZ"
3960   ENTER Address;Meas_data
3970   OUTPUT KBD;CHR$(255)&"K";
3980   Title$="'HIGHZ'"
3990   GOSUB Sub_title
4000   PRINT
4010   PRINT "Verify that the INT, REM, TLK, and 1 Mohm annunciators are on. The OPEN"
4020   PRINT "annunciator should be flashing. The display should read: 10 000 000 CW IN2"
4030   PRINT
4040   IF Meas_data=10000000 THEN GOTO Okay5
4050   PRINT "RETURNED HP-IB DATA INCORRECT: ";Meas_data
4060   PRINT
4070   Okay5:!
4080   GOTO Record_results
4090   ! End of Chk8
4100   !
4110   Chk9:!
4120   Test_number=9
4130   Title$="'SAMPLE and TRIGGER'"
4140   GOSUB Print_title
4150   PRINT "Checkpoint 9 tests the 'SAMPLE' and 'TRIGGER' HP-IB commands. Connect the"
4160   PRINT "rear panel 10   MHz OUT to Input 2 of the ";Inst_id$;"."
4170   PRINT
4180   GOSUB Ready_start
4190   OUTPUT Address;"INIT"
4200   OUTPUT Address;"SAMPLE,HOLD;HIGHZ"
4210   PRINT "Verify that the INT, HOLD, REM, LSN, and 1Mohm annunciators are on. The display"
4220   PRINT "should read: HOLDING- - -"
4230   PRINT
4240   INPUT "Press ENTER to trigger the counter and take a measurement.",Dummy$
4250   OUTPUT Address;"TRIGGER"
4260   ENTER Address;Meas_data
4270   OUTPUT KBD;CHR$(255)&"K";
4280   PRINT "The measurement should be: 10 000 000 CW IN2"
4290   PRINT
4300   IF Meas_data=10000000 THEN GOTO Okay6
4310   PRINT "RETURNED HP-IB DATA INCORECT: ";Meas_data
4320   PRINT
```

```
4330    Okay6:!
4340    GOTO Record_results
4350    ! End of Chk9
4360    !
4370    Chk10:!
4380    Test_number=10
4390    Title$="'RESOL' and 'HIRESOL'"
4400    GOSUB Print_title
4410    PRINT "Checkpoint 10 tests the 'RESOL'and 'HIRESOL' HP-IB commands. Connect the"
4420    PRINT "rear panel 10 MHz OUT to Input 2 of the ";Inst_id$;"."
4430    PRINT
4440    GOSUB Ready_start
4450    OUTPUT Address;"INIT"
4460    OUTPUT Address;"HIGHZ;RESOL,6" ! 1 MHz resolution
4470    Title$="'RESOL'"
4480    GOSUB Sub_title
4490    PRINT
4500    PRINT "Verify that the current reading is to 1MHz resolution. Press ENTER"
4510    PRINT " to program another decade of resolution."
4520    PRINT
4530    PRINT "Continue pressing ENTER until the counter displays the measurement with"
4540    PRINT "1Hz resolution."
4550    PRINT
4560    FOR I=5 TO 0 STEP -1
4570    DISP "Press ENTER to decrease the resolution to ";
4580    DISP INT(10^(I));"Hz."
4590    INPUT "",Dummy$
4600    OUTPUT Address;"RESOL,";I
4610    DISP
4620    NEXT I
4630    OUTPUT KBD;CHR$(255)&"K";
4640    OUTPUT Address;"HIRESOL,ON"
4650    PRINT "Verify that the INT, REM, LSN, 1Mohm, and HIGH RESOL INDICATORS (**) are on,"
4660    PRINT "the OPEN annunciator is flashing, and the display reads: 10 000 000. 0** IN2"
4670    PRINT
4680    GOTO Record_results
4690    ! End of Chk10
4700    !
4710    Chk11:!
4720    Test_number=11
4730    Title$="'OFFSET', 'SCALE', and 'SMOOTH'"
4740    GOSUB Print_title
4750    PRINT "Checkpoint 11 tests the 'OFFSET', 'SCALE', and 'SMOOTH' HP-IB commands."
4760    PRINT "Connect the rear panel 10      MHz OUT to Input 2 of the ";Inst_id$;"."
4770    PRINT
4780    GOSUB Ready_start
4790    REMOTE Address
4800    OUTPUT Address;"INIT"
4810    OUTPUT Address;"HIGHZ;OFFSET,-5E6,ON" ! Should be 5MHz
4820    Title$="'OFFSET'"
4830    GOSUB Sub_title
4840    PRINT
4850    PRINT "Verify that the OFFSET, INT, REM, TLK, and 1Mohm annunciators are on. The"
4860    PRINT "OPEN light should be flashing. The display should read: 5 000 000 CW IN2"
4870    ENTER Address;Meas_data
4880    IF Meas_data=5000000 THEN GOTO Okay7
4890    PRINT
4900    PRINT "RETURNED HP-IB DATA IS INCORRECT: ";Meas_data
4910    Okay7:!
4920    PRINT
4930    GOSUB Ready_start
4940    OUTPUT Address;"OFFSET,OFF;SCALE,2,ON" ! Should be 20MHz
```

```
4950    Title$="'SCALE'"
4960    GOSUB Sub_title
4970    PRINT
4980    PRINT "Verify that the SCALE, INT, REM, TLK, and 1Mohm annunciators are on. The"
4990    PRINT "OPEN light should be flashing. The display should read: 20 000 000 CW IN2"
5000    ENTER Address;Meas_data
5010    IF Meas_data=20000000 THEN GOTO Okay8
5020    PRINT
5030    PRINT "RETURNED HP-IB DATA INCORRECT: ";Meas_data
5040    Okay8:!
5050    PRINT
5060    GOSUB Ready_start
5070    OUTPUT KBD;CHR$(255)&"K";
5080    Title$="'SMOOTH'"
5090    GOSUB Sub_title
5100    PRINT
5110    PRINT "After pressing ENTER to program the counter, verify that the SMOOTH, INT, REM,"
5120    PRINT "LSN, and 1Mohm annunciators are on. The OPEN annunciator should be flashing."
5130    PRINT "The display should initially show 10 000 and increase the resolution to"
5140    PRINT "1Hz."
5150    PRINT
5160    GOSUB Ready_start
5170    OUTPUT Address;"SMOOTH,ON;HIGHZ;SCALE,OFF"
5180    GOSUB Ready_start
5190    OUTPUT Address;"SMOOTH,OFF"
5200    GOTO Record_results
5210    ! End of Chk11
5220    !
5230    Chk12:!
5240    Test_number=12
5250    Title$="'AUTO' and 'MANUAL'"
5260    GOSUB Print_title
5270    PRINT "Checkpoint 12 tests the 'AUTO'and 'MANUAL' HP-IB commands. Input a 1GHz"
5280    PRINT "signal at -5 dBm to Input 1 of the ";Inst_id$;"."
5290    PRINT
5300    GOSUB Ready_start
5310    REMOTE Address
5320    OUTPUT Address;"INIT"
5330    OUTPUT Address;"SAMPLE,HOLD;TRIGGER" ! Auto mode, single measurement
5340    ENTER Address;Meas_data
5350    IF Meas_data=1.E+38 THEN GOTO Fail
5360    OUTPUT KBD;CHR$(255)&"K";
5370    Title$="'AUTO'"
5380    GOSUB Sub_title
5390    PRINT
5400    PRINT "Verify that the INT, HOLD, REM, TLK, FM NORM, and AUTO annunciators are on"
5410    PRINT "and the ";Inst_id$;" is displaying ";Meas_data;" Hz."
5420    PRINT
5430    PRINT "If the ";Inst_id$;" display does not match the above reading, then an"
5440    PRINT "error occurred in the HP-IB transfer."
5450    PRINT
5460    GOSUB Ready_start
5470    OUTPUT KBD;CHR$(255)&"K";
5480    Title$="'MANUAL'"
5490    GOSUB Sub_title
5500    PRINT
5510    PRINT "This will trigger the ";Inst_id$;"."
5520    GOSUB Ready_start
5530    OUTPUT Address;"MANUAL,LASTF"
5540    OUTPUT Address;"SAMPLE,HOLD;TRIGGER"
5550    ENTER Address;Meas_data
5560    IF Meas_data1=1.E+38 THEN GOTO Fail
```

```
5570    OUTPUT KBD;CHR$(255)&"K";
5580    Title$="'MANUAL'"
5590    GOSUB Sub_title
5600    PRINT
5610    PRINT "Verify that the INT, HOLD, REM, TLK, and MAN annunciators are on"
5620    PRINT "and the ";Inst_id$;" is displaying ";Meas_data;" Hz."
5630    PRINT
5640    PRINT "If the ";Inst_id$;" display does not match the above reading, then an"
5650    PRINT "error occurred in the HP-IB transfer."
5660    PRINT
5670    GOTO Record_results
5680    Fail:!
5690    PRINT
5700    PRINT Inst_id$;" failed to acquire a"
5710    PRINT "signal."
5720    PRINT
5730    GOSUB Ready_start
5740    PRINT
5750    GOTO Record_results
5760    ! End of Chk12
5770    !
5780    Chk13:!
5790    Test_number=13
5800    Title$="'FMRATE'"
5810    GOSUB Print_title
5820    REMOTE Address
5830    OUTPUT Address;"INIT"
5840    PRINT "Checkpoint 13 tests the 'FMRATE' HP-IB command."
5850    PRINT
5860    PRINT "Input a 1 GHz signal at -5 dBm to Input 1 of the ";Inst_id$;"."
5870    PRINT
5880    GOSUB Ready_start
5890    OUTPUT Address;"AUTO;FMRATE,NORMAL"
5900    OUTPUT KBD;CHR$(255)&"K";
5910    Title$="'FMRATE', NORMAL"
5920    GOSUB Sub_title
5930    PRINT
5940    PRINT "Verify that the INT, REM, LSN, FM NORM, and AUTO annunciators are on. The OPEN"
5950    PRINT "annunciator should be flashing."
5960    PRINT
5970    GOSUB Ready_start
5980    OUTPUT Address;"FMRATE,LOW"
5990    OUTPUT KBD;CHR$(255)&"K";
6000    Title$="'FMRATE', LOW"
6010    GOSUB Sub_title
6020    PRINT
6030    PRINT "Verify that the INT, REM, LSN, FM LOW, and AUTO annunciators are on. The OPEN"
6040    PRINT "annunciator should be flashing."
6050    PRINT
6060    GOTO Record_results
6070    ! End of Chk13
6080    !
6090    Chk14:!
6100    Test_number=14
6110    Title$="'SRQMASK'"
6120    GOSUB Print_title
6130    OUTPUT Address;"INIT"
6140    REMOTE Address
6150    PRINT "Checkpoint 14 tests the 'SRQMASK' HP-IB command."
6160    PRINT
6170    PRINT "Set the signal source to output a 1 GHz signal at a level of 0 dBM"
6180    GOSUB Ready_start
```

```
6190    OUTPUT KBD;CHR$(255)&"K";
6200    Title$="MEASUREMENT COMPLETE bit"
6210    GOSUB Sub_title
6220    PRINT
6230    PRINT "This section tests the MEASUREMENT COMPLETE bit of the status byte of"
6240    PRINT "the ";Inst_id$;"."
6250    PRINT
6260    OUTPUT Address;"INIT"
6270    OUTPUT Address;"SAMPLE,HOLD;SRQMASK,2"
6280    GOSUB Ready_start
6290    ON INTR 7 GOTO Meas_intr
6300    ENABLE INTR 7;2
6310    OUTPUT Address;"TRIGGER"
6320    WAIT 2
6330    OFF INTR 7
6340    Fail_measure:!
6350    PRINT Inst_id$;" FAILED the MEASUREMENT COMPLETE bit test."
6360    GOTO Meas_done
6370    Meas_intr:!
6380    OFF INTR 7
6390    STATUS 7,1;B
6400    S=SPOLL(Address)
6410    PRINT "THE SPOLL IS ";S
6420    IF BIT(S,1) THEN GOTO Pass_measure
6430    GOTO Fail_measure
6440    Pass_measure:!
6450    PRINT Inst_id$;" PASSED the MEASUREMENT COMPLETE bit test."
6460    Meas_done:!
6470    PRINT
6480    GOSUB Ready_start
6490    OUTPUT KBD;CHR$(255)&"K";
6500    Title$="LOCAL bit"
6510    GOSUB Sub_title
6520    PRINT
6530    PRINT "This section tests the LOCAL bit of the status bytes of the ";Inst_id$;"."
6540    PRINT
6550    OUTPUT Address;"SRQMASK,16"
6560    GOSUB Ready_start
6570    ON INTR 7 GOTO Srq_intr
6580    ENABLE INTR 7;2
6590    LOCAL Address! SHOULD SET LCL BIT
6600    WAIT 1
6610    OFF INTR 7
6620    Fail_local:!
6630    PRINT Inst_id$;" FAILED the LOCAL bit test."
6640    GOTO Done_srq
6650    Srq_intr:!
6660    OFF INTR 7
6670    STATUS 7,1;B
6680    S=SPOLL(Address)
6690    PRINT "THE SPOLL IS ";S
6700    IF BIT(S,4) THEN GOTO Pass_local
6710    GOTO Fail_local
6720    Pass_local:!
6730    PRINT Inst_id$;" PASSED the LOCAL bit test."
6740    Done_srq:!
6750    PRINT
6760    GOSUB Ready_start
6770    OUTPUT KBD;CHR$(255)&"K";
6780    Title$="ERROR bit"
6790    GOSUB Sub_title
6800    PRINT
```

```
6810    PRINT "This section tests the ERROR bit of the status byte of the ";Inst_id$;"."
6820    PRINT
6830    OUTPUT Address;"SRQMASK,4"
6840    GOSUB Ready_start
6850    ON INTR 7 GOTO Error_intr
6860    ENABLE INTR 7;2
6870    OUTPUT Address;"MANUAL,9E+99" ! Error condition
6880    WAIT 1
6890    OFF INTR 7
6900    Fail_error:!
6910    PRINT Inst_id$;" FAILED the ERROR bit test."
6920    GOTO Done_error
6930    Error_intr:!
6940    OFF INTR 7
6950    STATUS 7,1;B
6960    S=SPOLL(Address)
6970    PRINT "THE SPOLL IS ";S
6980    IF BIT(S,2) THEN GOTO Pass_error
6990    GOTO Fail_error
7000    Pass_error:!
7010    PRINT Inst_id$;" PASSED the ERROR bit test."
7020    Done_error:!
7030    OUTPUT Address;"RESET"
7040    PRINT
7050    GOSUB Ready_start
7060    OUTPUT KBD;CHR$(255)&"K";
7070    Title$="OUTPUT DATA READY bit"
7080    GOSUB Sub_title
7090    PRINT
7100    PRINT "This section tests the OUTPUT DATA READY bit of the status byte of the"
7110    PRINT Inst_id$;"."
7120    PRINT
7130    OUTPUT Address;"SRQMASK,1"
7140    GOSUB Ready_start
7150    ON INTR 7 GOTO Ready_intr
7160    ENABLE INTR 7;2
7170    OUTPUT Address;"ID?"
7180    WAIT 1
7190    OFF INTR 7
7200    Fail_ready:!
7210    PRINT Inst_id$;" FAILED the OUTPUT DATA READY bit test."
7220    GOTO Done_ready
7230    Ready_intr:!
7240    PRINT
7250    OFF INTR 7
7260    STATUS 7,1;B
7270    S=SPOLL(Address)
7280    PRINT "THE SPOLL IS ";S
7290    ENTER Address;Setup$
7300    IF BIT(S,0) THEN GOTO Pass_ready
7310    GOTO Fail_ready
7320    Pass_ready:!
7330    PRINT Inst_id$;" PASSED the OUTPUT DATA READY bit test."
7340    Done_ready:!
7350    PRINT
7360    !OUTPUT Address;"SRQMASK,4"
7370    GOTO Record_results
7380    ! End of Chk14
7390    !
7400    Chk15:!
7410    Test_number=15
7420    Title$="'DUMP'"
```

```
7430    GOSUB Print_title
7440    REMOTE Address
7450    OUTPUT Address;"INIT"
7460    PRINT "Checkpoint 15 tests the 'DUMP' HP-IB command."
7470    PRINT
7480    Hookup:!
7490    PRINT "Connect a 1 GHz signal at -5 dBm to Input 1 of the ";Inst_id$;"."
7500    PRINT
7510    PRINT "Press ENTER to begin DUMPING data from the ";Inst_id$;" to the controller."
7520    PRINT "Ten measurements will be taken and displayed."
7530    PRINT
7540    GOSUB Ready_start
7550    REMOTE Address
7560    ENTER Address;Meas_data
7570    IF Meas_data=1.E+38 THEN GOTO Hookup
7580    OUTPUT Address;"MANUAL,LASTF;RESOL,4;DUMP,ON"
7590    PRINT "MEAS# DATA"
7600    FOR I=1 TO 10
7610    ENTER Address;Ascii_data
7620    WAIT .300
7630    PRINT I,Ascii_data,"*10       KHz"
7640    NEXT I
7650    PRINT
7660    OUTPUT Address;"DUMP,OFF"
7670    GOTO Record_results
7680    ! End of Chk15
7690    !
7700    Chk16:  !
7710    Test_number=16
7720    Title$="PULSE MEASUREMENT"
7730    GOSUB Print_title
7740    PRINT "BEFORE TESTING CHK 16, BE SURE TO MAKE ALL SET-UP AND CONNECTIONS AS
        OUTLINED IN THE MANUAL."
7750    OUTPUT Address;"FREQ"
7760    REMOTE Address
7770    PRINT
7780    PRINT
7790    PRINT "CHECKPOINT 16 TESTS THE 'PULSE FREQUENCY' HP-IB COMMAND."
7800    PRINT
7810    GOSUB Ready_start
7820    ENTER Address;Meas_data
7830    Title$="PULSE FREQUENCY"
7840    GOSUB Sub_title
7850    PRINT
7860    PRINT "VERIFY THE COUNTER DISPLAYS APPROX 1 GHZ PULSE"
7870    PRINT
7880    PRINT
7890    GOSUB Ready_start
7900    Title$="PULSE WIDTH MEASUREMENT"
7910    GOSUB Print_title
7920    OUTPUT Address;"PWID"
7930    OUTPUT Address;"AVER,100"
7940    REMOTE Address
7950    PRINT "CHECKPOINT 16 TESTS THE 'PULSE WIDTH' HP-IB COMMAND."
7960    PRINT
7970    GOSUB Ready_start
7980    ENTER Address;Meas_data
7990    Title$="PULSE WIDTH"
8000    GOSUB Sub_title
8010    PRINT
8020    PRINT "VERIFY THE COUNTER DISPLAYS APPROX .100 MICRO SEC PW"
8030    PRINT
```

```
8040   GOSUB Ready_start
8050   Title$="P OFFT MEASUREMENT"
8060   GOSUB Print_title
8070   OUTPUT Address;"OFFT"
8080   OUTPUT Address;"AVER,100"
8090   REMOTE Address
8100   PRINT "CHECKPOINT 16 TESTS THE 'OFFT' HP-IB COMMAND"
8110   PRINT
8120   GOSUB Ready_start
8130   ENTER Address;Meas_data
8140   Title$="P OFFT TIME"
8150   GOSUB Sub_title
8160   PRINT
8170   PRINT "VERIFY THE COUNTER DISPLAYS APPROX .500 MICRO SEC OFF"
8180   PRINT
8190   GOSUB Ready_start
8200   Title$="PRI MEASUREMENT"
8210   GOSUB Print_title
8220   OUTPUT Address;"PRI"
8230   OUTPUT Address;"AVER,100"
8240   REMOTE Address
8250   PRINT "CHECKPOINT 16 TESTS THE 'PRI MEASUREMENT' HP-IB COMMAND"
8260   PRINT
8270   GOSUB Ready_start
8280   ENTER Address;Meas_data
8290   Title$="PULSE REP INTERVAL"
8300   GOSUB Sub_title
8310   PRINT
8320   PRINT "VERIFY THE COUNTER DISPLAYS APPROX .600 MICRO SEC PRI"
8330   PRINT
8340   GOSUB Ready_start
8350   Title$="PULSE REP FREQUENCY"
8360   GOSUB Print_title
8370   OUTPUT Address;"PRF"
8380   OUTPUT Address;"AVER,100"
8390   REMOTE Address
8400   PRINT "CHECKPOINT 16 TESTS THE 'PRF' HP-IB COMMAND"
8410   PRINT
8420   GOSUB Ready_start
8430   ENTER Address;Meas_data
8440   Title$="PULSE REP FREQUENCY"
8450   GOSUB Sub_title
8460   PRINT
8470   PRINT "VERIFY THE COUNTER DISPLAYS APPROX 1663781 PRF"
8480   PRINT
8490   GOTO Record_results
8500   ! END OF CHK16
8510   Chk17:!
8520   Test_number=17
8530   Title$="CHECK ALL ADDRESSES"
8540   GOSUB Print_title
8550   REMOTE Address
8560   OUTPUT Address;"INIT"
8570   PRINT "Checkpoint 17 tests all of the valid HP-IB addresses except 21, which is"
8580   PRINT "the address of the controller."
8590   PRINT
8600   PRINT "TEST DESCRIPTION"
8610   PRINT
8620   PRINT "EACH ADDRESS TO BE TESTED IS MANUALLY SET ON REAR OF INSTRUMENT. PROGRAM WILL"
8630   PRINT "TEST IT WHEN TEST SOFTKEY IS PRESSED. THEN, NEXT ADDRESS IS SET ON INSTRUMENT,"
8640   PRINT "THE INCR SOFTKEY IS PRESSED TO INCREMENT PROGRAM TO NEXT ADDRESS, AND TEST"
8650   PRINT "IS DONE. A RUNNING TOTAL OF TESTS, PASSES, AND FAILS ARE LOGGED BY THE PROGRAM."
```

```
8660    PRINT
8670    GOSUB Ready_start
8680    Fail_counter=0! Reset fail counter
8690    Pass_counter=0! Reset pass counter
8700    FOR Address=700         TO 730
8710    IF Address=721 THEN GOTO Incr_address
8720    Re_test:        !
8730    OUTPUT KBD;CHR$(255)&"K";
8740    LOCAL 7
8750    PRINT
8760    PRINT "On the ";Inst_id$;", SET ADDRESS TO BE TESTED AT REAR PANEL DIP SWITCH,"
8770    PRINT
8780    PRINT "CYCLE POWER TO CAUSE INSTRUMENT TO RECOGNIZED ANY CHANGES MADE."
8790    PRINT
8800    PRINT "WAIT FOR INSTRUMENT TO FINISH POWER UP ROUTINE BEFOR TESTING."
8810    PRINT
8820    PRINT
8830    GOSUB Clear_keys
8840    ON KEY 1 LABEL "INCR" GOTO Incr_address
8850    ON KEY 6 LABEL " " GOTO Incr_address
8860    ON KEY 2 LABEL "EXIT" GOTO Exit_test1
8870    ON KEY 7 LABEL " " GOTO Exit_test1
8880    ON KEY 3 LABEL "TEST" GOTO Test_address
8890    ON KEY 8 LABEL " " GOTO Test_address
8900    PRINT "Press TEST to test current HP-IB address ";Address
8910    PRINT "Press INCR to skip to HP-IB address — ";
8920    IF Address=720 THEN
8930    PRINT Address+2
8940    ELSE
8950    IF Address<>730 THEN
8960    PRINT Address+1
8970    ELSE
8980    PRINT "NONE."
8990    END IF
9000    END IF
9010    PRINT
9020    PRINT
9030    PRINT "PRESS EXIT TO TERMINATE THIS CHECKPOINT."
9040    GOSUB Wait_for_key
9050    Test_address:!
9060    GOSUB Keys_off
9070    ON TIMEOUT 7,3 GOTO No_response
9080    REMOTE Address
9090    OUTPUT Address;"ID?"
9100    ENTER Address;Id_data$
9110    IF Id_data$=Inst_id$ THEN GOTO Incr_pass
9120    No_response:!
9130    OFF TIMEOUT 7
9140    PRINT
9150    Fail_counter=Fail_counter+1! Increment fail counter
9160    Fail_address(Fail_counter)=Address! Store passed address
9170    PRINT
9180    PRINT Inst_id$;" does not respond at address ";Address
9190    BEEP 250,.15
9200    WAIT .1
9210    BEEP 250,.15
9220    PRINT
9230    GOSUB Ready_start
9240    GOTO Re_test
9250    Incr_pass:!
9260    OFF TIMEOUT 7
9270    Pass_counter=Pass_counter+1! Increment pass ctr
```

```
9280    Pass_address(Pass_counter)=Address !Store pass address
9290    PRINT
9300    PRINT Inst_id$;" responds at address ";Address
9310    PRINT
9320    GOSUB Ready_start
9330    GOTO Re_test
9340    Incr_address:!
9350    GOSUB Keys_off
9360    ABORT 7
9370    CLEAR Address
9380    NEXT Address
9390    Exit_test1:!
9400    GOSUB Keys_off
9410    ABORT 7
9420    CLEAR Address
9430    IF Pass_counter=0 THEN GOTO No_pass_addr
9440    OUTPUT KBD;CHR$(255)&"K";
9450    PRINT "The ";Inst_id$;" responded at the following addresses:"
9460    FOR I=1 TO Pass_counter
9470    PRINT " ";Pass_address(I)
9480    NEXT I
9490    No_pass_addr:!
9500    IF Fail_counter=0 THEN GOTO No_address
9510    PRINT
9520    PRINT Inst_id$;" failed to respond at the following addresses:"
9530    PRINT
9540    FOR I=1 TO Fail_counter
9550    PRINT " ";Fail_address(I)
9560    NEXT I
9570    GOTO Finish_address
9580    No_address:!
9590    IF Pass_counter0 THEN GOTO Finish_address
9600    PRINT
9610    PRINT "No addresses were tested."
9620    Finish_address:!
9630    PRINT
9640    GOSUB Ready_start
9650    OFF TIMEOUT 7
9660    GOSUB Begin_search
9670    GOTO Record_results
9680    ! End of Chk17
9690    !
9700    !
9710    Final_exit: !
9720    PRINT "HP-IB VERIFICATION DONE"
9730    GOTO Exit_opver
9740    Error_exit: !
9750    PRINT ERRM$
9760    Exit_opver: !
9770    CONTROL 1,12;0
9780    RESET 7
9790    PRINTER IS CRT
9800    STOP    ! End of program
9810    !*************************************************************************
9820    !                          SUBROUTINES SECTION
9830    !*************************************************************************
9840    Begin_search:  ! SEARCH FOR 5361A/B ADDRESS
9850    OUTPUT KBD;CHR$(255)&"K";
9860    PRINT "SEARCHING FOR HP COUNTER AT ADDRESS";
9870    ON TIMEOUT 7,.4 GOTO Try_another
9880    FOR Address=700         TO 731
9890    IF Address=721 THEN GOTO Try_another! SKIP CONTROLLER
```

```
9900    IF Address=Ptr_add THEN GOTO Try_another! COUNTER ADDRESS SHOULD NOT BE EQUAL TO THE
        PRINTER ADDRESS
9910    OUTPUT CRT;Address;CHR$(8);CHR$(8);CHR$(8);CHR$(8);
9920    REMOTE Address
9930    OUTPUT Address;"ID?"
9940    ENTER Address;Inst_id$
9950    IF (Inst_id$="HP5361A" or Inst_id$="HP5361B") THEN GOTO Found_one
9960    Try_another: !
9970    ABORT 7
9980    CLEAR Address
9990    NEXT Address
10000   BEEP 550,.15
10010   WAIT .1
10020   BEEP 150,.15
10030   PRINT
10040   PRINT
10050   PRINT "NO COUNTER WAS FOUND ON THE HP-IB. CHECK ALL CONNECTIONS AND SWITCH SETTINGS."
10060   PRINT
10070   PRINT " BE SURE THAT THE ADDRESS OF THE PRINTER IS NOT THE SAME AS THE COUNTER."
10080   PRINT
10090   PRINT "RESTART PROGRAM"
10100   GOSUB Ready_start
10110   DISP Inst_id$
10120   GOTO Error_exit ! GOTO SKIP_PRINT ! TRY AGAIN
10130   Found_one:!
10140   PRINT
10150   PRINT
10160   PRINT Inst_id$;" FOUND AT ADDRESS ";VAL$(Address);"."
10170   BEEP 800,.03
10180   WAIT 3
10190   OFF TIMEOUT 7
10200   RETURN
10210   Record_results:!
10220   BEEP 800,.03
10230   INPUT "Press ENTER to record the results. ",Dummy$
10240   PRINT
10250   PRINT " Press the appropriate softkey to record the results of CHECKPOINT";
        Test_number;"."
10260   GOSUB Clear_keys
10270   ON KEY 1 LABEL " PASS" GOTO Pass_test
10280   ON KEY 6 LABEL " " GOTO Pass_test
10290   ON KEY 4 LABEL " FAIL" GOTO Fail_test
10300   ON KEY 9 LABEL " " GOTO Fail_test
10310   GOSUB Wait_for_key
10320   Pass_test:!
10330   GOSUB Keys_off
10340   Test_results$(Test_number)="PASS"
10350   GOTO Next_checkpt
10360   Fail_test:!
10370   GOSUB Keys_off
10380   Test_results$(Test_number)="FAIL"
10390   Next_checkpt:! Determine next checkpoint to be executed
10400   IF Test_number=18 THEN RETURN
10410   OUTPUT KBD;CHR$(255)&"K";
10420   PRINT "Current checkpoint: ";Test_number
10430   PRINT
10440   PRINT "Press the appropriate softkey to select the desired checkpoint..."
10450   PRINT
10460   PRINT "NEXT - Press K1 to perform the next checkpoint,"
10470   PRINT "EXIT - Press K2 to end the program,"
10480   PRINT "REPEAT - Press K3 to repeat this checkpoint, or"
10490   PRINT "GOTO# - Press K4 to select an arbitrary checkpoint."
```

```
10500   GOSUB Clear_keys
10510   ON KEY 1 LABEL " NEXT" GOTO Next_test
10520   ON KEY 6 LABEL " " GOTO Next_test
10530   ON KEY 2 LABEL " EXIT" GOTO Exit_test
10540   ON KEY 7 LABEL " " GOTO Exit_test
10550   ON KEY 3 LABEL " REPEAT" GOTO Repeat_test
10560   ON KEY 8 LABEL " " GOTO Repeat_test
10570   ON KEY 4 LABEL " GOTO #" GOTO Test_entry
10580   ON KEY 9 LABEL " " GOTO Test_entry
10590   GOSUB Wait_for_key
10600   First_check:! Determines the first checkpoint to execute
10610   OUTPUT KBD;CHR$(255)&"K";
10620   PRINT "Press the softkey to select the desired checkpoint."
10630   PRINT
10640   PRINT "FIRST - Press K1 to perform the first checkpoint,"
10650   PRINT "EXIT - Press K2 to end the program, or"
10660   PRINT "GOTO# - Press K4 to select an arbitrary checkpoint."
10670   GOSUB Clear_keys
10680   ON KEY 1 LABEL " FIRST" GOTO First_test
10690   ON KEY 6 LABEL " " GOTO First_test
10700   ON KEY 2 LABEL " EXIT" GOTO Exit_test
10710   ON KEY 7 LABEL " " GOTO Exit_test
10720   ON KEY 4 LABEL " GOTO #" GOTO Test_entry
10730   ON KEY 9 LABEL " " GOTO Test_entry
10740   GOSUB Wait_for_key
10750   Key_trap:!
10760   DISP "Wrong key pressed. Try again.";CHR$(7)
10770   RETURN
10780   Wait_for_key:!
10790   CONTROL 1,12;0
10800   DISP
10810   Loop:GOTO Loop
10820   Keys_off:!
10830   CONTROL 1,12;1
10840   RETURN
10850   Ready_start:!
10860   BEEP 800,.03
10870   INPUT "Press ENTER to continue. ",Dummy$
10880   RETURN
10890   Print_title:! Display checkpoint title
10900   OUTPUT KBD;CHR$(255)&"K";
10910   PRINT
10920   PRINT TAB(34);"CHECKPOINT";Test_number
10930   GOSUB Sub_title
10940   PRINT Horiz_line$
10950   BEEP 800,.03
10960   INPUT "Press ENTER to start the test.",Dummy$
10970   OUTPUT KBD;CHR$(255)&"K";
10980   RETURN
10990   Sub_title:!
11000   PRINT
11010   PRINT
11020   PRINT
11030   PRINT
11040   PRINT TAB(INT((80-(LEN(TRIM$(Title$))))/2));Title$
11050   RETURN
11060   First_test:!
11070   GOSUB Keys_off
11080   Checkpoint=1
11090   GOTO Branch_checkpt
11100   Next_test:!
11110   GOSUB Keys_off
```

```
11120  Checkpoint=Test_number+1
11130  GOTO Branch_checkpt
11140  Exit_test:!
11150  Checkpoint=0
11160  GOTO Branch_checkpt
11170  Repeat_test:!
11180  GOSUB Keys_off
11190  Checkpoint=Test_number
11200  GOTO Branch_checkpt
11210  Test_entry:!
11220  GOSUB Keys_off
11230  OUTPUT KBD;CHR$(255)&"K";
11240  Title$="CHECKPOINT SUMMARY"
11250  GOSUB Sub_title
11260  PRINT
11270  GOSUB Menu
11280  INPUT "Type the checkpoint number desired (1 to 17), and press ENTER. ",Test_number
11290  IF (Test_number <1) OR (Test_number >17) THEN GOTO Integer_error
11300  Checkpoint=Test_number
11310  GOTO Branch_checkpt
11320  Integer_error:!
11330  DISP "Please enter an integer only, 1 through 17.";CHR$(7)
11340  GOTO Test_entry
11350  Branch_checkpt:!
11360  IF (Checkpoint=0 OR Checkpoint=18) THEN GOTO Print_results
11370  ON Checkpoint GOTO Chk1, Chk2, Chk3, Chk4, Chk5, Chk6, Chk7, Chk8, Chk9, Chk10, Chk11,
       Chk12, Chk13, Chk14, Chk15, Chk16, Chk17
11380  Print_results:!
11390  PRINTER IS CRT
11400  OUTPUT KBD;CHR$(255)&"K";
11410  PRINT "Do you wish to have a hardcopy of the results?"
11420  GOSUB Clear_keys
11430  ON KEY 1 LABEL " YES" GOTO Print_it
11440  ON KEY 6 LABEL " " GOTO Print_it
11450  ON KEY 4 LABEL " NO" GOTO No_print
11460  ON KEY 9 LABEL " " GOTO No_print
11470  GOSUB Wait_for_key
11480  RETURN
11490  Clear_keys: !
11500  CONTROL 1,12;0 ! KEY LABELS ON
11510  ON KEY 0 LABEL " " GOSUB Key_trap
11520  ON KEY 1 LABEL " " GOSUB Key_trap
11530  ON KEY 2 LABEL " " GOSUB Key_trap
11540  ON KEY 3 LABEL " " GOSUB Key_trap
11550  ON KEY 4 LABEL " " GOSUB Key_trap
11560  ON KEY 5 LABEL " " GOSUB Key_trap
11570  ON KEY 6 LABEL " " GOSUB Key_trap
11580  ON KEY 7 LABEL " " GOSUB Key_trap
11590  ON KEY 8 LABEL " " GOSUB Key_trap
11600  ON KEY 9 LABEL " " GOSUB Key_trap
11610  RETURN
11620  Menu:!
11630  CONTROL 1,12;1
11640  Title$="5361A/B CHECKPOINT SUMMARY"
11650  GOSUB Sub_title
11660  PRINT
11670  PRINT " 1 'REMOTE', 'LOCAL LOCKOUT', 'LOCAL' ** 9 'SAMPLE' and 'TRIGGER'"
11680  PRINT " 2 Self Check ('TEST?') ** 10 'RESOL' and 'HIRESOL'"
11690  PRINT " 3 'DISPLAY' ** 11 'OFFSET', 'SCALE', and 'SMOOTH'"
11700  PRINT " 4 'INIT' and 'RESET' ** 12 'AUTO' and 'MANUAL'"
11710  PRINT " 5 'REF' and 'OVEN' ** 13 'FMRATE'"
11720  PRINT " 6 'ERR?' ** 14 'SRQMASK'"
```

```
11730  PRINT " 7 'SET' and 'SET?' ** 15 'DUMP'"
11740  PRINT " 8 'LOWZ' and 'HIGHZ' ** 16 'PULSE MEASUREMENT"
11750  PRINT " ** 17 'CHECK ALL ADDRESS'"
11760  RETURN
11770  Print_it:!
11780  GOSUB Keys_off
11790  OUTPUT KBD;CHR$(255)&"K";
11800  PRINTER IS Ptr_add
11810  ON ERROR GOTO Prnt_stuck
11820  ON TIMEOUT Ptr_add DIV 100,1 GOTO Prnt_stuck
11830  OUTPUT Ptr_add USING "#,K";" "! TEST FOR RESPONSE
11840  OFF TIMEOUT
11850  OFF ERROR
11860  GOTO No_print
11870  Prnt_stuck:!
11880  CONTROL 1,12;1
11890  DISP (Ptr_add);" NOT RESPONDING. CHECK PRINTER IS ON, & ADDRESS & HOOK-UP IS CORRECT."
11900  BEEP 600,.3
11910  WAIT 3
11920  OFF TIMEOUT
11930  OFF ERROR
11940  GOTO Print_results
11950  No_print:!
11960  GOSUB Keys_off
11970  OUTPUT KBD;CHR$(255)&"K";
11980  Title$="CHECKPOINT RESULTS"
11990  GOSUB Sub_title
12000  PRINT Horiz_line$
12010  PRINT
12020  PRINT "Counter: ";Inst_id$;" at address";Address
12030  PRINT
12040  FOR Test_number=1 TO 8
12050  PRINT " ";Test_number;TAB(8);Test_results$(Test_number);
12060  PRINT TAB(30);8+Test_number;TAB(34);Test_results$(8+Test_number)
12070  NEXT Test_number
12080  PRINT TAB(30);17;TAB(34);Test_results$(17);
12090  PRINT
12100  PRINT
12110  PRINTER IS CRT
12120  OUTPUT Address;"INIT"
12130  LOCAL 7
12140  GOTO Final_exit
12150  END
```

2

ADJUSTMENTS

2-1. INTRODUCTION

This section describes the adjustments required to maintain the HP 5361B operating characteristics within specification. Adjustments should be made when required, such as after a performance test failure or when components are replaced that may affect an adjustment. If the adjustments are to be considered valid, the HP 5361B line input voltage must be within +5% to –10% of normal.

Table 2-1 lists the adjustment procedures and the recommended order of performance, and identifies the adjustable components involved.

2-2. EQUIPMENT REQUIRED

The test equipment required for the adjustment procedures is listed in *Table B-1* (Recommended Test Equipment) of Appendix B. Substitute test equipment may be used if it meets or exceeds the required characteristics listed in the table.

2-3. ADJUSTMENT LOCATIONS

Adjustment locations are identified in *Figure 2-1*. All adjustments, except for the TCXO standard timebase adjustment, must be made with the top cover removed. The TCXO adjustment is made through the rear panel hole labeled TCXO ADJUST.

2-4. SAFETY CONSIDERATIONS

This section contains warnings and cautions that must be followed for your protection and to avoid damage to the equipment.

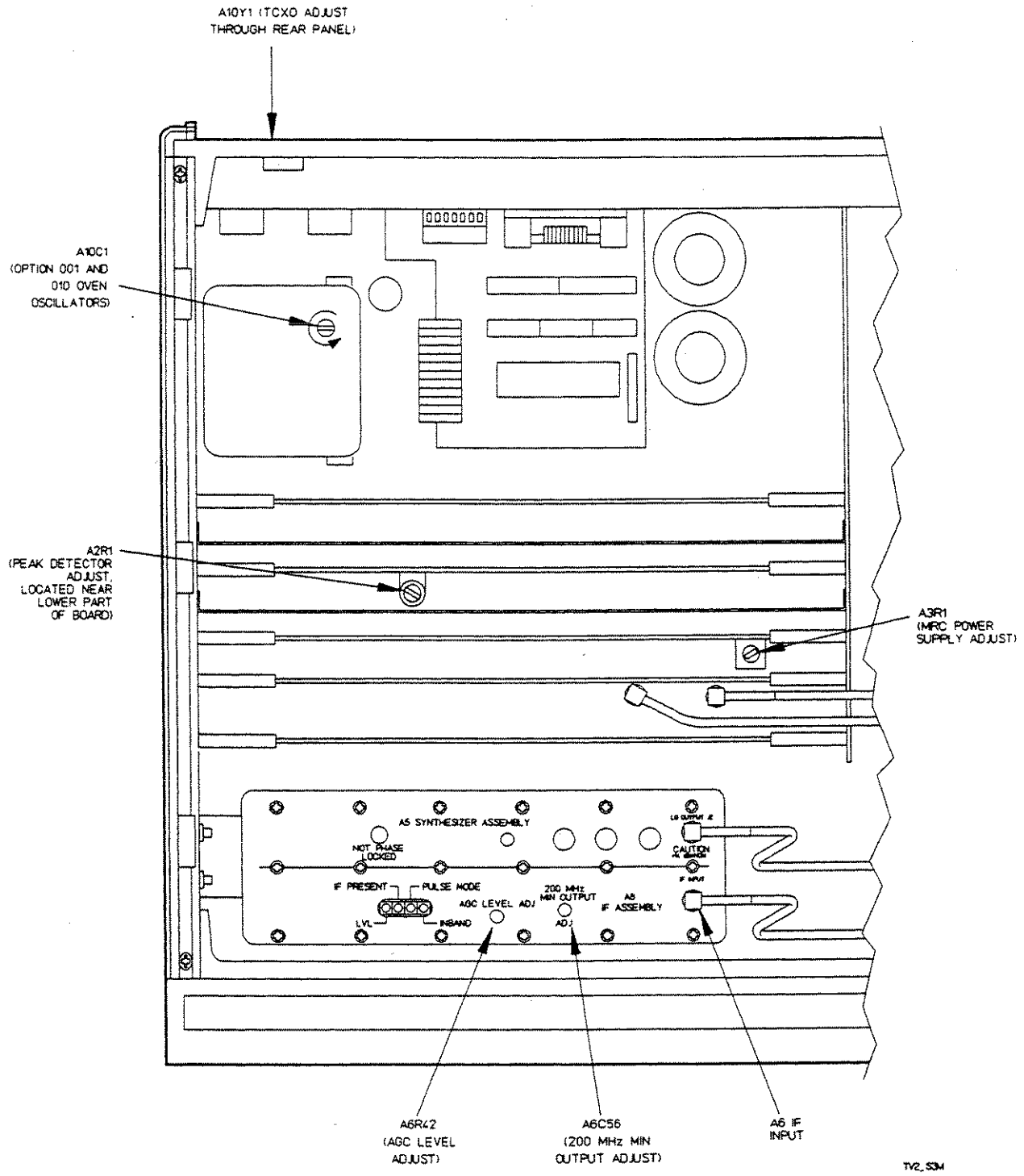


Figure 2-1. HP 5361B Adjustment Locations

2-7. Peak Detector Adjustment (INPUT 2, 50Ω)

Potentiometer A2R1 adjusts the peak detector circuitry for the 50 Ω portion of INPUT 2. The peak detector determines the sensitivity of the input circuitry. To perform this adjustment, proceed as follows:

1. Connect the negative terminal of the HP 3466A DVM to chassis ground of the counter. Connect the positive terminal of the DVM to TP1 at the top of the A2 assembly.

2. Set a synthesizer (HP 8660C/86603A/86632B) for an output of 17 mV (–22.4 dBm) at 400 MHz. Connect the synthesizer output to INPUT 2 of the HP 5361B.

3. Connect the REFERENCE OUTPUT connector on the rear panel of the synthesizer to the rear panel EXT REF IN connector of the counter.

4. Select INPUT 2 (50 Ω impedance) on the HP 5361B by pressing the 50 Ω key.

5. Adjust A2R1 clockwise until the counter just begins to gate and display the 400 MHz signal. It is easiest to find this transition point by noting where the voltage at the test point jumps above 4.5 volts. At this point, the counter should be gating and displaying the 400 MHz signal.

6. To verify the adjustment, set the synthesizer output to –23 dBm at 400 MHz, and verify that the HP 5361B displays all zeroes: 00 000 000 000. Slowly increase the synthesizer level to –22 dBm and verify that the counter displays 400 MHz correctly.

2-8. IF Amplifier Adjustments

The IF amplifier adjustments consist of two separate adjustments, A6R42 and A6C56. Potentiometer A6R42 (AGC LEVEL ADJUST) is adjusted first to set the automatic gain level of the A6 IF bandpass. Next, the frequency response of the 175 MHz elliptic filter is tuned by adjusting A6C56 (200 MHz MIN OUTPUT ADJ) which places one notch of the 175 MHz filter exactly at 200 MHz.

IF AGC LEVEL ADJUSTMENT

To adjust A6R42 (AGC LEVEL ADJ) for IF AGC level control, refer to *Figure* 2-2 and proceed as follows:

1. Remove the instrument's top cover.

2. Disconnect the A6 IF input from the output of A12.

3. Connect the output of the HP 8660B to the input of A6.

4. Set the HP 8660B to 70 MHz at a level of 0 dBm.

5. Connect the HP 436A Power Meter to rear panel IF OUT connector of the HP 5361B.

6. Adjust A6R42 (AGC Level Pot) for a power meter reading of –12.0 dBm ±0.1 dBm. Use a nonmetallic adjustment tool such as the HP P/N 8730-0013 or GC Electronics P/N 8276.

7. Change the HP 8660B power output from –30 to +0 dBm in 10 dB steps (or less) to verify IF output power of –12.0 ±0.3 dBm.

8. Verify that the IF Present/Inband LEDs are ON, and the Level/Pulse Mode LEDs are OFF.

9. Set the HP 8660B to –50 dBm and verify that the Level, IF Present, Pulse Mode and Inband LEDs are OFF.

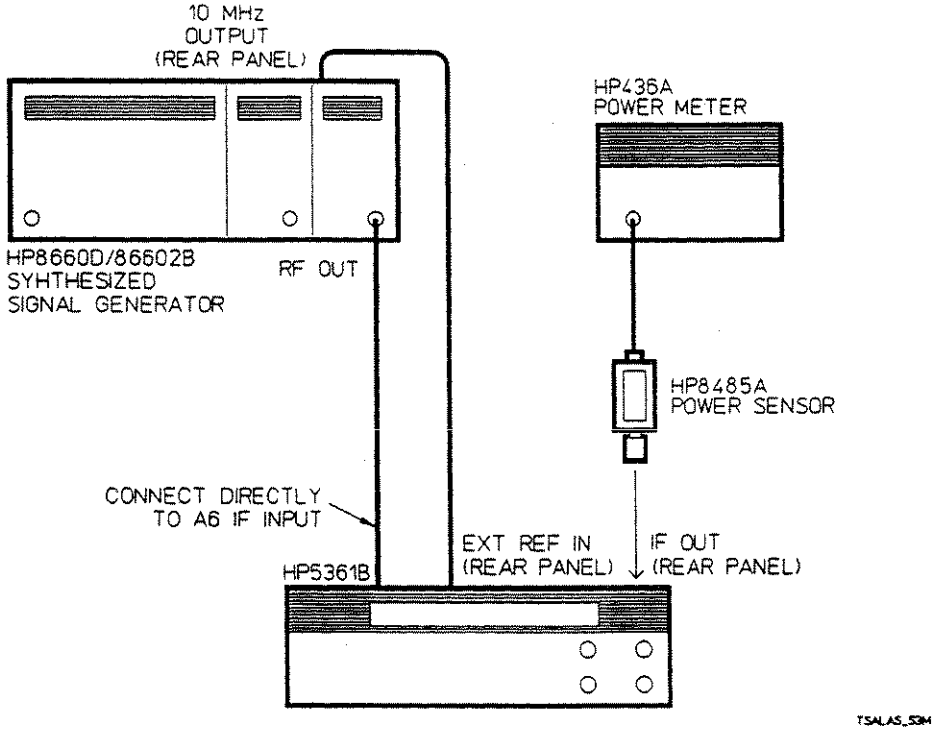


Figure 2-2. AGC Level Adjustment Setup

200 MHZ ELLIPTIC FILTER NOTCH ADJUSTMENT

Capacitor A6C56 (200 MHz MIN OUTPUT ADJ) is adjusted to set the frequency response of the 200 MHz elliptic filter on the A6 IF Amplifier/Detector Assembly. The filter will be adjusted to have maximum attenuation at 200 MHz, thus causing the response of the filter to

be approximately 43 dB down at 200 MHz for open AGC loop response. Refer to *Figure* 2-3. To adjust A6C56, proceed as follows:

1. Remove the instrument's top cover.

2. Disconnect the A6 IF input from the output of A12.

3. Connect the output of the HP 8660B to the input of A6.

4. Connect the IF output of the HP 5361B to the input of the HP 8566B Spectrum Analyzer.

5. Set the HP 8660B Synthesized Sweeper to 200 MHz at 0 dBm.

6. Locate the 200 MHz signal trace on the HP 8566B Spectrum Analyzer display and adjust A6C56 (200 MHz MIN OUTPUT ADJUST) for minimum signal amplitude. Use a non-metallic adjustment tool such as the HP P/N 8730-0013 or GC Electronics P/N 8276.

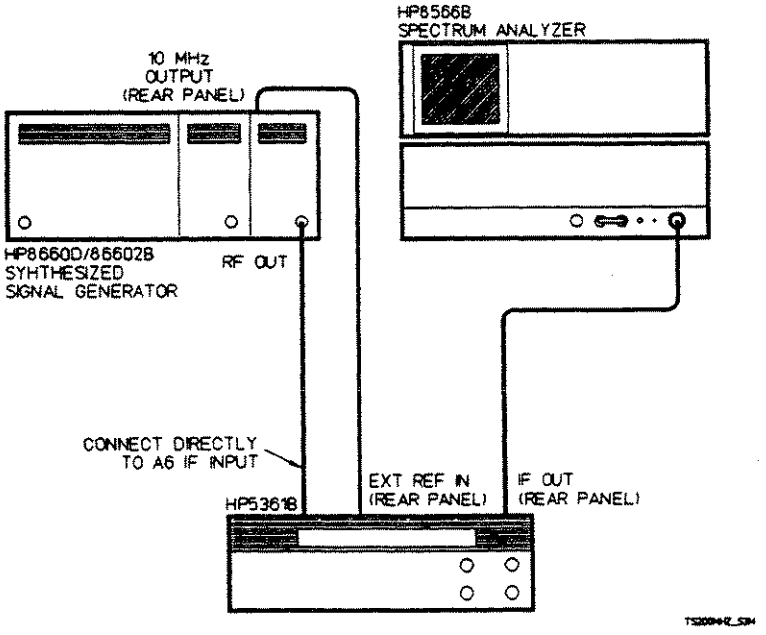


Figure 2-3. 200 MHz Elliptic Filter Notch Adjustment Setup

2-9. TCXO Adjustment (A10 Standard Timebase)

Two procedures are given for adjustment of the TCXO standard timebase. If operation of the counter is only at 25°C (78°F), then adjust the oscillator frequency as close as possible to 10 MHz, using the first procedure, immediately following this paragraph (i.e., TXCO TIMEBASE ADJUSTMENT). If the operation of the counter will be over the full temperature range of 0°C to 50°C, then the TCXO must be offset by the amount labeled on its cover,

using the second procedure "TCXO TIMEBASE/OFFSET ADJUSTMENT". The offset is necessary to keep the TCXO frequency within the manufacturer's temperature specifications. The TCXO standard timebase is factory-set for use at 25°C.

NOTE

Allow the TCXO in the instrument to warm up for a minimum of 30 minutes before making either TCXO adjustment.

TCXO TIMEBASE ADJUSTMENT

To adjust the TCXO Timebase for the average room-temperature environment, (25°C) proceed as follows:

1. Connect a house standard (1, 2, 5, or 10 MHz reference frequency) to the EXTERNAL TRIG INPUT of an oscilloscope and set the main triggering to EXTERNAL. Connect the 5361B rear panel 10 MHz OUT to the Channel A input of the oscilloscope. (See *Figure 2-4.*)

2. Insert a tuning wand through the TCXO ADJUST hole in the rear panel of the 5361B and into the tuning screw of the TCXO (Y1) on the TCXO Assembly. Adjust the TCXO for a minimum sideways movement of the signal on the oscilloscope display.

3. By timing the sideways movement (in cm/second) of the signal on the oscilloscope display, the accuracy of the timebase can be determined based on the oscilloscope sweep speed, as shown in *Table* 2-2. This completes the adjustment of the TCXO for use at 25°C.

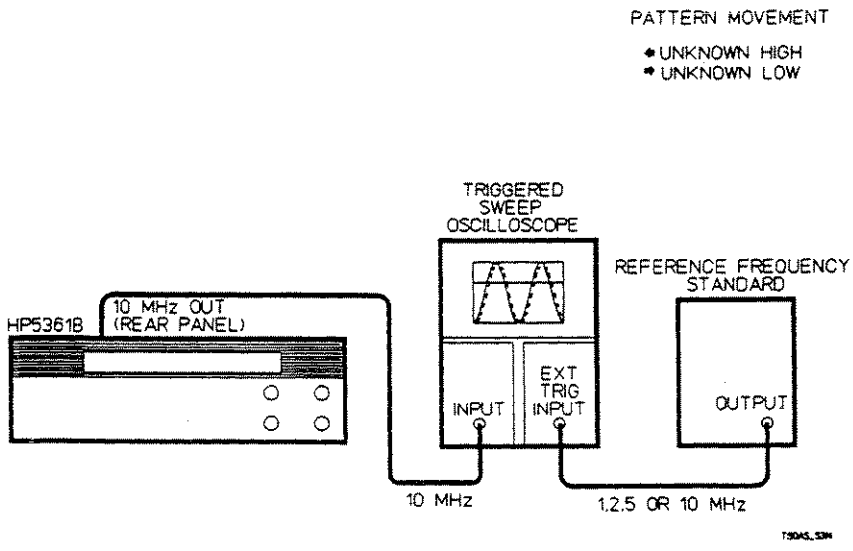


Figure 2-4. Oscillator Adjustment Setup

Table 2-2. TCXO Adjustment (A10 Standard Timebase)

MOVEMENT	SWEEP SPEED			NOTES
	1 µs/cm	0.1 µs/cm	0.01 µs/cm	
1 cm/s	1×10^{-6}	1×10^{-7}	1×10^{-8}	Time scope trace movement with second hand of watch or clock.
1 cm/10s	1×10^{-7}	1×10^{-8}	1×10^{-10}	
1 cm/100s	1×10^{-8}	1×10^{-9}	1×10^{-10}	

TCXO TIMEBASE/OFFSET ADJUSTMENT

To adjust the TCXO Timebase for proper operation over its entire operating temperature range (0°C to 50°C), proceed as follows:

1. Remove the HP 5361B top cover, locate the TCXO, and record the frequency offset (located on the TCXO component cover) on paper.

2. Replace the HP 5361B top cover, turn its power switch to ON, and let the instrument warm up for at least 30 minutes.

3. Connect a house standard (1, 2, 5, or 10 MHz reference frequency) to the external reference input of a high resolution counter such as an HP 5384A Frequency Counter (10 MHz IN/OUT BNC connector).

4. Connect the HP 5361B 10MHZ OUT on the rear panel to Channel A Input of the HP 5384A Frequency Counter.

5. Set the HP 5384A to FREQ A, 1 second GATE TIME.

6. Insert a tuning wand through the TCXO ADJUST hole in the rear panel of the HP 5361B and into the tuning screw of the TCXO (Y1) on the A10 Assembly. Adjust the TCXO frequency to 10 MHz ± the offset labeled on the cover of the TCXO. For example, if the offset is labeled +3.5 Hz, the TCXO should be adjusted for a frequency of 10.0000035 MHz on the HP 5384A display at a room temperature of 25°C. This completes the adjustment of the TCXO with offset for use at 0°C to 50°C.

2-10. Oven Oscillator Adjustment (A10 Option 001 or 010 Timebase)

The following procedure describes the adjustment of the Oven Oscillator Timebase (Option 001) and the High Stability Timebase (Option 010). To perform the adjustment, refer to *Figure* 2-4 and proceed as follows:

NOTE

Allow the oven oscillator to warm up for a minimum of 24 hours before making this adjustment.

1. Connect a house standard (1, 2, 5, or 10 MHz reference frequency) to the EXTERNAL SYNC INPUT of an oscilloscope and set the oscilloscope to EXTERNAL SYNC. Connect the HP 5361B rear panel 10 MHZ OUT to the Channel A input of the oscilloscope. (See *Figure 2-4.*)

2. Remove the top cover of the instrument and locate the adjustment (A10C1) on the top of the oven oscillator, as shown in *Figure 2-1.*

3. Adjust the oscillator for minimum sideways movement of the signal displayed on the oscilloscope. Increase the oscilloscope sweep speed for greater resolution.

4. By timing the sideways movement (in cm/second) of the signal on the oscilloscope display, the approximate offset can be be determined based on the oscilloscope sweep speed, as shown in *Table 2-2.* For example, if the trace moves 5 cm in 10 seconds and the sweep speed is 0.01 μs/cm, the oscillator's signal is within 5×10^{-9} of the reference frequency. The calculation can also be made as follows:

$$\frac{\Delta f}{f} = \frac{\Delta t}{t}$$

$$\frac{\Delta f}{f} = \frac{5 \times 0.01 \mu s/cm}{10s} = 5 \times 10^{-9}$$

where

$\frac{\Delta f}{f}$ is the normalized frequency difference between the oscillator and the reference signal.

Δt is the change observed in the oscilloscope.

t is the time required for Δt to occur.

5. After adjustment, the oven oscillator (Option 001 or 010) should be within 5×10^{-9} of the reference frequency. The Oven Oscillator adjustment for the Option 001 or 010 Timebase is now completed.

3

REPLACEABLE PARTS

3-1. INTRODUCTION

This section contains information for ordering parts. *Table 3-1* is a list of exchange assemblies, and *Table 3-2* is a list of abbreviations and reference designations used in the parts list and throughout the manual. *Table 3-3* lists all replaceable parts for the Standard HP 5361B and HP 5361A. *Table 3-4* lists all replaceable parts for Options. *Table 3-5* is a listing of the manufacturer's code numbers given in the parts list.

3-2. EXCHANGE ASSEMBLIES

The only assembly within the instrument that may be replaced on an exchange basis is the U1 Sampler contained inside the A12 Microwave Module. The factory repaired and tested exchanged assemblies are available only on a trade-in basis; therefore, the defective assemblies must be returned for credit. For this reason, assemblies required for spare parts stock must be ordered by the "new assembly" part number. The part numbers for the U1 Sampler assemblies are listed below:

Table 3-1. Exchange Assemblies

ASSEMBLY	NEW ASSEMBLY HP PART NO.	EXCHANGE ASSEMBLY HP PART NO.
U1 Sampler for Standard HP 5361A and 5361B, and HP 5361B/Option 026	05361-60204	05361-69204
U1 Sampler for HP 5361B/Option 040	05361-60205	05361-69205

3-3. SPECIAL PARTS REPLACEMENT CONSIDERATIONS

Certain mechancical parts and electrical components require special considerations. These are as follows:

- The A9 Display/Driver Assembly consists of the Liquid Crystal Display, and the display driver and backlight circuits. The A9 Display/Driver Assembly is not a repairable assembly. If any portion of the assembly is defective, a new Display/Driver Assembly must be ordered (HP P/N 05350-60123).

- Option 010 High Stability Timebase: The Option 010 High Stability Oven Oscillator (HP P/N 10811-60211) is not a field repairable assembly. If service is required, order HP Part Number 10811-69111.

3-4. ABBREVIATIONS AND REFERENCE DESIGNATIONS

Table 3-1 lists abbreviations and reference designations used in the parts list, schematics, and throughout the manual. In some cases, two forms of the abbreviations are used, one all in capital letters, and one with partial or no capitals. This occurs because the abbreviations in the parts list are in capital letters only, while other abbreviation forms, with lower case and upper case letters, are used in the schematics and other parts of the manual.

3-5. REPLACEABLE PARTS LIST

Table 3-3 and *3-4* are lists of the replaceable parts and are organized as follows:

1. Electrical assemblies and their components in alphanumeric order by reference designation.
2. Chassis-mounted electrical parts in alphanumeric order by reference designation.
3. Chassis hardware and mechanical parts in alphanumeric order by reference designation.

The information given for each part consists of the following:

1. The Hewlett-Packard part number.
2. Part number check digit (CD).
3. The total quantity (Qty) in each individual assembly.
4. The description of the part.
5. A typical manufacturer of the part in a five-digit code.
6. The manufacturer's part number for the part.

The total quantity for each part used within an assembly is given only once at the first appearance of the part number in the list for that assembly.

3-6. HOW TO ORDER A PART

Hewlett-Packard wants to keep your parts ordering process as simple and efficient as possible. Think of the process as having the following steps:

- Identifying the part and the quantity you want.
- Determining the ordering method to be used and contacting Hewlett-Packard.

3-7. Parts Identification

To identify the part(s) you want, first refer to the Service information in the manual for the product. Use schematic diagrams and component locator diagrams, and parts list descriptions.

When ordering from Hewlett-Packard, the important numbers to note from the Parts List are the HP Part Number and part-number check digit (in the "CD" column), and the quantity of the part you want.

If the part you want is *not* identified in the manual, you can call on Hewlett-Packard for help (see "Contacting Hewlett-Packard" below). Please have the following information at hand when you contact HP for help:

- Instrument Model Number (example "HP 5361B").
- Complete instrument Serial Number (example "1234A56789"). Information about where to find the serial number is given at the front of the Operating and Programming Manual in the "HOW TO USE THIS MANUAL" section.
- Description of the part and its use.
- Quantity of the part required.

3-8. Contacting Hewlett-Packard

Depending on where you are in the world, there are one or more ways in in which you can get parts or parts information from Hewlett-Packard.

- **Outside the United States**, contact your local HP sales office. HP sales offices are listed at the back of this manual.
- **Within the United States**, we encourage you to order replacement parts or request parts information directly by telephone or mail from the HP Support Materials Organization, using the telephone numbers or address listed below. (You can also contact your local HP sales office. HP sales offices are listed at the back of this manual.)

By telephone:

- For Parts Ordering, use our toll-free number, (800) 227-8164, Monday through Friday (except Holidays), 6 am to 5 pm (Pacific Time).

  If you need a part in a hurry, an extra-cost Hotline phone ordering service is available, 24 hours a day. Use the toll-free number above at the times indicated; at other times, use (415) 968-2347.

- For Parts Identification Assistance, call us at (916) 783-0804. Our Parts Identification hours are from Monday through Friday, 6 am to 5 pm (Pacific Time).

For mail correspondence, use the address below:

Hewlett-Packard
Support Materials Roseville
P.O. Box 1145
Roseville, CA 95661-1145

3-9. CABINET PARTS AND HARDWARE

To locate and identify miscellaneous cabinet and chassis parts and instrument hardware, refer to *Figures 3-1* through *3-5*. These figures provide various exploded views of the instrument, with the parts identified by reference designations. Most of the illustrations are accompanied by a table containing part number, description, and quantity information for each reference designation shown. The quantity indicated represents the total used within the instrument.

REFERENCE DESIGNATIONS

A	=	assembly	DS	=	annunciator; signaling device audio or visual; lamp; LED	LS	=	audible alarm; audible signaling device; buzzer; transducer	TB	=	terminal board
AT	=	attenuator, isolator; termination	E	=	miscellaneous electrical part	M	=	metre	TC	=	thermocouple
B	=	fan, motor	F	=	fuse	MP	=	miscellaneous mechanical part	TP	=	test point
BT	=	battery	FL	=	filter	P	=	electrical connector, movable portion; plug	U	=	integrated circuit; microcircuit
C	=	capacitor	H	=	hardware				V	=	electron tube
CP	=	coupler	HY	=	circulator	Q	=	transistor; SCR; triode thyristor	VR	=	voltage regulator; breakdown diode
CR	=	diode; diode thyristor; varactor	J	=	electrical connector stationary portion, jack	R	=	resistor	W	=	cable; transmission path; wire; jumper
DC	=	directional coupler	K	=	relay	RT	=	thermistor	X	=	socket
DL	=	delay line	L	=	coil; inductor	S	=	switch	Y	=	crystal unit-piezo-electric
						T	=	transformer	Z	=	tuned cavity; tuned circuit

ABBREVIATIONS

A	=	ampere	HD	=	head	N/C	=	normally closed	SI	=	silicon
ac	=	alternating current	HDW	=	hardware	NE	=	neon	SIL	=	silver
ACCESS	=	accessory	HF	=	high frequency	NEG	=	negative	SL	=	slide
ADJ	=	adjustment	HG	=	mercury	nF	=	nanofarad	SNR	=	signal-to-noise ratio
A/D	=	analog-to-digital	HI	=	high	NI PL	=	nickel plate	SPDT	=	single-pole, double-throw
AF	=	audio frequency	HP	=	Hewlett-Packard	N/O	=	normally open	SPG	=	spring
AFC	=	automatic frequency control	HPF	=	high pass filter	NOM	=	nominal	SPL	=	special
AGC	=	automatic gain control	HR	=	hour (used in parts list)	NORM	=	normal	SPST	=	single-pole, single-throw
AL	=	aluminum	HV	=	high voltage	NPN	=	negative-positive-negative	SR	=	split ring
ALC	=	automatic level control	Hz	=	hertz	NP0	=	negative-positive zero (zero temperature coefficient)	SSB	=	single sideband
AM	=	amplitude modulation	IC	=	integrated circuit				SST	=	stainless steel
AMPL	=	amplifier	ID	=	inside diameter	NRFR	=	not recommended for field replacement	STL	=	steel
APC	=	automatic phase control	IF	=	intermediate frequency				SQ	=	square
ASSY	=	assembly	IMPG	=	impregnated	ns	=	nanosecond	SWR	=	standing-wave ratio
AUX	=	auxiliary	in	=	inch	NSR	=	not separately replaceable	SYNC	=	synchronize
AVG	=	average	INCD	=	incandescent	nW	=	nanowatt	T	=	timed (slow-blow fuse)
AWG	=	american wire gauge	INCL	=	include(s)	OBD	=	order by description	TA	=	tantalum
BAL	=	balance	INP	=	input	OD	=	outside diameter	TC	=	temperature compensating
BCD	=	binary-coded decimal	INS	=	insulation	OH	=	oval head	TD	=	time delay
BD	=	board	INT	=	internal	OP AMPL	=	operational amplifier	TERM	=	terminal
BE CU	=	beryllium copper	kg	=	kilogram	OPT	=	option	TFT	=	thin-film transistor
BFO	=	beat frequency oscillator	kHz	=	kilohertz	OSC	=	oscillator	TGL	=	toggle
BH	=	binder head	kΩ	=	kilohm	OX	=	oxide	THD	=	thread
BKDN		breakdown	kV	=	kilovolt	oz	=	ounce	THRU	=	through
BP	=	bandpass	lb	=	pound	Ω	=	ohm	TI	=	titanium
BPF	=	bandpass filter	LC	=	inductance-capacitance	P	=	peak (used in parts list)	TOL	=	tolerance
BRS	=	brass	LED	=	light-emitting diode	PAM	=	pulse-amplitude modulation	TRIM	=	trimmer
BWO	=	backward wave oscillator	LF	=	low frequency	PC	=	printed circuit	TSTR	=	transistor
CAL	=	calibrate	LG	=	long	PCM	=	pulse-code modulation; pulse-count modulation	TTL	=	transistor-transistor logic
ccw	=	counterclockwise	LH	=	left hand				TV	=	television
CER	=	ceramic	LIM	=	limit	PDM	=	pulse-duration modulation	TVI	=	television interference
CHAN	=	channel	LIN	=	linear taper (used in parts list)	pF	=	picofarad	TWT	=	traveling wave tube
cm	=	centimeter	lin	=	linear	PH BRZ	=	phosphor bronze	U	=	micro (10^{-6}) (used in parts list)
CMO	=	cabinet mount only	LK WASH	=	lock washer	PHL	=	phillips	UF	=	microfarad (used in parts list)
COEF	=	coefficient	LO	=	low; local oscillator	PIN	=	positive-intrinsic-negative	UHF	=	ultra-high frequency
COM	=	common	LOG	=	logarithmic taper (used in parts list)	PIV	=	peak inverse voltage	UNREG	=	unregulated
COMP	=	composition				pk	=	peak	V	=	volt
COMPL	=	complete	log	=	logarithmic	PL	=	phase lock	VA	=	voltampere
CONN	=	connector	LPF	=	low pass filter	PLL	=	phase-lock loop	Vac	=	volts ac
CP	=	cadmium plate	LV	=	low voltage	PLO	=	phase lock oscillator	VAR	=	variable
CRT	=	cathode ray tube	m	=	metre (distance)	PM	=	phase modulation	VCO	=	voltage-controlled oscillator
CTL	=	complementary transistor logic	mA	=	milliampere	PNP	=	positive-negative-positive	Vdc	=	volts dc
CW	=	continuous wave	MAX	=	maximum	P/O	=	part of	VDCW	=	volts, dc, working (used in parts list)
cw	=	clockwise	MΩ	=	megohm	POLY	=	polystyrene			
D/A	=	digital-to-analog	MEG	=	meg (10^6) (used in parts list)	PORC	=	porcelain	V(F)	=	volts, filtered
dB	=	decibel	MET FILM	=	metal film	POS	=	positive; position(s) (used in parts list)	VFO	=	variable-frequency oscillator
dBm	=	decibel referred to 1mW	MET OX	=	metal oxide				VHF	=	very-high frequency
dc	=	direct current	MF	=	medium frequency; microfarad (used in parts list)	POSN	=	position	Vpk	=	volts peak
deg	=	degree (temperture interval or difference)				POT	=	potentiometer	Vp-p	=	volts peak-to-peak
... °	=	degree (plane angle)	MFR	=	manufacturer	p-p	=	peak-to-peak	Vrms	=	volts rms
°C	=	degree Celsius (centigrade)	mg	=	milligram	PP	=	peak-to-peak (used in parts list)	VSWR	=	votage standing wave ratio
°F	=	degree Fahrenheit	MHz	=	megahertz				VTO	=	voltage-tuned oscillator
°K	=	degree Kelvin	mH	=	millihenry	PPM	=	pulse-position modulation	VTVM	=	vacuum-tube voltmeter
DEPC	=	deposited carbon	mho	=	conductance	PREAMPL	=	preamplifier	V(X)	=	volts, switched
DET	=	detector	MIN	=	minimum	PRF	=	pulse-repetition frequency	W	=	watt
diam	=	diameter	min	=	minute (time)	PRR	=	pulse-repetition rate	W/	=	with
DIA	=	diameter (used in parts list)	... '	=	minute (plane angle)	ps	=	picosecond	WIV	=	working inverse voltage
DIFF AMPL	=	differential amplifier	MINAT	=	miniature	PT	=	point	WW	=	wirewound
div	=	division	mm	=	millimeter	PTM	=	pulse-time modulation	W/O	=	without
DPDT	=	double-pole, double-throw	MOD	=	modulator	PWM	=	pulse-width modulation	YIG	=	yttrium-iron-garnet
DR	=	drive	MOM	=	momentary	PWV	=	peak working voltage	Zo	=	characteristic impedance
DSB	=	double sideband	MOS	=	metal-oxide semiconductor	RC	=	resistance capacitance			
DTL	=	diode-transistor logic	ms	=	millisecond	RECT	=	rectifier			
DVM	=	digital voltmeter	MTG	=	mounting	REF	=	reference			
ECL	=	emitter-coupled logic	MTR	=	meter (indicating device)	REG	=	regulated			
EMF	=	electromotive force	MUX	=	multiplexer	REPL	=	replaceable			
EDP	=	electronic data processing	mV	=	millivolt	RF	=	radio frequency			
ELECT	=	electrolytic	mVac	=	millivolt, ac	RFI	=	radio frequency interference			
ENCAP	=	encapsulated	mVdc	=	millivolt, dc	RH	=	round head; right hand			
EXT	=	external	mVpk	=	millivolt, peak	RLC	=	resistance-inductance-capacitance			
F	=	farad	mVp-p	=	millivolt, peak-to-peak						
FET	=	field-effect transistor	mVrms	=	millivolt, rms	RMO	=	rack mount only			
F/F	=	flip-flop	mW	=	milliwatt	rms	=	root-mean-square			
FH	=	flat head	MY	=	mylar	RND	=	round			
FIL H	=	fillister head	μA	=	microampere	ROM	=	read-only memory			
FM	=	frequency modulation	μF	=	microfarad	R&P	=	rack and panel			
FP	=	front panel	μH	=	microhenry	RWV	=	reverse working voltage			
FREQ	=	frequency	μmho	=	micromho	S	=	scattering parameter			
FXD	=	fixed	μs	=	microsecond	s	=	second (time)			
g	=	gram	μV	=	microvolt	... "	=	second (plane angle)			
GE	=	germanium	μVac	=	microvolt, ac	S-B	=	slow-blow fuse (used in parts list)			
GHz	=	gigahertz	μVdc	=	microvolt, dc	SCR	=	silicon controlled rectifier; screw			
GL	=	glass	μVpk	=	microvolt, peak						
GND	=	ground(ed)	μVp-p	=	microvolt, peak-to-peak	SE	=	selenium			
H	=	henry	μVrms	=	microvolt, rms	SECT	=	sections			
h	=	hour	μW	=	microwatt	SEMICON	=	semiconductor			
HET	=	heterodyne	nA	=	nanoampere	SHF	=	super-high frequency			
HEX	=	hexagonal	NC	=	no connection						

NOTE

All abbreviations in the parts list will be in upper case.

MULTIPLIERS

Abbreviation	Prefix	Multiple
T	tera	10^{12}
G	giga	10^{9}
M	mega	10^{6}
k	kilo	10^{3}
da	deka	10
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}
f	femto	10^{-15}
a	atto	10^{-18}

Table 3-3. Standard Instrument Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	**05361-60001**	**9**	**1**	**BD- BUFFER/PWR SUPPLY CONTROL**	**28480**	**05361-60001**
A1C1	0160-0576	5	12	CAPACITOR-FXD 0. 1 UF 50 V	09969	RPE121-105X7R104M50V
A1C2	0160-5862	2	3	CAPACITOR-FXD 240PF 1 00 V	04222	CAC02COG241F100A
A1C3	0160-5862	2		CAPACITOR-FXD 240PF 1 00 V	04222	CAC02COG241F100A
A1C4	0160-0576	5		CAPACITOR-FXD 0. 1 U F 50 V	09969	RPE121-105X7R104MS0V
A1C5	0180-3834	6	4	CAPACITOR-FXD 33UF 1 0 V TA	12344	T398F336K010AS
A1C6	0180-3834	6		CAPACITOR-FXD 33UF 1 0 V TA	12344	T398F336K010AS
A1C7	0180-3771	0	1	CAPACITOR-FXD 1 UF 35 V TA	12344	T398A105K035AS
A1C8	0160-0576	5		CAPACITOR-FXD 0. 1 UF 50 V	09969	RPE121-105X7R104M50V
A1C9	0160-3879	7	8	CAPACITOR-FXD 0.01 UF 1 00 V	09969	RPE121-105X7R103M100V
A1C10	0160-3879	7		CAPACITOR-FXD 0.01 UF 1 00 V	09969	RPE121-105X7R1 03M100V
A1C11	0160-0576	5		CAPACITOR-FXD 0. 1 UF 50 V	09969	RPE121-105X7R104M50V
A1C12	0180-3831	3	2	CAPACITOR-FXD 1 0UF 35 V TA	12344	T398G106K035AS
A1C13	0180-3770	9	3	CAPACITOR-FXD 2.2UF 35 V TA	12344	T39SC225K035AS
A1C14	0160-0576	5		CAPACITOR-FXD 0. 1 UF 50 V	09969	RPE121-105X7R104M50V
A1C15	0160-3874	2	4	CAPACITOR-FXD 0F 200 V	09969	RPE121-105C0G1 00D200V
A1C16	0160-3874	2		CAPACITOR-FXD 0F 200 V	09969	RPE1 21-105C0G 1 00D200V
A1C17	0160-3874	2		CAPACITOR-FXD 0F 200 V	09969	RPE121-105C0G100D200V
A1C18	0160-3879	7		CAPACITOR-FXD 0.01 UF 100 V	09969	RPE121-105X7R103M100V
A1C19	0160-0576	5		CAPACITOR-FXD 0. 1 UF 50 V	09969	RPE121-105X7R104M50V
A1C20	0160-5862	2		CAPACITOR-FXD 240PF 1 00 V	04222	CAC02C0G241F100A
A1C21	0160-3875	3	1	CAPACITOR-FXD 22PF 200 V	09969	RPE1 21-105C0G220J200V
A1C22	0160-0576	5		CAPACITOR-FXD 0.1 UF 50 V	09969	RPE121-105X7R104M50V
A1C23	0180-3834	6		CAPACITOR-FXD 33UF 10 V TA	12344	T398F336K010AS
A1C24	0160-3879	7		CAPACITOR-FXD 0.01 UF 1 00 V	09969	RPE121-105X7R103M100V
A1C25				NOT ASSIGNED		
A1C26	0160-4389	6	2	CAPACITOR-FXD 1 00PF 200 V	09969	RPE1 21-105COG 1 01 J200V
A1C27	0160-4389	6		CAPACITOR-FXD 1 00PF 200 V	09969	RPE1 21-105COG1 01 J200V
A1C28	0180-3834	6		CAPACITOR-FXD 33UF 1 0 V TA	12344	T398F336K010AS
A1C29	0160-0576	5		CAPACITOR-FXD 0. 1 UF 50 V	09969	RPE121-105X7R104M50V
A1C30	0180-3770	9		CAPACITOR-FXD 2.2UF 35 V TA	12344	T398C225K035AS
A1C31	0160-3879	7		CAPACITOR-FXD 0.01 UF 100 V	09969	RPE121-105X7R103M100V
A1C32	0160-0576	5		CAPACITOR-FXD 0. 1 UF 50 V	09969	RPE121-105X7R104M50V
A1C33	0160-0576	5		CAPACITOR-FXD 0.1 UF 50 V	09969	RPE121-105X7R104M50V
A1C34				NOT ASSIGNED		
A1C35	0160-3874	2		CAPACITOR-FXD 0F 200 V	09969	RPE 1 21-105COG 1 00D200V
A1C36	0160-4497	7	1	CAPACITOR-FXD 82PF 200 V	09969	RPE121-105COG820J200V
A1C37	0160-3879	7		CAPACITOR-FXD 0.01 UF 1 00 V	09969	RPE121-105X7R1 03M100V
A1C38	0160-3879	7		CAPACITOR-FXD 0.01 UF 1 00 V	09969	RPE1 21-105X7R1 03M1 00V
A1C39	0180-3770	9		CAPACITOR-FXD 2.2UF 35 V TA	12344	T398C225K035AS
A1C40	0180-3769	6	1	CAPACITOR-FXD 6.8UF 35 V TA	12344	T398F685K035AS
A1C41	0160-4040	6	1	CAPACITOR-FXD 1000PF 1 00 V	09969	RPE1 21-105C0G1 02J100V
A1C42	0160-3879	7		CAPACITOR-FXD 0.01 UF 1 00 V	09969	RPE121-105X7R103M1 00V
A1C43	0160-0576	5		CAP FXD 0.1 UF 50 V	09969	RPE121-105X7R104M50V
A1C44	0160-0576	5		CAPACITOR-FXD 0. 1 UF 50 V	09969	RPE121-105X7R104M50V
A1C45	0160-4547	8	1	CAPACITOR-FXD 150PF 200 V	09969	RPE121-105C0G1 51J200V
A1C46	0180-3831	3		CAPACITOR-FXD 1 0UF 35 V TA	12344	T398G106K035AS
A1CR1	1902-0962	8	1	DIODE-ZNR 15V 5% DO-35 PD=.4W TC=+.087%	28480	1902-0962
A1CR2	1902-0953	7	1	DIODE-ZNR 6.2V 5% DO-35 PD=.4W TC=+.053%	28480	1902-0953
A1CR3	1901-0518	8	2	DIODE-SCHOTTKY SM SIG	12403	5082-2800
A1CR4	1901-0050	3	23	DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A1CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A1CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A1CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A1CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A1CR9	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A1CR10	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A1CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A1CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A1CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A1CR14	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A1CR15	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1CR16	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35		9N171
A1CR17	1901-0047	8	3	DIODE-SWITCHING 20V 75MA 1 0NS DO-35		28480
A1CR18	1902-0951	5	1	DIODE-ZNR 5.12V 5%		28480
A1CR19	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35		9N171
A1CR20	1901-0047	8		DIODE-SWITCHING 20V 75MA 1 0NS DO-35		28480
A1CR21	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35		9N171
A1CR22	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35		9N171
A1CR23	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35		9N171
A1CR24	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35		9N171
A1CR25	1902-0956	0	1	DIODE-ZNR 8.2V 5% DO-35 PD=.4W TC=+.065%		28480
A1CR26	1901-0518	8		DIODE-SCHOTTKY SM SIG		12403
A1CR27	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35		9N171
A1CR28				NOT ASSIGNED		
A1CR29	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35		9N171
A1CR30	1901-0047	8		DIODE-SWITCHING 20V 75MA 1 0NS DO-35		28480
A1CR31	1901-0539	3	1	DIODE-SCHOTTKY SM SIG		28480
A1CR32	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35		9N171
A1CR33	1901-0050	3		D1ODE-SWITCHING 80V 200MA 2NS DO-35		9N171
A1CR34	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35		9N171
A1DS1	1990-1022	8	1	LED-LAMP LUM-INT=4MCD IF=25MA-MAX BVR=5V		28480
A1L1	9100-0348	2	3	INDUCTOR RF-CH-MLD 1UH ±1%		91637
A1L2	9100-0348	2		INDUCTOR RF-CH-MLD 1 UH ±1 %		91637
A1L3	9140-0181	5	2	INDUCTOR RF-CH-MLD 22UH ±5%		91637
A1L4	9140-0549	9	2	INDUCTOR RF-CH-MLD 8.2UH ±5%		91637
A1L5	9140-0181	5		INDUCTOR RF-CH-MLD 22UH ±5%		91637
A1L6	9140-0549	9		INDUCTOR RF-CH-MLD 8.2UH ±5%		91637
A1L7	9140-0906	2	1	INDUCTOR 1MH ±10%.172D-INX.43LG-IN		04099
A1L8	9100-0348	2		INDUCTOR RF-CH-MLD 1UH ±1%		91637
A1L9	9140-0634	3	1	INDUCTOR RF-CH-MLD 10UH ±10%		32159
A1MP1	1480-0116	8	2	PIN-GRV.062-IN-DIA.25-IN-LG STL		73957
A1MP2	4040-0748	3	2	EXTR-PC BD BLK POLYC.062-IN-BD-THKNS		28480
A1MP3	2110-0269	0	2	FUHLR-CLP-TYP		91506
A1P1A/P1B	1251-7986	9	2	CONNECTOR-POST TYPE 50-CONT		28480
A1Q1	1854-0215	1	6	TRANSISTOR NPN SI TO-92 PD=350MW		04713
A1Q2	1854-0215	1		TRANSISTOR NPN SI TO-92 PD=350MW		04713
A1Q3	1854-0092	2	2	TRANSISTOR NPN SI PD=200MW FT=600MHZ		27014
A1Q4	1854-0092	2		TRANSISTOR NPN SI PD=200MW FT=600MHZ		27014
A1Q5	1853-0036	2	5	TRANSISTOR PNP SI TO-92 PD=625MW		04713
A106	1853-0036	2		TRANSISTOR PNP SI TO-92 PD=625MW		04713
A1Q7	1853-0036	2		TRANSISTOR PNP SL TO-92 PD=625MW		04713
A1Q8	1853-0281	9	4	TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW		04713
A1Q9	1853-0281	9		TRANSISTOR PNP 2N2907A SL TO-18 PD=400MW		04713
A1Q10	1854-0215	1		TRANSISTOR NPN SI TO-92 PD=350MW		04713
A1011				NOT ASSIGNED		
A1012	1853-0036	2		TRANSISTOR PNP SL TO-92 PD=625MW		04713
A1Q13	1854-0215	1		TRANSISTOR NPN SI TO-92 PD=350MW		04713
A1Q14				NOT ASSIGNED		
A1Q15	1853-0036	2		TRANSISTOR PNP SI TO-92 PD=625MW		04713
A1Q16	1854-0215	1		TRANSISTOR NPN SI TO-92 PD=350MW		04713
A1Q17	1853-0405	9	1	TRANSISTOR PNP SI PD=300MW FT=850MHZ		04713
A1Q18				NOT ASSIGNED		
A1Q19				NOT ASSIGNED		
A1Q20	1854-0215	1		TRANSISTOR NPN SI TO-92 PD=350MW		04713
A1Q21	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW		04713
A1Q22	1853-0281	9		TRANSISTOR PNP 2N2907A SI TO- 1 8 PD=400MW		04713
A1R1	0698-3158	4	2	RESISTOR 23.7K ±1 %. 1 25W TF TC=0±1 00		12498
A1R2	0757-0442	9	3	RESISTOR 1 0K ±1 %. 1 25W TF TC=0±1 00		12498
A1R3	2100-3353	8	1	RESISTOR-TRMR 20K 1 0% TKF SI DE-ADJ 1 -TRN		28480
A1R4	0698-3158	4		RESISTOR 23.7K ± 1 % . 1 25W TF TC=0± 1 00		12498
A1R5	0757-0199	3	6	RESISTOR 21.5K ± 1 % . 1 25W TF TC=0± 1 00		12498

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R6	0698-3441	8	2	RESISTOR 215 ±1%.125W TF TC=0±100	12498	CT4-1/8-TO-215R-F
A1R7	0757-0280	3	3	RESISTOR1K ±1%.125W TFTC=0±100	12498	CT4-1/8-TO-1001-F
A1R8	0757-0416	7	3	RESISTOR 511 ±1%.125W TF TC=0±100	12498	CT4-1/8-TO-51 1 R-F
A1R9	0698-0084	9	4	RESISTOR 2.15K ±1 %.1 25W TF TC=0±1 00	12498	CT4-1/8-TO-2151-F
A1R10	0757-0280	3		RESISTOR 1 K ±1 %. 1 25W TF TC=0±1 G0	12498	CT4-1/8-TO-1001-F
A1R11	0757-0416	7		RESISTOR 511 ±1%.125W TF TC=0±1 00	12498	CT4-1/8-TO-51 1 R-F
A1R12	0698-0084	9		RESISTOR 2.15K ±1 %. 1 25W TF TC=0±1 00	12498	CT4-1/8-TO-2151-F
A1R13	0699-0069	2	1	RESISTOR 2.15M ±1 %. 1 25W TF TC=0±1 00	19701	5033R
A1R14	0757-0199	3		RESISTOR 21.5K ±1 %. 1 25W TF TC=0±1 00	12498	CT4-1/8-TO-2152-F
A1R15				NOT ASSIGNED		
A1R16	0698-3154	0	1	RESISTOR 4.22K ±1 %. 1 25W TF TC=0±1 00	12498	CT4-1/8-TO-4221-F
A1R17	0757-0416	7		RESISTOR 511 ±1%.125W TF TC=0±1 00	12498	CT4-1/8-TO-51 1 R-F
A1R18	0757-0199	3		RESISTOR 21.5K ±1 %. 1 25W TF TC=0±1 00	12498	CT4-1/8-TO-2152-F
A1R19	0698-3441	8		RESISTOR 215 ±1%.125W TF TC=0±1 00	12498	CT4-1/8-TO-215R-F
A1R20	0757-0274	5	2	RESISTOR 1.21 K ±1 %. 1 25W TF TC=0±1 00	12498	CT4-1/8-TO-1211-F
A1R21	0757-0442	9		RESI STOR 1 0K ± 1 %. 1 25W TF TC=0±100	12498	CT4-1/8-TO-1002-F
A1R22	0757-0274	5		RESI STOR 1.21 K ± 1 %. 1 25W TF TC=0± 1 00	2M627	CRB1 4 OR CRB25
A1R23	0698-0084	9		RESISTOR 2.15K ± 1 %. 1 25W TF TC=0± 1 00	12498	CT4-1/8-TO-2151-F
A1R24	0757-0438	3	5	RESISTOR 5.1 1 K ± 1 %. 1 25W TF TC=0± 1 00	12498	CT4-1/8-TO-5111-F
A1R25				NOT ASSIGNED		
A1R26	0757-0199	3		RESISTOR 21.5K ±1 %. 1 25W TF TC=0±1 00	12498	CT4-1/8-TO-2152-F
A1R27	0757-0199	3		RESISTOR 21.5K ± 1 %. 1 25W TF TC=0±1 00	12498	CT4-1/8-TO-2152-F
A1R28	1810-0406	0	6	NETWORK-RES 8-SIP 10.0K OHM X 4	32997	430BR-102-103
A1R29	1810-0207	9	1	NETWORK-RES 8-SIP 22.0K OHM X 7	C1433	750-81
A1R30	1810-0406	0		NETWORK-RES 8-SIP 10.0K OHM X 4	32997	4308R-102-103
A1R31	0698-6264	9	2	RESISTOR 400 ±0.5%.125W TF TC=0±100	12498	NA4
A1R32	0698-3458	7	1	RESISTOR 348K ±1%.125W TF TC=0±1 00	12498	CT4
A1R33	0757-0438	3		RESISTOR 5.1 1K ±1%.125W TF TC=0±100	12498	CT4-1/8-TO-51 1 1 - F
A1R34	0698-0084	9		RESISTOR 2.15K ± 1 %. 1 25W TF TC=0● 1 00	12498	CT4-1/8-TO-2151-F
A1R35	1810-0223	9	1	NETWORK-RES 8-SIP 1.0M OHM X 7	91637	$
A1R36	1810-0406	0		NETWORK-RES 8-SIP 1 0.0K OHM X 4	32997	4308R-102-103
A1R37	1810-0444	6	1	NETWORK-RES 8-SIP 1 00.0K OHM X 4	32997	4308R-102-104
A1R38	1810-0374	1	1	NETWORK-RES 8-SIP 1.0K OHM X 4	32997	4308R-102-102
A1R39	0757-1094	9	1	RESISTOR 1.47K ±1 %. 1 25W TF TC=0±1 00	12498	CT4-1/8-TO-1471-F
A1R40	0757-0438	3		RESISTOR 5.1 1 K ±1 %. 125W TF TC=0● 1 00	12498	CT4-1/8-TO-51 1 1 -F
A1R41	0698-6360	6	11	RESISTOR 1 0K ±0. 1 %. 1 25W TF TC=0±25	12498	NE55
A1R42	0698-6360	6		RESISTOR 1 0K ●0. 1 %. 1 25W TF TC=0±25	12498	NE55
A1R43	0698-6360	6		RESI STOR 1 0K ±0. 1 %. 1 25W TF TC=0●25	12498	NE55
A1R44	0698-6360	6		RESISTOR 1 0K ±0. 1 %. 1 25W TF TC=0±25	12498	NE55
A1R45	1810-0406	0		NETWORK-RES 8-SIP 10.0K OHM X 4	32997	4308R-102-103
A1R46	1810-0406	0		NETWORK-RES 8-SIP 10.0K OHM X 4	32997	4308R-102-103
A1R47	1810-0347	8	1	NETWORK-RES 8-SIP 2.2K OHM X 4	32997	4308R-102-222
A1R48	0696-0085	0	1	RESISTOR 2.61 K ±1%.125W TF TC=0●100	12498	CT4-1/8-TO-261 1 -F
A1R49	0757-0418	9	1	RESISTOR 619 ±1%.125W TF TC=0±1 00	12498	CT4-1/8-TO-619R-F
A1R50	0757-0401	0	1	RESISTOR 100 ±1 %. 1 25W TF TC=0±1 00	12498	CT4-1/8-TO-101-F
A1R51	0698-3429	2	1	RESISTOR 19.6 ±1%.125W TF TC=0±1 G0	2M627	CRB14 OR CRB25
A1R52	0698-6360	6		RESi STOR 1 0K ±0. 1 %. 125W TF TC=0±25	12498	NE55
A1R53	0698-6264	9		RESISTOR 400 ±0.5%.125W TF TC=0±100	12498	NA4
A1R54	0757-0463	4	2	RESISTOR 82.5K ± 1 %. 1 25W TF TC=0± 1 00	12498	CT4-1/8-TO-8252-F
A1R55	0757-0442	9		RESISTOR 1 0K ±1 %. 1 25W TF TC=0± 1 00	12498	CT4-1/8-TO-1002-F
A1R56	0757-0424	7	1	RESISTOR 1. 1 K ± 1 %. 1 25W TF TC=0± 1 00	12498	CT4-1/8-TO- 1 1 0 1 - F
A1R57	0757-0280	3		RESISTOR 1 K ± 1 % . 1 25W TF TC=0±1 00	12498	CT4-1/8-TO-1GO1-F
A1R58				NOT ASSIGNED		
A1R59	0698-7212	9	2	RESISTOR 100 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-100R-F
A1R60	0698-7212	9		RESISTOR 100 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-100R-F
A1R61	0698-7188	8	1	RESISTOR 10 ±1 %.05W TF TC=0±100	12498	C3-1/8-TO-10R-F
A1R62	0698-3158	4		RESISTOR 23.7K ±1%.125W TF TC=0±100	2M627	CRB1 4 OR CRB25
A1R63 -R69				NOT ASSIGNED		
A1R70	0698-3157	3	1	RESISTOR 19.6K ●1%.125W TF TC=0●L 00	12498	CT4-1/8-TO-1962-F

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R71	0698-6360	6		RESISTOR 10K ±0.1%.125W TF TC=0±25	12498	NE55
A1R72	0698-6360	6		RESISTOR 10K±0.1%.125WTFTC=0●25	12498	NE55
A1R73	0698-6360	6		RESISTOR 1 0K ±0.1%.125W TF TC=0±25	12498	NE55
A1R74	0698-6360	6		RESISTOR 1 0K ±0.1%.125W TF TC=0±25	12498	NE55
A1R75	0698-6360	6		RESISTOR 1 0K ±0. 1 % . 1 25W TF TC=0±25	12498	NE55
A1R76	0698-8827	4	1	RESISTOR1M ●1%.125WTFTC=0±100	12498	CT4
A1R77	0757-0438	3		RESISTOR 5.1 1K ±1%.125W TF TC=0±100	12498	CT4-1/8-TO-51 1 1-F
A1R78	0757-0438	3		RESISTOR 5.1 1K ±1%.125W TF TC=0±100	12498	CT4-1/8-TO-5111-F
A1R79	0757-0462	3		RESISTOR 75K ± 1 %. 1 25W TF TC=0± 1 00	12498	CT4-1/8-TO-7502-F
A1R80	0757-0465	6	1	RESISTOR 100K ±1%.125W TF TC=0±100	12498	CT4-1/8-TO-1003-F
A1R81	0698-6360	6		RESISTOR 1 0K ±0. 1 %. 1 25W TF TC=0●25	12498	NE55
A1R82	1810-0406	0		NETWORK-RES 8-SIP 1 0.0K OHM X 4	32997	4308R-102-103
A1TP1 -TP7	0360-0124	3	7	CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
A1U1	1826-0718	0	1	IC V RGLTR-V-REF-ADJ 4.95/5.05V 8-DIP-C	04713	MC1404U5
A1U2	1826-0772	6	1	IC V RGLTR-ADJ-POS 1.2/32V TO-92 PKG	04713	LM317LZ
A1U3	1820-1437	0	1	IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
A1U4	1820-1425	6	2	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A1U5	1820-1423	4	1	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A1U6	1820-1442	7	1	IC CNTR TTL LS DECD ASYNCHRO	01295	SN74LS290N
A1U7	1826-0138	8	2	IC COMPARATOR GP QUAD 14-DIP-P PKG	27014	LM339N
A1U8	1826-0138	8		IC COMPARATOR GP QUAD 14-DIP-P PKG	27014	LM339N
A1U9	1820-1074	1	1	IC DRVR TTL NOR QUAD 2-INP	01295	SN74128N
A1U10	1820-1425	6		IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A1U11	1826-0904	6	2	IC V RGLTR-FXD-POS 4.8/5.2V TO-220 PKG	27014	LM330T-5.0
A1U12	1826-0904	6		IC V RGLTR-FXD-POS 4.8/5.2V TO-220 PKG	27014	LM330T-5.0
A1U13	1826-0147	9	1	IC V RGLTR-FXD-POS 11.5/12.5V TO-220 PKG	04713	UA7812UC
A1U14	1826-0161	7	2	IC OP AMP GP QUAD 14-DIP-P PKG	27014	LM324N
A1U15	1826-0161	7		IC OP AMP GP QUAD 14-DIP-P PKG	27014	LM324N

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	**05350-60002**	**7**	**1**	**LOW FREQUENCY INPUT ASSY (SERIES 2713)**	**28480**	**05350-60002**
A2C1	0160-3879	7	11	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C4	0160-4787	8	1	CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30	28480	0160-4787
A2C5	0160-4554	7	8	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A2C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C7	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A2C8	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A2C9	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A2C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C11	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A2C12	0160-0576	5	3	CAPACIATOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A2C13	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A2C14				NOT ASSIGNED		
A2C15	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C16	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C17	0160-4557	0	3	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A2C18	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A2C19				NOT ASSIGNED		
A2C20	0160-4804	0	1	CAPACITOR-FXD 56PF +-5% 100VDC CER 0+-30	28480	0160-4804
A2C21	0180-2929	8	1	CAPACITOR-FXD 68UF +-10% 10VDC TA	28480	0180-2929
A2C22	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C23	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C24	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A2C25	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C26	0160-5649	3	1	CAPACITOR-FXD 100PF +-5% 500VDC CER	28480	0160-5649
A2C27	0160-4704	9	1	CAPACITOR-FXD .01UF +-10% 500VDC CER	28480	0160-4704
A2C28	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C29	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
A2C30	0160-4204	4	1	CAPACITOR-FXD .033UF +-10% 500VDC CER	72982	8131-M500-W5R-333K
A2C31	0160-0576	5		CAPACIATOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A2C32	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2C33	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
A2C34	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A2CR1	1901-0539	3	10	DIODE-SM SIG SCHOTTKY	28480	1901-0539
A2CR2	1901-0539	3		DIODE-SM SIG SCHOTTKY	28480	1901-0539
A2CR3	1901-0539	3		DIODE-SM SIG SCHOTTKY	28480	1901-0539
A2CR4	1901-0539	3		DIODE-SM SIG SCHOTTKY	28480	1901-0539
A2CR5	1901-0539	3		DIODE-SM SIG SCHOTTKY	28480	1901-0539
A2CR6	1901-0539	3		DIODE-SM SIG SCHOTTKY	28480	1901-0539
A2CR7	1901-0539	3		DIODE-SM SIG SCHOTTKY	28480	1901-0539
A2CR8	1901-0539	3		DIODE-SM SIG SCHOTTKY	28480	1901-0539
A2CR9	1901-0539	3		DIODE-SM SIG SCHOTTKY	28480	1901-0539
A2CR10	1901-0539	3		DIODE-SM SIG SCHOTTKY	28480	1901-0539
A2CR11	1901-0050	3	2	DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A2CR12	1901-0376	6	2	DIODE-GEN PRP 35V 50MA DO-35	9N171	1N3595
A2CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A2CR14	1901-0376	6		DIODE-GEN PRP 35V 50MA DO-35	9N171	1N3595
A2L1	9135-0072	2	1	INDUCTOR 56NH 5.893% 2.6D-MMX6.6LG-MM	28480	9135-0072
A2L2	9100-1788	6	4	CORE-FERRITE CHOKE-WIDEBAND;IMP:>680	28480	9100-1788
A2L3	9100-1788	6		CORE-FERRITE CHOKE-WIDEBAND;IMP:>680	28480	9100-1788
A2L4	9100-0368	6	1	INDUCTOR RF-CH-MLD 330NH 10%	28480	9100-0368
A2L5	9100-1788	6		CORE-FERRITE CHOKE-WIDEBAND;IMP:>680	28480	9100-1788
A2L6	9100-1788	6		CORE-FERRITE CHOKE-WIDEBAND;IMP:>680	28480	9100-1788
A2MP1	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
A2MP2	4040-0748	3	2	EXTR-PC BD BLK POLYC .062-IN-BD-THKNS	28480	4040-0748
A2MP3	0403-0026	6	1	PLUG-HOLE BDR-HD FOR .187-D HOLE NYL	02768	207-120241-03-0101
A2MP4	1206-0554	6	1	HEAT SINK SGL DIP	28480	1205-0554
A2P1	1251-7996	9	1	CONN-POST TYPE .100-PIN SPCG 50-CONT	28480	1251-7986

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2Q1	1854-0092	2	2	TRANSISTOR NPN SI PD=200MW FT=600MHZ	26480	1854-0092
A2Q2	1854-0092	2		TRANSISTOR NPN SI PD=200MW FT=600MHZ	26480	1854-0092
A2Q3	1853-0036	2	3	TRANSISTOR PNP SI PD=310MW FT=250MHZ	27014	2N3906
A2Q4	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	27014	2N3906
A2Q5	1854-0215	1	4	TRANSISTOR NPN SI TO-92 PD=350MW	04713	2N3904
A2Q6	1853-0354	7	1	TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A2Q7	1854-0215	1		TRANSISTOR NPN SI TO-92 PD=350MW	04713	2N3904
A2Q8	1854-0215	1		TRANSISTOR NPN SI TO-92 PD=350MW	04713	2N3904
A2Q9	1855-0327	8	1	TRANSISTOR J-FET 2N4416 N-CHAN D-MODE	01295	2N4416
A2Q10	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	27014	2N3906
A2Q11	1854-0215	1		TRANSISTOR NPN SI TO-92 PD=350MW	04713	2N3904
A2R1	2100-2489	9	1	RESISTOR-TRMR 5K 10% C SID-ADJ 1-TRN	73138	82PAR5K
A2R2	0757-0442	9	11	RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1002-F
A2R3	0698-3441	8	4	RESISTOR 215 1% .125W F TC=0+-100	24546	CT4-1/8-TO-215R-F
A2R4	0698-4037	0	2	RESISTOR 46.4 1% .125W F TC=0+-100	28480	0698-4037
A2R5	0699-0073	8	1	RESISTOR 10M 1% .125W F TC=0+-150	28480	0699-0073
A2R6	0698-3441	8		RESISTOR 215 1% .125W F T=0+-100	24546	CT4-1/8-TO-215R-F
A2R7	0757-1094	9	2	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1471-F
A2R8	0757-0458	7	2	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-5112-F
A2R9	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1002-F
A2R10	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1002-F
A2R11	0757-0458	7		RESISTOR 51.1K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-5112-F
A2R12	0698-3155	1	1	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-4641-F
A2R13	0698-3437	2	1	RESISTOR 133 1% .125W F TC=0+-100	24546	CT4-1/8-TO-133R-F
A2R14	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1471-F
A2R15	0757-0421	4	3	RESISTOR 825 1% .125W F TC=0+-100	24546	CT4-1/8-TO-825R-F
A2R16	0698-3443	0	2	RESISTOR 287 1% .125W F TC=0+-100	24546	CT4-1/8-TO-287R-F
A2R17	0698-3440	7	1	RESISTOR 196 1% .125W F TC=0+-100	24546	CT4-1/8-TO-196R-F
A2R18	0698-3439	4	2	RESISTOR 178 1% .125W F TC=0+-100	24546	CT4-1/8-TO-178R-F
A2R19	0757-0403	2	1	RESISTOR 121 1% .125W F TC=0+-100	24546	CT4-1/8-TO-121R-F
A2R20	0698-3158	4	2	RESISTOR 23.7K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-2372-F
A2R21	0757-0401	0	3	RESISTOR 100 1% .125W F TC=0+-100	24546	CT4-1/8-TO-101-F
A2R22	0698-3441	8		RESISTOR 215 1% .125W F T=0+-100	24546	CT4-1/8-TO-215R-F
A2R23	0698-3441	8		RESISTOR 215 1% .125W F T=0+-100	24546	CT4-1/8-TO-215R-F
A2R24	0757-0727	3	2	RESISTOR 562 1% .25W F TC=0+-100	24546	NAS-1/4-TO-562R-F
A2R25	0698-3158	4		RESISTOR 23.7K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-2372-F
A2R26	1810-0203	5	1	NETWORK-RES 8-SIP 470.0 OHM X 7	11236	750-81-R470
A2R27	0698-3431	6	1	RESISTOR 23.7 1% .125W F TC=0+-100	03888	PM355-1/8-TO-23R7-F
A2R28	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1002-F
A2R29	0757-0439	4	1	RESISTOR 6.81K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-6811-F
A2R30	0757-0727	3		RESISTOR 562 1% .25W F TC=0+-100	24546	NAS-1/4-TO-562R-F
A2R31	1810-0541	4	1	NETWORK-RES 6-SIP MULTI-VALUE	28480	1810-0541
A2R32	1810-0219	3	1	NETWORK-RES 8-SIP 220.0 OHM X 4	11236	750-83-R220
A2R33	0757-0421	4		RESISTOR 825 1% .125W F TC=0+-100	24546	CT4-1/8-TO-825R-F
A2R34	0698-3443	0		RESISTOR 287 1% .125W F TC=0+-100	24546	CT4-1/8-TO-287R-F
A2R35	0698-3439	4		RESISTOR 178 1% .125W F TC=0+-100	24546	CT4-1/8-TO-178R-F
A2R36	0757-0317	7	1	RESISTOR 1.33K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1331-F
A2R37	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	CT4-1/8-TO-101-F
A2R38	0698-0082	7	2	RESISTOR 464 1% .125W F TC=0+-100	24546	CT4-1/8-TO-4640-F
A2R39	0757-0280	3	3	RESISTOR 1K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1001-F
A2R40	0757-0400	9	1	RESISTOR 90.9 1% .125W F TC=0+-100	24546	CT4-1/8-TO-90R9-F
A2R41	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	28480	0698-4037
A2R42	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	CT4-1/8-TO-4640-F
A2R43	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1002-F
A2R44	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1002-F
A2R45	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1002-F
A2R46	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	CT4-1/8-TO-101-F
A2R47	0757-0421	4		RESISTOR 825 1% .125W F TC=0+-100	24546	CT4-1/8-TO-825R-F
A2R48	0757-1108	6	1	RESISTOR 300 1% .125W F TC=0+-100	24546	CT4-1/8-TO-301-F
A2R49	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1001-F
A2R50	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1002-F

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2R51	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1001-F
A2R52	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1002-F
A2R53	0698-8827	4	2	RESISTOR 1M 1% .125W F TC=0+-100	28480	0698-8827
A2R54	0698-8827	4		RESISTOR 1M 1% .125W F TC=0+-100	28480	0698-8827
A2R55	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1002-F
A2R56	0757-0178	8	1	RESISTOR 100 1% .25W F TC=0+-100	24546	NA5-1/4-TO-101-F
A2R57	0757-0463	4	1	RESISTOR 82.5K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-8252-F
A2R58	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-TO-1002-F
A2R59	0757-0422	5	1	RESISTOR 909 1% .125W F TC=0+-100	24546	CT4-1/8-TO-909R-F
A2R60	0698-7200	5	1	RESISTOR 31.6 1% .05W F TC=0+-100	24546	C3-1/L8-TO-31R6-F
A2TP1	1251-0600	0	2	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A2TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	28480	1251-0600
A2U1	1820-1780	6	1	IC PRESCR ECL	07263	11C90DC
A2U2	1826-0139	9	1	IC OP AMP GP DUAL 8-DIP-P PKG	3L585	CA1458G
A2U3	1820-2823	0	2	IC GATE ECL/10KH NOR QUAD 2-INP	04713	MC10H102P
A2U4	1813-0215	5	2	IC WIDEBAND AMPL TO-39 PKG	04713	MWA220
A2U5	1813-0215	5		IC WIDEBAND AMPL TO-39 PKG	04713	MWA220
A2U6	1820-3075	6	1	IC RECEIVER ECL/10KH LINE RECEIVER TPL	04713	MC10H116L
A2U7	1813-0214	4	1	IC WIDEBAND AMPL TO-39 PKG	04713	MWA210
A2U8	1820-2823	0		IC GATE ECL/10KH NOR QUAD 2-INP	04713	MC10H102P
A2U9	1826-0346	0	1	IC OP AMP GP DUAL 8-DIP-P PKG	27014	LM358N
A2W1	05350-60103	9	1	CABLE ASSY- LOW FREQUENCY	28480	05350-60103

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	**05361-60003**	1	1	**COUNTER ASSEMBLY**	**28480**	**05361-60003**
A3C1	0160-4557	0	24	CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C2	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C3	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C4	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C5	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C6	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C7	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C8	0160-0576	5	2	CAPACITOR-FXD 0.1UF 50V	09969	RPE121-105X7R104M50V
A3C9	0160-4846	0	2	CAPACITOR-FXD 1500PF 100V	09969	RPA20C0G152J100VPT
A3C10	0160-0576	5		CAPACITOR-FXD 0.1UF 50V	09969	RPE121-105X7R104M50V
A3C11	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C12	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C13	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C14	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C15	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C16	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C17	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C18	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C19	0180-2929	8	1	CAPACITOR-FXD 68UF 10V TA	12344	T140B686K010AS
A3C20	0180-2690	0	2	CAPACITOR-FXD 3.3UF 15V TA	56289	150D335X9015A2
A3C21	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C22	0160-4846	0		CAPACITOR-FXD 1500PF 100V	09969	RPA20C0G152J100VPT
A3C23	0160-4808	4	1	CAP-FXD 470PF 100V	09969	RPA10C0G471J100V
A3C24	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C25	0160-4554	7	3	CAP-FXD 0.01UF 50V	09969	RPA10X7R103M50V
A3C26	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C27	0160-4799	2		CAPACITOR-FXD 2.2PF ±11.36% 100V CER COG	04222	MA101A222CAAH
A3C28	0160-4554	7		CAP-FXD 0.01UF 50V	09969	RPA10X7R103M50V
A3C29	0160-4554	7		CAP-FXD 0.01UF 50V	09969	RPA10X7R103M50V
A3C30	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C31	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C32	0180-2690	0		CAPACITOR-FXD 3.3UF 15V TA	56289	150D335X9015A2
A3C33	0165-4786	7	1	CAP-FXD 27PF 100V	09969	RPA10C0G270J100
A3C34	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C35	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C36	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3C37	0160-4557	0		CAPACITOR-FXD 0.1UF 50V	09969	RPA30X7R104M50V
A3CR1 – CR6	91901-0050	3	6	DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A3DL1	1810-0724	5	1	DELAY LINE ACTIVE DEVICE W/DUAL IN-LING	07393	LPSLDM-100
A3L1	9140-0537	5	1	INDUCTOR RF-CH-MLD 2.2UH +-5%	91637	IM-2 2.2UH 5%
A3L2	9100-1788	6	2	CORE-FERRITE CHOKE-WIDEBAND;IMP:>680	11214	LB2/2.5ZB
A3L3	9100-1788	6		CORE-FERRITE CHOKE-WIDEBAND;IMP:>680	11214	LB2/2.5ZB
A3P1	1251-7986	9	1	CONNECTOR-POST TYPE .100-PIN-SPCG 50-CONT	28480	1251-7986
A3R1	2100-3351	6	1	RESISTOR-TRMR 500 10% TKF SIDE-ADJ 1-TRN	28480	2100-3351
A3R2	0698-3446	3	5	RESISTOR 383 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-383R-F
A3R3	0698-3132	4	2	RESISTOR 261 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-2610-F
A3R4	0757-0418	9	3	RESISTOR 619 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-619R-F
A3R5	0757-0394	0	1	RESISTOR 51.1 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-51R-F
A3R6	0757-0280	3	5	RESISTOR 1K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1001-F
A3R7	0757-0438	3	3	RESISTOR 5.11K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-5111-F
A3R8	0757-1094	9	2	RESISTOR 1.47K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1471-F
A3R9	0757-0420	3	2	RESISTOR 750 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-751-F
A3R10	0757-0421	4	2	RESISTOR 825 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-825R-F
A3R11	0757-0465	6	2	RESISTOR 100 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1003-F
A3R12	0757-0442	9	3	RESISTOR 10K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1002-F
A3R13	0757-0438	3		RESISTOR 5.11K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-5111-F

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3R14	0698-3446	3		RESISTOR 383 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-383R-F
A3R15	0698-3151	7	1	RESISTOR 2.87K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-2871-F
A3R16	0757-0418	9		RESISTOR 619 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-619R-F
A3R17	0698-3159	5	2	RESISTOR 26.1K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-2612-F
A3R18	0698-3446	3		RESISTOR 383 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-383R-F
A3R19	0698-3132	4		RESISTOR 261 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-2610-F
A3R20	0698-0085	0	1	RESISTOR 2.61K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-2611-F
A3R21	0757-0422	5	1	RESISTOR 909 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-909R-F
A3R22	0757-0279	0	1	RESISTOR 3.16K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-3161-F
A3R23	0757-0416	7	2	RESISTOR 511 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-511R-F
A3R24	0698-0083	8	3	RESISTOR 1.96K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1961-F
A3R25	0698-0083	8		RESISTOR 1.96K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1961-F
A3R26	0757-0280	3		RESISTOR 1K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1001-F
A3R27	0698-3441	8	2	RESISTOR 215 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-215R-F
A3R28	0757-0280	3		RESISTOR 1K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1001-F
A3R29	0757-0438	3		RESISTOR 5.11K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-5111-F
A3R30	0757-1094	9		RESISTOR 1.47K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1471-F
A3R31	0757-0421	4		RESISTOR 825 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-825R-F
A3R32	0757-0420	3		RESISTOR 750 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-751-F
A3R33	0757-0465	6		RESISTOR 100K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1003-F
A3R34	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1002-F
A3R35	0757-0416	7		RESISTOR 511 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-511R-F
A3R36	0698-3159	5		RESISTOR 26.1 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-2612-F
A3R37	0698-3157	3	1	RESISTOR 19.6K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1962-F
A3R38	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1002-F
A3R39	0757-0280	3		RESISTOR 1K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1001-F
A3R40	0757-0418	9		RESISTOR 619 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-619R-F
A3R41	0698-3153	9	1	RESISTOR 3.83K +-1% .125TF TC=0+-100	12498	CT4-1/8-TO-3831-F
A3R42	0757-0400	9	2	RESISTOR 90.9 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-90R9-F
A3R43	0757-0280	3		RESISTOR 1K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1001-F
A3R44	0698-3437	2	2	RESISTOR 133 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-133R-F
A3R45	0757-0400	9		RESISTOR 90.9 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-90R9-F
A3R46	0698-3446	3		RESISTOR 383 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-383R-F
A3R47	0698-3437	2		RESISTOR 133 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-133R-F
A3R48	0698-3446	3		RESISTOR 383 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-383R-F
A3R49	0698-0083	8		RESISTOR 1.96K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1961-F
A3R50	0698-3438	3	1	RESISTOR 147 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-147R-F
A3R51	0698-3441	8		RESISTOR 215 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-215R-F
A3TP1	0360-0124	3	1	CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
A3U1	1813-0119	8	1	CLOCK OSCILLATOR XTAL 40-MHZ 0.01%	12703	K1100AM-40MHZ
A3U2	1820-2694	3	2	IC FF TTL F J-K NEG-EDGE-TRIG	18324	74F112N
A3U3	1826-0065	0	2	IC COMPARATOR PRCH 8-DIP-P PKG	27014	LM311N
A3U4	1858-0054	4	2	TRANSISTOR ARRAY 16-PIN PLASTIC DIP	28480	1858-0054
A3U5	1820-2312	2	1	IC MISC	28480	1820-2312
A3U6	1826-0346	0	1	IC OP AMP GP DUAL 8-DIP-P PKG	27014	LM358N
A3U7	1826-0393	7	1	IC V RGLTR-ADJ-POS 1.2/37V TO-220 PKG	27014	LM317T
A3U8	1820-3347	5	1	IC-20 MHZ PROGRAMMABLE INTERVAL TIMER	34649	P8254-2
A3U9	1820-2694	3		IC FF TTL F J-K NEG-EDGE-TRIG	18324	74F112N
A3U10	1826-0065	0		IC COMPARATOR PRCN 8-DIP-P PKG	27014	LM311N
A3U11	1858-0054	4		TRANSISTOR ARRAY 16-PIN PLASTIC DIP	28480	1858-0054
A3U12	1820-2962	8	1	IC GATE ECL/10KH OR QUAD 2-INP	04713	MC10H103P
A3U13	1820-3225	8	1	IC MUXR/DATA-SEL TTL F 8-TO-1-LINE	18324	74F251N
A3U14	1820-2695	4	1	IC MUXR/DATA-SEL TTL F 2-TO-1 LINE QUAD	18324	74F158N
A3U15	1820-2776	2	1	IC COUNTER TTL ALS DECD SYNCHRO	01295	SN74ALS160BN
A3XU5	1200-0654	7	1	SOCKET-IC DIP 40-CONT DIP DIP-SLDR	01295	C8740-01
	0361-0685	3	1	RIVET-BLIND DR-PIN RNDH .125DIA	02768	231-080551-05-0101
	0403-0026	6	1	PLUG-HOLE BDR-HD FOR .19-D HOLE NYLON	02768	207-120241-03-0101
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	73957	GP24-063 X 250-17
	4040-0748	3	2	EXTR-PC BD BLK POLYC .062-IN-BD-THKNS	28480	4040-0748

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	**05350-60023**	**2**	**1**	**MICROPROCESSOR BOARD (STANDARD) SERIES 3049**	**28480**	**05350-60023**
A4	**05350-60024**	**3**	**1**	**MICROPROCESSOR BOARD (OPTION 700) SERIES 3049**	**28480**	**05350-60024**
				NOTE A4U8 AND A4U9 ARE NOT SUPPLIED WITH THE A4 MICROPROCESSOR BOARD. THEY MUST BE ORDERED SEPARATELY.		
C1	0160-4787	8	2	CAPACITOR-FXD 22PF +-5% 100WVDC CER	04222	SA102A220JAAH
C2	0160-4787	8		CAPACITOR-FXD 22PF +-5% 100WVDC CER	04222	SA102A220JAAH
C3	0160-4557	0	20	CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C4	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C5	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C6	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C7	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C8	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C9	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C10	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C11	0180-3770	9	1	CAPACITOR-FXD 2.2UF +-10% 35V TA	56289	299D225X9035BB1
C12	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C13	0160-4806	4	1	CAPACITOR-FXD 470PF +-5% 100VDC CER	04222	SA101A471JAAH
C14	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C15	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C16	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C17	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C18	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C19	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C20	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C21	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C22	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C23	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C24	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C25	0180-3775	4	2	CAPACITOR-FXD 68UF +-10% 10V TA	56289	299D686X9010DB1
C26	0180-3775	4		CAPACITOR-FXD 68UF +-10% 10V TA	56289	299D686X9010DB1
CR1	1901-0050	3	3	DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
J1	1251-4775	8	1	CONNECTOR POST-TYPE .150-PIN SPCG 10-CONT	00779	87221-9
L1	9100-0541	7	1	INDUCTOR RF-CH-MLD 250UH +-10%	04213	1670-1
L2	9140-0990		1	INDUCTOR 1UH +-10% .172D-INX .43LG-IN	99800	1641-102
MP1	1480-0116	8	2	PIN-GROOVE .062-IN-DIA .25-IN-LG STL	73957	GP24-063 X 250-17
MP2	4040-0748	3	2	EXTRACTOR- PC BOARD BLACK	28480	4040-0748
P1A	1251-7986	9	2	CONNECTOR-POST-TYPE .100-PIN SPCG 50-CONT	00779	534204-1
P1B	1251-7986	9		CONNECTOR-POST-TYPE .100-PIN SPCG 50-CONT	00779	534204-1
R1	0698-3157	3	3	RESISTOR 19.6K +-1% .125W TF TC=0+-100	19701	SF425H
R2	8159-0005	0	3	RESISTOR- ZERO-OHM 22AWG	28480	8159-0005
R3	8159-0005	0		RESISTOR- ZERO-OHM 22AWG	28480	8159-0005
R4	0757-0442	9	6	RESISTOR 10K +-1% .125W TF TC=0+-100	19701	SF425H
R5	8159-0005	0		RESISTOR- ZERO-OHM 22AWG	28480	8159-0005
R6	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	19701	SF425H
R7	1810-0398	9	1	RESISTOR 10-SIP 22K-OHM	11236	750-101
R8	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	19701	SF425H
R9	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	19701	SF425H
R10	0698-3157	3		RESISTOR 19.6K +-1% .125W TF TC=0+-100	19701	SF425H
R11	0698-3157	3		RESISTOR 19.6K +-1% .125W TF TC=0+-100	19701	SF425H
R12	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	19701	SF425H
R13	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	19701	SF425H
U1	1820-3159	7	1	IC MPU W/2 MHZ CLOCK 8-BITS 64K ADDRESS	04713	MC68B03L
U2	1810-0758	5	1	DELAY LINE 14-DIP	28480	1810-0758
U3	1820-2684	1	1	IC GATE TTL/F NAND QUAD 2-INP	18324	74F00N

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U4	05361-80009	9	1	ADDRESS DECODER	28480	05361-80009
U5	1820-2488	3	1	IC-FF TTL/ALS D-TYPE POS-EDGE TRIG	01295	SN74ALS74AN
U6	1820-3121	3	1	IC TRANSCEIVER TTL/ALS BUS OCTL	01295	SN74ALS245AN
U7	1820-2724	0	6	IC LCH TTL/ALS TRANSPARENT OCTL	01295	SN74ALS573CN
U8	05350-80029		1	EPROM	28480	05350-80029
U9	1820-3415		1	IC-TIMER MODULE (OPT 700 ONLY)	28480	1820-3415
U10	1818-3185	4	1	IC-CMOS 65536 (64K) STAT RAM 120-NS 3-S	S4013	HM6264ALP-12L
U11	1820-2724	0		IC LCH TTL/ALS TRANSPARENT OCTL	01295	SN74ALS573CN
U12	1820-3100	8	1	IC DECODER TTL/ALS BIN 3-TO-8-LINE 3-INP	01295	SN74ALS138N
U13	1820-2757	9	4	IC FF TTL/ALS D-TYPE POS-EDGE-TRIG COM	01295	SN74AALS574BN
U14	1820-2757	9		IC FF TTL/ALS D-TYPE POS-EDGE-TRIG COM	01295	SN74AALS574BN
U15	1820-2757	9		IC FF TTL/ALS D-TYPE POS-EDGE-TRIG COM	01295	SN74AALS574BN
U16	1820-2757	9		IC FF TTL/ALS D-TYPE POS-EDGE-TRIG COM	01295	SN74AALS574BN
U17	1820-2724	0		IC LCH TTL/ALS TRANSPARENT OCTL	01295	SN74ALS573CN
U18	1820-2724	0		IC LCH TTL/ALS TRANSPARENT OCTL	01295	SN74ALS573CN
U19	1820-2724	0		IC LCH TTL/ALS TRANSPARENT OCTL	01295	SN74ALS573CN
U20	1820-2724	0		IC LCH TTL/ALS TRANSPARENT OCTL	01295	SN74ALS573CN
XU8	1200-0567	1	1	SOCKET-IC 28-PIN DIP DIP-SLDR	09922	DILB28P-308T
Y1	0410-1386	8	1	CRYSTAL- QUARTZ 8MHZ HC-49/8-HLDR	28480	0410-1386

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5	**05350-60018**	**5**	**1**	**SYNTHESIZER ASSEMBLY (SERIES 3049)**	**28480**	**05350-60018**
A5C1	0170-0066	9	1	CAPACITOR-FXD 0.027UF 200V POLYE-FL	19701	708D1HJ273PK201AX
A5C2	0160-3879	7	19	CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C3	0160-4040	6	8	CAPACITOR-FXD 1000PF 100 V	09969	RPE121-105COG102J100V
A5C4	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C5	0180-4132	9	5	CAPACITOR-FXD 6.8UF +-10% 35V TA	12340	T322D685K035AS
A5C6	0180-0210	6	4	CAPACITOR-FXD 3.3UF 15V TA	56289	150D335X0015A2
A5C7	0180-4135	2	7	CAPACITOR-FXD 33UF +-10% 10V TA	12340	T322D336K010AS
A5C8	0160-4040	6		CAPACITOR-FXD 1000PF 100 V	09969	RPE121-105COG102J100V
A5C9	0180-0210	6		CAPACITOR-FXD 3.3UF 15V TA	56289	150D335X0015A2
A5C10	0160-0576	5	1	CAPACITOR-FXD 0.1UF 50V	09969	RPE121-105X7R104M50V
A5C11	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C12				NOT ASSIGNED		
A5C13	0160-4040	6		CAPACITOR-FXD 1000PF 100 V	09969	RPE121-105COG102J100V
A5C14	0160-4389	6	14	CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V
A5C15				NOT ASSIGNED		
A5C16	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C17	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C18	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C19	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C20	0160-4389	6		CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V
A5C21				NOT ASSIGNED		
A5C22				NOT ASSIGNED		
A5C23				NOT ASSIGNED		
A5C24	0180-4132	9		CAPACITOR-FXD 6.8UF +-10% 35V TA	12340	T322D685K035AS
A5C25	0180-4132	9		CAPACITOR-FXD 6.8UF +-10% 35V TA	12340	T322D685K035AS
A5C26	0180-4132	9		CAPACITOR-FXD 6.8UF +-10% 35V TA	12340	T322D685K035AS
A5C27	0180-1731	8	1	CAPACITOR-FXD 4.7UF 50V TA	56289	150D475X9050B2
A5C28	0160-4040	6		CAPACITOR-FXD 1000PF 100 V	09969	RPE121-105COG102J100V
A5C29	0160-4481	9	1	CAPACITOR-FXD 270PF 100V	09969	RPE121-105COG271J100V
A5C30	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C31	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C32				NOT ASSIGNED		
A5C33	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C34	0180-4135	2		CAPACITOR-FXD 33UF +-10% 10V TA	12340	T322D336K010AS
A5C35	0160-4040	6		CAPACITOR-FXD 1000PF 100 V	09969	RPE121-105COG102J100V
A5C36	0160-4040	6		CAPACITOR-FXD 1000PF 100 V	09969	RPE121-105COG102J100V
A5C37	0160-3874	2	1	CAPACITOR-FXD 0F 200V	09969	RPE121-105COG100D200V
A5C38				NOT ASSIGNED		
A5C39	0170-0019	2	1	CAPACITOR-FXD 0.1UF 200V POLYE-FL	19701	708OD1MR104PJ201AX
A5C40	0180-4135	2		CAPACITOR-FXD 33UF +-10% 10V TA	12340	T322D336K010AS
A5C41	0180-4135	2		CAPACITOR-FXD 33UF +-10% 10V TA	12340	T322D336K010AS
A5C42	0180-4135	2		CAPACITOR-FXD 33UF +-10% 10V TA	12340	T322D336K010AS
A5C43	0180-0210	6		CAPACITOR-FXD 3.3UF 15V TA	56289	150D335X0015A2
A5C44	0160-4527	4	1	CAPACITOR-FXD 56PF +-5% 200V CER COG	12340	C320C560J2G5CA
A5C45	0160-4492	2	1	CAPACITOR-FXD 18PF 200V	09969	RPE121-105COG180J200V
A5C46	0160-4040	6		CAPACITOR-FXD 1000PF 100 V	09969	RPE121-105COG102J100V
A5C47	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C48	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C49	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C50	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C51				NOT ASSIGNED		
A5C52				NOT ASSIGNED		
A5C53	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C54	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C55	0160-4389	6		CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V
A5C56	0160-4389	6		CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V
A5C57	0160-4389	6		CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V
A5C58	0180-4135	2		CAPACITOR-FXD 33UF +-10% 10V TA	12340	T322D336K010AS
A5C59	0160-4389	6		CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V
A5C60	0160-4389	6		CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5C61	0180-4132	9		CAPACITOR-FXD 6.8UF +-10% 35V TA	12340	T322D685K035AS
A5C62	0180-4135	2		CAPACITOR-FXD 33UF +-10% 10V TA	12340	T322D336K010AS
A5C63	0160-4389	6		CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V
A5C64	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C65	0160-4389	6		CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V
A5C66	0160-4389	6		CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V
A5C67	0160-4040	6		CAPACITOR-FXD 1000PF 100 V	09969	RPE121-105C0G102J100V
A5C68	0160-4389	6		CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V
A5C69	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C70	0160-4389	6		CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V
A5C71	0180-0210	6		CAPACITOR-FXD 3.3UF 15V TA	56289	150D335X0015A2
A5C72	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X4103M100V
A5C73	0160-4389	6		CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V
A5C74	0160-4389	6		CAPACITOR-FXD 100PF 200V	09969	RP3121-105C0G101J200V
A5CR1	1901-0050	3	11	DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A5CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A5CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A5CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A5CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A5CR6	1901-0734	0	1	DIODE-PWR RECT 1N5818 30V 1A	04713	1N5858
A5CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A5CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A5CR9	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A5CR10	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A5CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A5CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A5CR13	0122-0161	4	1	DIODE-VVC 2.15PF 7% BVR=30V	25403	BB405B
A5DS1	1990-1022	8	1	LED-LAMP LUM-INT=4MCD IF=25MA-MAX BVR=5V	28480	HLMP-5030
A5J2	1250-1314	3	1	CONNECTOR-RF SM-SLD FEM PC 50-OHM	98291	52-054-0000-226
A5L1	9140-0906	2	4	INDUCTOR 1MH +-10% .172D-INX.43LG-IN	04099	9250-105
A5L2	9140-0906	2		INDUCTOR 1MH +-10% .172D-INX.43LG-IN	04099	9250-105
A5L3	9140-0906	2		INDUCTOR 1MH +-10% .172D-INX.43LG-IN	04099	9250-105
A5L4	9140-0906	2		INDUCTOR 1MH +-10% .172D-INX.43LG-IN	04099	9250-105
A5L5	9100-0541	7	2	INDUCTOR RF-CH-MLD 250UG +-10%	91637	ICS-1041-1
A5L6	9100-0541	7		INDUCTOR RF-CH-MLD 250UG +-10%	91637	ICS-1041-1
A5L7	9100-0654	3	1	CORE-FERRITE CHOKE-WIDEBAND;IMP:>800	02114	VK200 21/48
A5L8	9100-2258	7	5	INDUCTOR RF-CH-MLD 1.2UH +-10%	91637	IM-2 1.2UH 10%
A5L9	9100-2258	7		INDUCTOR RF-CH-MLD 1.2UH +-10%	91637	IM-2 1.2UH 10%
A5L10	9135-0076	6	1	INDUCTOR RF-CH-MLD 39NH +-6%	06560	010150-054J
A5L11	9100-2258	7		INDUCTOR RF-CH-MLD 1.2UH +-10%	91637	IM-2 1.2UH 10%
A5L12	9100-2258	7		INDUCTOR RF-CH-MLD 1.2UH +-10%	91637	IM-2 1.2UH 10%
A5L13	9100-2258	7		INDUCTOR RF-CH-MLD 1.2UH +-10%	91637	IM-2 1.2UH 10%
A5MP1	5000-9043	6	1	PIN EXTRACTOR	28480	5000-9043
A5MP2	5040-6852	3	1	EXTRACTOR-ORN	28480	5040-6852
A5MP3	05350-00014	5	1	GROUND STRAP-RIG	28480	05350-00014
A5MP4	05350-00015	6	1	GROUND STRAP, LEFT	28480	05350-00015
A5MP5	1205-0316	8	1	HEAT SINK SGL TO-5/TO-39-CS	13103	2260C
A5MP6	1205-0554	6	2	HEAT SINK SGL DIP	30161	5802B
A5P1	1251-7986	9	1	CONN-POST TYPE .100-PIN SPCG 50-CONT	28480	1251-7986
A5Q1				NOT ASSIGNED		
A5Q2				NOT ASSIGNED		
A5Q3	1854-0215	1	2	TRANSISTOR NPN SI TO-92 PD=350MW	04713	2N3904
A5Q4	1853-0036	2	3	TRANSISTOR PNP SI TO-92 PD=625MW	04713	2N3906(SEL)
A5Q5	1853-0036	2		TRANSISTOR PNP SI TO-92 PD=625MW	04713	2N3906(SEL)
A5Q6	1854-0591	6	1	TRANSISTOR NPN SI PD=180MW FT=4 GHZ	03334	BFR90
A5Q7	1854-0345	8	1	TRANSISTOR NPN 2N5179 SI TO-72 PD=200MW	02037	2N5179
A5Q8				NOT ASSIGNED		
A5Q9				NOT ASSIGNED		

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R1	0757-0442	9	3	RESISTOR 10K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1002-F
A5R2	0698-3155	1	1	RESISTOR 4.64K +-1% .125W F TC-0+-100	12482	CT4-1/8-TO-4641-F
A5R3	0698-3156	2	2	RESISTOR 14.7K +-1% .125W F TC=0+-100	12482	CT4-1/8-TO-1472-F
A5R4	0757-0279	0	3	RESISTOR 3.16K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-3161-F
A5R5	0698-3454	3	2	RESISTOR 215K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-2153-F
A5R6	0698-0084	9	2	RESISTOR 2.15K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-2151-F
A5R7	0698-0084	9		RESISTOR 2.15K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-2151-F
A5R8	1810-0478	6	1	NETWORK RES 8-SIP 22.0K OHM X 4	32997	4308R-102-223
A5R9	0757-0420	3	1	RESISTOR 750 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-751-F
A5R10	0757-0317	7	2	RESISTOR 1.33K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1331-F
A5R11	0757-0279	0		RESISTOR 3.16K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-3161-F
A5R12				NOT ASSIGNED		
A5R13	1810-0488	8	1	NETWORK-RESIS 8-SIP 4.7K OHM X 4	32997	4308R-102-472
A5R14	0757-0401	0	1	RESISTOR 100 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-101-F
A5R15	0698-0082	7	1	RESISTOR 464 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-4640-F
A5R16	0698-3454	3		RESISTOR 215K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-2153-F
A5R17	1810-0406	0	1	NETWORK RES 8-SIP 10.0K OHM X 4	32997	4308R-102-103
A5R18	0698-3162	0	1	RESISTOR 46.4K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-4642-F
A5R19	1810-0398	9	1	NETWORK-RES 10-SIP 22.0K OHM X 9	C1433	750-101
A5R20	0698-3152	8	1	RESISTOR 3.48K +-1% .125W TF TC=0+-100	12498	CTR-1/8-TO-1002-F
A5R21	0757-0279	0		RESISTOR 3.16K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-3161-F
A5R22	0757-0465	6	3	RESISTOR 100K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1003-F
A5R23	0757-0317	7		RESISTOR 1.33K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1331-F
A5R24	0698-3444	1	1	RESISTOR 316 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-316R-F
A5R25	2100-3352	7	1	RESISTOR-TRMR 1K 10% TKD SIDE-ADJ 1-TRN	28480	2100-3352
A5R26	0757-0465	6		RESISTOR 100K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1003-F
A5R27	0698-3441	8	1	RESISTOR 215 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-215R-F
A5R28	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1002-F
A5R29	1810-0445	7	3	NETWORK-RES 6-SIP 100.0 OHM X 3	32997	4306R-102-101
A5R30	1810-0445	7		NETWORK RES 6 SIP 100.0 OHM X 3	06252	750-63-R100
A5R31	1810-0203	5	1	NETWORK-RES 8-SIP 470.0 OHM X 7	C1433	750-81
A5R32	1810-0708	5	1	NETWORK-RES 6-SIP 1.5K OHM X 5	C1433	750-61
A5R33	1810-0445	7		NETWORK RES 6-SIP 100.0 OHM X 3	06252	750-63-R10001
A5R34	1810-0445	7		NETWORK-RES 6-SIP 100.0 OHM X 3	32997	4306R-102-101
A5R35	0757-0395	1	2	RESISTOR 56.2 +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-56R2-F
A5R36	0757-0395	1		RESISTOR 56.2 +-1% .125W TF TC=0+-100	12498	C54-1/8-TO-56R2-F
A5R37	0698-0084	9		RESISTOR 2.15K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-2151-F
A5R38	0757-0283	6	1	RESISTOR 2K +-1% .125W TF TC=0+-100	12498	CT4-1/8-GO-2001-F
A5R39				NOT ASSIGNED		
A5R40	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0+-100	12482	CT4-1/8-TO-5111-F
A5R41	0757-0465	6		RESISTOR 100K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1003-F
A5TP1	1251-0600	0	5	CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	12360	94-155-1010-01-03-00
A5TP2	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	12360	94-155-1010-01-03-00
A5TP3	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	12360	94-155-1010-01-03-00
A5TP4	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	12360	94-155-1010-01-03-00
A5TP5	1251-0600	0		CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ	12360	94-155-1010-01-03-00
A5U1	1826-0371	1	1	IC OP AMP LOW-BIAS H-IMPD 8-PIN TO-99	27014	LF256N
A5U2	1826-0412	1	1	IC-COMPARATOR PRCN DUAL 8-DIP-P PKG	27014	LM393N
A5U3	1820-3405	6	1	IC MISC CMOS 4-BIT	04713	MC145146P
A5U4	1820-2724	0	1	IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
A5U5	1826-1099	2	1	IC V RGLTR-ADJ NEG TO-92 PKG	27014	LM337LZ
A5U6	1826-0372	2	1	IC MISC 8-DIP-P PKG	28480	A251-0100
A5U7	1820-1383	5	1	IC CNTR ECL BDC POS-EDGE-TRIG	04713	MC10138L
A5U8	1820-3340	8	1	IC GATE ECL/10KH OR-AND-INV	04713	MC10H121P
A5U9	1813-0213	3	1	IC WIDEBAND AMPL TO-39 PKG	04713	MWA130
A5U10	1820-1888	5	1	IC PRESCR ECL	04713	MC12013L
A5W1	8159-0005	0	2	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	11502	YZ0 1/4
A5W2	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	11502	YZ0 1/4

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6R1	1810-0366	1	2	NETWORK-RES 6-SIP 220.0 OHM X 5	C1433	750-61
A6R2	1810-0370	7	1	NETWORK-RES 8-SIP 220.0 OHM X 7	C1433	750-81
A6R3	0698-7203	8	4	RESISTOR 42.2 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-42R2-F
A6R4	0698-7203	8		RESISTOR 42-2 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-42R2-F
A6R5	0698-7251	6	1	RESISTOR 4.22K ±1 %.05W TF TC=0±100	12498	C3-1/8-TO-4221-F
A6R6	0698-7253	8	2	RESISTOR 5.1 1K ±1%.05W TF TC=04-100	12498	C3-1/8-TO-51 1 1-F
A6R7	1810-0447	9	1	NETWORK-RES 8-SIP 68.0 OHM X 4	32997	4308R-102-680
A6R8	0698-7239	0	1	RESISTOR 1.33K ±1 %.05W TF TC=0±100	12498	C3-1/8-TO-1331-F
A6R9	0698-7244	7	2	RESISTOR 2.15K ±1%.05W TF TC=0±100	12498	C3-1/8-TO-2151-F
A6R10	0698-7205	0	2	RESISTOR 51.1 ±1%.05W TF TC=0±1 00	12498	C3-1/8-TO-51R1-F
A6R11	0698-7222	1	2	RESISTOR 261 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-261R-F
A6R12	0698-7219	6	1	RESISTOR 196 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-196R-F
A6R13	0698-7203	8		RESISTOR 42.2 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-42R2-F
A6R14	0698-7222	1		RESISTOR 261 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-261R-F
A6R15	0698-3441	8	2	RESISTOR 215 ±1%.125W TF TC=0±100	12498	CT4-1/8-TO-215R-F
A6R16	0698-7198	0	2	RESISTOR 26.1 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-26R1-F
A6R17	0698-7198	0		RESISTOR 26.1 ±1%.05WTF TC=0±100	12498	C3-1/8-TO-26R1-F
A6R18	0698-3441	8		RESISTOR 215 ±1%.125W TF TC=0±100	12498	CT4-1/8-TO-215R-F
A6R19	0698-7212	9	3	RESISTOR 100 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-100R-F
A6R20	0698-7212	9		RESISTOR 100 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-100R-F
A6R21	0699-0071	6	1	RESISTOR 4.64M ±1%.125W TF TC=0±100	19701	5033R
A6R22				NOT ASSIGNED		
A6R23	0698-7266	3	2	RESISTOR 17.8K ±1 %.05W TF TC=0±100	12498	C3-1/8-TO-1782-F
A6R24	0698-7203	8		RESISTOR 42.2 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-42R2-F
A6R25	0698-7209	4	2	RESISTOR 75 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-75R0-F
A6R26	0698-7208	3	2	RESISTOR 68.1 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-68R1-F
A6R27	0698-7208	3		RESISTOR 68.1 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-68R1-F
A6R28	0698-7209	4		RESISTOR 75 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-75R0-F
A6R29	0698-7240	3	1	RESISTOR 1.47K ±1 %.05W TF TC=0±100	12498	C3-1/8-TO-1471-F
A6R30	0698-7241	4	1	RESISTOR 1.62K ±1%.05W TF TC=0±lOO	12498	C3-1/8-TO-1621-F
A6R31	1810-0366	1		NETWORK-RES 6-SIP 220.0 OHM X 5	C1433	750-61
A6R32	0698-7192	4	2	RESISTOR 14.7 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-14R7-F
A6R33	0698-7188	8	1	RESISTOR 10 ±1 %.05W TF TC=0±100	12498	C3-1/8-TO-10R-F
A6R34	0698-7192	4		RESISTOR 14.7 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-14R7-F
A6R35	0698-3438	3	1	RESISTOR 147 ±1%.125W TF TC=0±100	12498	CT4-1/8-TO-147R-F
A6R36	0698-7248	1	2	RESISTOR 3.16K 1%.05W TF TC=0±100	19701	5063J
A6R37				NOT ASSIGNED		
A6R38	1810-0374	1	1	NETWORK-RES 8-SIP 1.0K OHM X 4	32997	4308R- 1 02-102
A6R39	0698-7267	4	1	RESISTOR 19.6K ±1 % .05W TF TC=0±100	12498	C3-1/8-TO-1962-F
A6R40	0698-7280	1	1	RESISTOR 68.1 K ±1 %.05W TF TC=0±100	12498	C3-1/8-TO-6812-F
A6R41				NOT ASSIGNED		
A6R42	2100-3749	6	1	RESISTOR-TRMR 5K 10% TKF SIDE-ADJ 17-TRN	09969	3105X502
A6R43	0698-7200	5	1	RESISTOR 31.6 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-31R6-F
A6R44				NOT ASSIGNED		
A6R45				NOT ASSIGNED		
A6R46				NOT ASSIGNED		
A6R47	1810-0368	3	2	NETWORK-RES 6-SIP 10.0K OHM X 5	C1433	750-61
A6R48	0698-7248	1		RESISTOR 3.16K ±1 %.05W TF TC=0±100	12498	C3-1/8-TO-3161-F
A6R49	0698-7236	7	1	RESISTOR 1 K ±1 %.05W TF TC=0±100	12498	C3-1/8-TO-1001-F
A6R50	0698-7235	6	1	RESISTOR 909 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-909R-F
A6R51	0698-7221	0	1	RESISTOR 237 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-237R-F
A6R52	0699-2024	3	1	RESISTOR 215K ±1%.05W TF TC=0±100	2M627	CRB20
A6R53	0698-7269	6	1	RESISTOR 23.7K ±1%.05W TF TC=0±100	12498	C3-1/8-TO-2372-F
A6R54	0698-7266	3		RESISTOR 17.8K ±1%.05W TF TC=0±100	12498	C3-1/8-TO-1782-F
A6R55	1810-0406	0	1	NETWORK-RES 8-SIP 1 0.0K OHM X 4	32997	430BR-102-103
A6R56	0698-7271	0	1	RESISTOR 28.7K ±1%.05W TF TC=0±100	12498	C3-1/8-TO-2872-F
A6R57	0699-0981	7	1	20.5K ±1%.05W TF TC=0±100	12498	C3-1/8-TO-2050-F
A6R58	0698-7262	9	1	RESISTOR 12.1K ±1%.05W TF TC=0±100	12498	C3-1/8-TO-1212-F
A6R59	0699-0070	5	1	RESISTOR 3.16M 1%.125W TF TC=0±100	91637	CMF-55
A6R60	1810-0934	9	1	NETWORK RESISTOR 8-SIP 56.0K OHM X 4	12515	08-R-102-563

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A6R61	0698-7252	7	1	RESISTOR 4.64K:T1 %.05W TF TC=0±100	12498	C3-1/8-TO-4641-F
A6R62	0698-7253	8		RESISTOR 5.1 1 K ±1 %.05W TF TC=0±100	12498	C3-1/8-TO-51 1 1 -F
A6R63	0698-7260	7	1	RESISTOR 1 0K ±1 %.05W TF TC=0±100	12498	C3-1/8-TO-1002-F
A6R64	0698-8826	3	1	RESISTOR 825K 1%.12SWTFTC=0±100	91637	CMF-55-1
A6R65	1810-0368	3		NETWORK-RES 6-SIP 10.0K OHM X 5	C1433	750-61
A6R66				NOT ASSIGNED		
A6R67	0698-7205	0		RESISTOR 51.1 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-51R1-F
A6R68	0698-7244	7		RESISTOR 2.15K ±1%.05W TF TC=0-100	12498	C3-1/8-TO-2151-F
A6R69	0698-7212	9		RESISTOR 100 ±1%.05W TF TC=0±100	12498	C3-1/8-TO-100R-F
A6R70	0699-0073	8	1	RESISTOR 10.0M 1%.125W TF TC=0±100	28480	0699-0073
A6TP1 - TP3	0360-0124	3	3	CONNECTOR-SGL CONT PIN.04-IN-BSC-SZ RND	28480	0360-0124
A6U 1	1826-1378	0	3	IC COMPARATOR HS DUAL 16-DIP-C PKG	34335	AM6687DL
A6U2	1820-2860	5	1	IC LCH ECL/10KH D-TYPE POS-EDGE-TRIG COM	04713	MC10H130P
A6U3				NOT ASSIGNED		
A6U4	1826-1378	0		IC COMPARATOR HS DUAL 16-DIP-C PKG	34335	AM6687DL
A6U5	1858-0133	0	2	TRANSISTOR ARRAY 16-PIN PLSTC DIP	34371	CA3227E
A6U6	1858-0133	0		TRANSISTOR ARRAY 16-PIN PLSTC DIP	34371	CA3227E
A6U7	1826-1378	0		IC COMPARATOR HS DUAL 16-DIP-C PKG	34335	AM6687DL
A6U8	1826-1440	7	1	SAMPLE AND HOLD 8 -DIP-P	27014	LF39BAN
A6U9	1826-0360	8	1	IC COMPARATOR GP QUAD 16-DIP-P PKG	04713	MC3431 P
A6U10	1826-1920	8	2	IC RF/IF AMPL WB 8-DIP-P PKG	18324	NE5204N
A6U11	1820-3437	4	1	IC BFR TTL ALS NON-INV HEX	01295	SN74ALS1035N
A6U12	1826-0772	6	1	IC V RGLTR-ADJ-POS 1.2/32V TO-92 PKG	04713	LM317LZ
A6U13	1826-0161	7	1	IC OP AMP GP QUAD 14-DIP-P PKG	27014	LM324N
A6U14	1826-0544	0	1	IC V RGLTR-V-REF-FXD 2.5V 8-DIP-C PKG	34333	SG3503Y
A6U15	1826-1920	8		IC RF/IF AMPL WB 8-DIP-P PKG	18324	NE5204N
A6U16	5088-7078	7	1	VARIABLE PI ATTN	28480	5088-7078
A6U17	1820-6421	2	1	IC MV CMOST74HC MONOSTBL RETRIG DUAL	18324	74HC4538N
A6U18	1820-2923	1	1	IC GATE CMOSF74HC NAND TPL 3-INP	04713	MC74HC10N
A6U19	1820-1440	5	1	IC LCH T-RL LS QUAD	01295	SN74LS279AN
A6W1	1251-4682	6	1	CONN-POST TYPE.100-PIN-SPCG 3-CONT	28480	1251-4682
A4W2	8120-5253	9	1	CABLE-ASSY-COAX 28480 81	0-5253	
A6W2	1250-1368	7	1	CONNECTOR-RF SMB M PC 50-OHM	98291	51-053-0129
	0520-0127	6	2	SCREW-MACH 2-56.188-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	05305-00010	6	1	CLAMP-GRNDING	28480	05305-00010
	05350-00014	5	1	GROUND STRAP-RIG	28480	05350-00014
	05350-00015	6	1	GND STRAP-LEFT	28480	05350-00015
	0610-0001	6	2	NUT-HEX-DBL-CHAM 2-56-THD.062-IN-THK	00000	ORDER BY DESCRIPTION
	1258-0141	8	1	JUMPER-REMOVABLE FOR 0.025 IN SQ PINS	00779	530153-2
	2190-0014	1	2	WASHER-LK INTL T NO. 2.089-IN-ID	78189	1902-00-00-2580
	5000-9043	6	1	PIN EXTRACTOR	28480	5000-9043
	5040-6852	3	1	EXTRACTOR-ORN	28480	5040-6852

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7	**05361-60007**	**5**	**1**	**KEYBOARD ASSEMBLY**	**28480**	**05361-60007**
A7DS1	1990-0486	6	1	LED-LAMP LUM-INT=2MCD IF=25MA=MAX BVR=5V	28480	HLMP-1301
A7J3	1200-0607	0	1	SOCKET-IC DIP 16-CONT DIP-DKP-SLDR	01295	C8716-01
A7J4	1252-0293	9	1	CONNECTOR POST-TYPE 4-CONT	28480	1252-0293
A7L1	9100-1788	6	2	CORE-FERRITE CHOKE-WIDEBAND;IMP:>680	11214	LB2/2.5ZB
A7L2	9100-1788	6		CORE-FERRITE CHOKE-WIDEBAND;IMP:>680	11214	LB2/2.5ZB
A7MP3	4040-1615	5	1	STANDOFF-LED .196-IN-WD .196-IN-LG BLK	28480	4040-1615
A7MP4	3131-0496	0	1	ACTUATOR-ROCKER SWITCH CHINA WHITE	10454	AT496CW
A7R5	1810-0690	4	1	NETWORK RESISTOR 6-SIP 22.0K OHM X 5	C1433	750-61
A7S1	3101-2713	5	1	SWITCH-ROCKER SIG-SW SPDT .02A 20VDC PC	10454	A12KB
A7U1	1820-3437	4	1	IC BFR TTL ALS NON-INV HEX	01295	SN74AS1035N
A7U2	1820-3270	3	1	IC GATE TTL ALS NAND QUAD 2-INP	01295	SN74ALS03BN
A7U3	1820-3638	7	1	IC BFR TTL ALS INV OCTL	01295	SN74ALS466AN
A7U4	1820-2309	7	1	IC ENCODER CMOS	27014	MM74C923N
A7U5	1820-2488	3	1	IC FF TTL ALS D-TYPE POS-EDGE-TRIG	01295	SN74ALS74AN
	5060-9436	7	20	SWITCH-PUSHBUTTON SPST NO-MOM	71468	5060-9436
	5041-0376	6	3	KEYCAP-BLANK	28480	5041-0376
	5041-4752	0	4	KEYCAP-FR GRAY	28480	5041-4752
	5041-4755	3	1	KEY CAP-FG#1	28480	5041-4755
	5041-4756	4	1	KEYCAP-FG#2	28480	5041-4756
	5041-4757	5	1	KEY CAP-FG#3	28480	5041-4757
	5041-4758	5	1	KEY CAP-FG#4	28480	5041-4758
	5041-4759	7	1	KEY CAP-FG#5	28480	5041-4759
	5041-4760	0	2	KEY CAP-FG#6,9	28480	5041-4760
	5041-4761	1	1	KEY CAP-FG#7	28480	5041-4761
	5041-4762	2	1	KEY CAP-FG#8	28480	5041-4762
	5041-4763	3	1	KEY CAP-FG#0	28480	5041-4763
	5041-4764	4	1	KEY CAP-FG .	28480	5041-4764
	5041-4765	5	1	KEY CAP +/-	28480	5041-4765
	5041-4766	6	1	SEQCHQHT-FGE	28480	5041-4766

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8	**05361-60008**	**6**	**1**	**MOTHERBOARD ASSEMBLY**	**28480**	**05361-60008**
A8C1	0180-3813	1	2	CAPACITOR-FXD 10UF 10 V TA	12344	T398C106K010AS
A8C2	0180-3813	1		CAPACITOR-FXD 10UF 10 V TA	12344	T398C106K010AS
A8C3	0180-3485	3	1	CAPACITOR-FXD 6300UF 40 V AL-ELCTLT	19701	3120BA632U040HH
A8C4	0180-3486	4	1	CAPACITOR-FXD 6300UF 60 V AL-ELCTLT	19701	3120BC632U060HH
A8C5	0160-3879	7	3	CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X7R103M100V
A8C6	0180-4244	4	2	CAPACITOR-FXD 47UF 40 V AL-ELCTLT	56289	672D476H040CD5C
A8C7	0180-2864	0	2	CAPACITOR-FXD 1000UF 15 V AL-ELCTLT	56289	672D108H015ET5J
A8C8	0180-2864	0		CAPACITOR-FXD 1000UF 15 V AL-ELCTLT	56289	672D108H015ET5J
A8C9	0180-4244	4		CAPACITOR-FXD 47UF 40 V AL-ELCTLT	56289	672D476H040CD5C
A8C10	0180-3771	0	1	CAPACITOR-FXD 1UF 35 V TA	12344	T398A105K035AS
A8C11	0180-3845	9	2	CAPACITOR-FXD 4.7UF 35 V TA	12344	T398E475K035AS
A8C12	0180-3845	9		CAPACITOR-FXD 4.7UF 35 V TA	12344	T398E475K035AS
A8C13	0180-4243	3	1	CAPACITOR-FXD 4.7UF 100 V AL-ELCTLT	10392	CEUSM2A4R7
A8C14	0160-0576	5	1	CAPACITOR-FXD 0.1UF 50 V	09969	RPE121-105X7R104M50V
A8C15	0160-0970	3	1	CAPACITOR-FXD 0.47UF 80 V POLYE-FL	19701	708D1HV474PK800AX
A8C16	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X7R103M100V
A8C17	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X7R103M100V
A8C18	0180-3483	1	2	CAPACITOR-FXD 15 V AL-ELCTLT	56289	36DE623G015BB2P
A8C19	0180-3483	1		CAPACITOR-FXD 15 V AL-ELCTLT	56289	36DE623G015BB2P
A8C20	0180-4242	2	1	CAPACITOR-FXD 100UF 15 V AL-ELCTLT	56289	672D107H015CC3C
A8CR1	1901-1080	1	1	DIODE-SCHOTTKY 20V 1A	04713	1N5817(RELAXED)
A8CR2	1901-0050	3	3	DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A8CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A8CR4	1901-0731	7	3	DIODE-PWR RECT 400V 1A	28480	1901-0731
A8CR5	1902-0939	9	2	VOLTAGE SUPPRESSOR VR=5.0V	11961	1N5908
A8CR6	1902-0939	9		VOLTAGE SUPPRESSOR VR=5.0V	11961	1N5906
A8CR7	0837-0241	6	1	VOLTAGE SUPPRESSOR VR=15V V=24.4V.	24444	SA15A
A8CR8	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A8CR9	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A8CR10	1901-0731	7		DIODE-PWR RECT 400V 1A	28480	1901-0731
A8CR11	1906-0286	7	3	DIODE-CT-S-BARR 35V 20A	04713	MBR2035CT
A8CR12	1906-0286	7		DIODE-CT-S-BARR 35V 20A	04713	MBR2035CT
A8CR13	1906-0096	7	1	DIODE-FW BRDG 200V 2A	28480	1906-0096
A8CR14	1906-0079	6	1	DIODE-FW BRDG 100V 10A	1B546	VJ148X
A8CR15	1906-0286	7		DIODE-CT-S-BARR 35V 20A	04713	MBR2035CT
A8F1	2110-0679	6	1	FUSE-SUBMINIATURE 1A 125V NTD AX	75915	R251001T1
A8F2	2110-0688	7	1	FUSE-SUBMINIATURE 3A 125V NTD AX UL	75915	R251003T1
A8H1	0535-0004	6	4	NUT-HEX DBL-CHAM M3 X 0.5 2.9MM-THK	00000	ORDER BY DESCRIPTION
A8H2	2190-0584	7	4	WASHER-LK HLCL 3.0 MM 3.1-MM-ID	28480	2190-0584
A8J1	1250-1935	4	5	CONNECTOR-RF BNC FEM PC-W-STDFS 50-OHM	24931	28JR356-1
A8J2	1250-1935	4		CONNECTOR-RF BNC FEM PC-W-STDFS 50-OHM	24931	28JR356-1
A8J3	1250-1935	4		CONNECTOR-RF BNC FEM PC-W-STDFS 50-OHM	24931	28JR356-1
A8J4	1250-1935	4		CONNECTOR-RF BNC FEM PC-W-STDFS 50-OHM	24931	28JR356-1
A8J5	1252-0032	4	1	CONN-UTIL P-&-SKT 2-CKT 2-CONT	27264	15-31-1026
A8J6	1251-7684	4	1	CONN-POST TYPE .100-PIN-SPCG 14-CONT	28480	1251-7684
A8J7	1251-8773	4	1	CONN-POST TYPE .100-PIN-SPCG 20-CONT	28480	1251-8773
A8J8	1252-0033	5	1	CONN-UTIL P-&-SKT 4-CKT 4-CONT	27264	15-31-1046
A8J9	1251-8339	8	1	CONN-UTIL P-&-SKT 3-CKT 3-CONT	27264	15-31-1036
A8J10	1252-0034	6	1	CONN-POST TYPE .100-PIN-SPCG 16-CONT	28480	1252-0034
A8J11	1251-8535	6	1	CONN-POST TYPE .100-PIN-SPCG 10-CONT	28480	1251-8535
A8J12	1250-1935	4		CONNECTOR-RF BNC FEM PC-W-STDFS 50-OHM	24931	28JR356-1
A8L1	9100-2616	1	1	TRANSFORMER-PULSE BIFILAR WOUND 18.0 MM	12406	E46
A8L2	9140-0928	8	1	INDUCTOR 100UH ±10% .172D-INX.43LG-IN	91637	IMS-5 100UH ±10%
A8MP3	1205-0496	7	2	HEAT SINK SGL TO-3-CS	13103	6016B-SM4
A8MP4	1205-0462	5	3	HEAT SINK SGL TO-220-CS	13103	6038B-TT
A8Q1	1853-0347	8	1	TRANSISTOR PNP SI DARL PD=40W FT=1MHZ	04713	MJE700
A8Q2	1854-0365	2	1	TRANSISTOR NPN SI PD=310MW FT=60MHZ	04713	2N4410
A8Q3	1854-0215	1	2	TRANSISTOR NPN SI TO-92 PD=350MW	04713	2N3904

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8Q4	1853-0036	2	1	TRANSISTOR PNP SI TO-92 PD=625MW	04713	2N3906(SEL)
A8Q5	1854-0215	1		TRANSISTOR NPN SI TO-92 PD=350MW	04713	2N3904
A8Q6	1853-0478	6	2	TRANSISTOR PNP 2N6490 TO-220AB PD=1.8W	04713	2N6490
A8Q7	1853-0478	6		TRANSISTOR PNP 2N6490 TO-220AB PD=1.8W	04713	2N6490
A8Q8	1854-0884	0	2	TRANSISTOR NPN 2N6488 TO-220AB PD=1.8W	04713	2N6488
A8Q9	1854-0884	0		TRANSISTOR NPN 2N6488 TO-220AB PD=1.8W	04713	2N6488
A8Q10	1854-0697	3	2	TRANSISTOR NPN 2N5886 SI TO-3 PD=200W	04713	2N5886
A8Q11	1854-0697	3		TRANSISTOR NPN 2N5886 SI TO-3 PD=200W	04713	2N5886
A8R1	1810-0429	7	3	NETWORK-RES 10-SIP 22.0K OHM X 5	32997	4310R-102-223
A8R2	1810-0429	7		NETWORK-RES 10-SIP 22.0K OHM X 5	32997	4310R-102-223
A8R3	1810-0398	9	1	NETWORK-RES 10-SIP 22.0K OHM X 9	C1433	750-101
A8R4	0698-0082	7	2	RESISTOR 464 ±1% .125W TF TC=0±100	12498	CT4-1/8-T0-4640-F
A8R5	0698-3155	1	1	RESISTOR 4.64K ±1% .125W TF TC=0±100	12498	CT4-1/8-T0-4641-F
A8R6	0698-3440	7	1	RESISTOR 196 ±1% .125W TF TC=0±100	12498	CT4-1/8-TO-196R-F
A8R7	0698-3158	4	1	RESISTOR 23.7K ±1% .125W TF TC=0±100	12498	CT4-1/8-TO-2372-F
A8R8	0811-1826	1	1	RESISTOR .05 ±5% 3W PWI TC=0±250	91637	CW-2B-39
A8R9	0698-0082	7		RESISTOR 464 ±1% .125W TF TC=0±100	12498	CT4-1/8-T0-4640-F
A8R10	0811-1831	8	1	RESISTOR 2 ±5% 3W PWI TC=0±50	01686	T2B-79
A8R11	0811-3544	4	1	RESISTOR .1 ±5% 3.25W PWI TC=0±90	54294	LA462
A8R12	0698-3153	9	1	RESISTOR 3.83K ±1% .125W TF TC=0±100	12498	CT4-1/8-TO-3161-F
A8R13	0757-0442	9	1	RESISTOR 10K ±1% .125W TF TC=0±100	12498	CT4-1/8-TO-1002-F
A8R14	1810-0347	8	1	NETWORK-RES 8-SIP 2.2K OHM X 4	32997	4308R-102-222
A8R15	0757-0317	7	2	RESISTOR 1.33K ±1% .125W TF TC=0±100	12498	CT4-1/8-TO-1331-F
A8R16	1810-0542	5	1	NETWORK-RES 10-SIP 10.0K OHM X 5	32997	4310R-102-103
A8R17	0698-5880	3	1	RESISTOR 14.7 ±1% .25W TF TC=0±100	K8479	H4
A8R18	0757-0401	0	2	RESISTOR 100 ±1% .125W TF TC=0±100	12498	CT4-1/8-TO-101-F
A8R19	0698-4645	6	1	RESISTOR 4.22K ±1% .25W TF TC=0±100	12498	NA5-1/4-TO-4221-F
A8R20	1810-0429	7		NETWORK-RES 10-SIP 22.0K OHM X 5	32997	4310R-102-223
A8R21	0757-0180	2	2	RESISTOR 31.6 ±1% .125W TF TC=0±100	D8439	MK2
A8R22	0757-0180	2		RESISTOR 31.6 ±1% .125W TF TC=0±100	D8439	MK2
A8R23	0757-0401	0		RESISTOR 100 ±1% .125W TF TC=0±100	12498	CT4-1/8-TO-101-F
A8R24	0757-0317	7		RESISTOR 1.33K ±1% .125W TF TC=0±100	12498	CT4-1/8-T0-1331-F
A8R25	0698-3156	2	1	RESISTOR 14.7K 1% .125W TF TC=0+-100	91637	CMF-55-1
A8S1	3101-2761	3	1	SWITCH-DIP SL 7-1A 0.1A 30VDC	11236	207-7
A8TP1	0360-0124	3	2	CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
A8TP2	0360-0124	3		CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
A8U1	1826-0527	9	1	IC V RGLTR-ADJ-NEG 1.2/37V TO-220 PKG	27014	LM337T
A8XA1A	1251-7300	1	8	CONN-POST TYPE .100-PIN-SPCG 50-CONT	28480	1251-7300
A8XA1B	1251-7300	1		CONN-POST TYPE .100-PIN-SPCG 50-CONT	28480	1251-7300
A8XA2	1251-7300	1		CONN-POST TYPE .100-PIN-SPCG 50-CONT	28480	1251-7300
A8XA3	1251-7300	1		CONN-POST TYPE .100-PIN-SPCG 50-CONT	28480	1251-7300
A8XA4A	1251-7300	1		CONN-POST TYPE .100-PIN-SPCG 50-CONT	28480	1251-7300
A8XA4B	1251-7300	1		CONN-POST TYPE .100-PIN-SPCG 50-CONT	28480	1251-7300
A8XA5	1251-7300	1		CONN-POST TYPE .100-PIN-SPCG 50-CONT	28480	1251-7300
A8XA6	1251-7300	1		CONN-POST TYPE .100-PIN-SPCG 50-CONT	28480	1251-7300
A8XA9	1251-8911	2	1	CONN-POST TYPE .100-PIN-SPCG 60-CONT	28480	1251-8911
A8XA10	1251-1633	1	1	CONNECTOR-PC EDGE 15-CONT/ROW 1-ROW	04072	252-1S-30-310
	1252-1861	9	3	CONNECTOR-SGL CONT SKT .041-IN-BSC-SZ	00779	50865-8

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9	05350-60123	3	1	DISPLAY DRIVER ASSEMBLY	28480	05350-60123

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A12L11	9140-0531	9		INDUCTOR RF-CH-MLD 1UH +-5%	91637	IM-2 1UH 5%
A12L12	9140-0531	9		INDUCTOR RF-CH-MLD 1UH +-5%	91637	IM-2 1UH 5%
A12L13	9140-0531	9		INDUCTOR RF-CH-MLD 1UH +-5%	91637	IM-2 1UH 5%
A12L14	9135-0080	2	1	INDUCTOR 27NH +-5.556% 2.6D-MMX6.6LG-MM	24226	10M271X-1
A12L15	9135-0076	6	1	INDUCTOR RF-CH-MLD 39NH +-6%	06560	010150-054J
A12L16	9140-0518	2	1	INDUCTOR RF-CH-MLD 200NH +-5%	91637	IM-2 .2UH 5%
A12L17	9135-0068	6	1	INDUCTOR RF-CH-MLD 33NH +-6.36%	24226	10M033X-1
A12L18	9140-0520	6	1	INDUCTOR RF-CH-MLD 240NH +-5%	91637	IM-2 .24UH 5%
A12L19	9140-0531	9		INDUCTOR RF-CH-MLD 1UH +-5%	91637	IM-2 1UH 5%
A12MP1	1205-0213	4	1	HEAT SINK SGL TO-5/TO-39-CS	13103	2228B
A12Q1	1854-1003	7	1	TRANSISTOR NPN SI PD=200MW	S0562	2SC2876
A12Q2	1854-0990	9	1	TRANSISTOR NPN SI TO-39 PD=6.75W	04713	MRF630
A12R1	0698-7229	8	1	RESISTOR 511 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-511R-F
A12R2	0757-0280	3	1	RESISTOR 1K +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-1001-F
A12R3	0757-0400	9	2	RESISTOR 90.9 +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-90R9-F
A12R4	0698-7210	7	1	RESISTOR 82.5 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-82R5-F
A12R5	0698-7207	2	1	RESISTOR 61.9 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-61R9-F
A12R6	0698-7212	9	1	RESISTOR 100 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-100R-F
A12R7	0698-7277	6	1	RESISTOR 51.1K +-1% .05W TF TC=0+-100	12498	C3-1/8-T0-5112-F
A12R8	0757-0400	9		RESISTOR 90.9 +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-90R9-F
A12R9	0698-0083	8	1	RESISTOR 1.96K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1961-F
A12R10	0698-7215	2	1	RESISTOR 133 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-133R-F
A12U1				SEE CHASSIS PARTS	28480	5088-7079
A12U2	1813-0213	3	1	IC WIDEBAND AMPL TO-39 PKG	04713	MWA130

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A14	**05361-60009**	7	1	**GATE BOARD ASSEMBLY**	**28480**	**05361-60009**
A14C1	0160-4554	7	40	CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C2	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C3	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C4	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C5	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C6	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C7	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C8	0160-4812	0	1	CAPACITOR-FXD 220PF 100 V	09969	RPA10C0G221J100V
A14C9	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C10	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C11	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C12	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C13	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C14	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C15	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C16	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C17	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C18	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C19	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C20	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C21	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C22	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C23	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C24	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C25	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C26	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C27	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C28	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C29	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C30	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C31	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C32	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C33	0160-4791	4	2	CAPACITOR-FXD 10PF 100 V	09969	RPA10C0G100D100
A14C34	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C35	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C36	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C37	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C38	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C39	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C40	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C41	0160-4791	4		CAPACITOR-FXD 10PF 100 V	09969	RPA10C0G100D100
A14C42	0180-3834	6	4	CAPACITOR-FXD 33UF 10 V TA	12344	T398F336K010AS
A14C43	0180-3834	6		CAPACITOR-FXD 33UF 10 V TA	12344	T398F336K010AS
A14C44	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14C45	0180-3834	6		CAPACITOR-FXD 33UF 10 V TA	12344	T398F336K010AS
A14C46	0180-3834	6		CAPACITOR-FXD 33UF 10 V TA	12344	T398F336K010AS
A14C47	0160-4554	7		CAPACITOR-FXD 0.01UF 50 V	09969	RPA10X7R103M50V
A14CR1	1901-0033	2	2	DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A14CR2	1901-0033	2		DIODE-GEN PRP 180V 200MA DO-35	9N171	1N645
A14J1	1250-1368	7	2	CONNECTOR-RF SMB M PC 50-OHM	98291	51-053-0129
A14J2	1250-1368	7		CONNECTOR-RF SMB M PC 50-OHM	98291	51-053-0129
A14L1	9100-1788	6	2	CORE-FERRITE CHOKE-WIDEBAND-IMP:>680	11214	LB2/2.5ZB
A14L2	9100-1788	6		CORE-FERRITE CHOKE-WIDEBAND-IMP:>680	11214	LB2/2.5ZB
A14P1	1251-8912	3	1	CONN-POST TYPE .100-PIN-SPCG 60-CONT	28480	1251-8912
A14R1	1810-0279	5	2	NETWORK-RES 10-SIP 4.7K OHM X 9	C1433	750-101
A14R2	1810-0488	8	4	NETWORK-RES 8-SIP 4.7K OHM X 4	32997	4308R-1O2-472
A14R3	1810-0488	8		NETWORK-RES 8-SIP 4.7K OHM X 4	32997	4308R-1O2-472
A14R4	1810-0279	5		NETWORK-RES 10-SIP 4.7K OHM X 9	C1433	750-101
A14R5	0698-7252	7	3	RESISTOR 4.64K +-1% .05W TF TC=0+-100	12498	C3-1/8-T0-4641-F

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Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A14R6	0698-7244	7	1	RESISTOR 2.15K +-1% .05W TF TC=0+-100	12498	C3-1/8-T0-2151-F
A14R7	1810-0229	5	4	NETWORK-RES 8-SIP 330.0 OHM X 7	C1433	750-81
A14R8	0698-7210	7	1	RESISTOR 82.5 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-82R5-F
A14R10	0698-7216	3	10	RESISTOR 147 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-147R-F
A14R11						
A14R12	0698-7220	9	15	RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R13	0698-7220	93		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R14	0698-7216	30		RESISTOR 147 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-147R-F
A14R15	0698-7205	09	2	RESISTOR 51.1 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-51R1-F
A14R16	0698-7212	9	4	RESISTOR 100 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-100R-F
A14R17	0698-7220	9		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R18	0698-7216	3		RESISTOR 147 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-147R-F
A14R19	0698-7216	3		RESISTOR 147 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-147R-F
A14R20	0698-7220	9		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R21	0698-7212	9		RESISTOR 100 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-100R-F
A14R22	0698-7212	9		RESISTOR 100 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-100R-F
A14R23	1810-0229	5		NETWORK-RES 8-SIP 330.0 OHM X 7	C1433	750-81
A14R24	0698-7220	9		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R25	0698-7216	3		RESISTOR 147 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-147R-F
A14R26	1810-0277	3	1	NETWORK-RES 10-SIP 2.2K OHM X 9	C1433	750-101
A14R27	0698-7252	7		RESISTOR 4.64K +-1% .05W TF TC=0+-100	12498	C3-1/8-T0-4641-F
A14R28	1810-0769	8	2	NETWORK-RES 10-SIP 150.0 OHM X 9	C1433	750-101
A14R29	1810-0372	9	2	NETWORK-RES 10-SIP 220.0 OHM X 9	C1433	750-101
A14R30	0698-7205	0		RESISTOR 51.1 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-51R1-F
A14R31	1810-0229	5		NETWORK-RES 8-SIP 330.0 OHM X 7	C1433	750-81
A14R32	0698-7220	9		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R33	0698-7216	3		RESISTOR 147 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-147R-F
A14R34	1810-0229	5		NETWORK-RES 8-SIP 330.0 OHM X 7	C1433	750-81
A14R35	0698-7216	3		RESISTOR 147 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-147R-F
A14R36	0698-7240	3	1	RESISTOR 1.47K +-1% .05W TF TC=0+-100	12498	C3-1/8-T0-1471-F
A14R37	0698-7220	9		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R38	1810-0231	9	1	NETWORK-RES 8-SIP 2.2K OHM X 7	C1433	750-81
A14R39	1810-0488	8		NETWORK-RES 8-SIP 4.7K OHM X 4	32997	4308R-1O2-472
A14R40	1810-0488	8		NETWORK-RES 8-SIP 4.7K OHM X 4	32997	4308R-1O2-472
A14R41	0698-7220	9		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R42	0698-7252	7		RESISTOR 4.64K +-1% .05W TF TC=0+-100	12498	C3-1/8-T0-4641-F
A14R43						
A14R44	0698-7212	9		RESISTOR 100 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-100R-F
A14R45	0698-7220	9		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R46	0698-7222	1	2	RESISTOR 261 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-261R-F
A14R47	0698-7220	9		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R48	0698-7220	9		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R49	0698-7220	9		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R50	0698-7222	1		RESISTOR 261 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-261R-F
A14R51	0698-7216	3		RESISTOR 147 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-147R-F
A14R52	0698-7220	9		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R53	0698-7216	3		RESISTOR 147 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-147R-F
A14R54	0698-7216	3		RESISTOR 147 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-147R-F
A14R55	0698-7220	9		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R56	1810-0769	8		NETWORK-RES 10-SIP 150.0 OHM X 9	C1433	750-101
A14R57	1810-0372	9		NETWORK-RES 10-SIP 220.0 OHM X 9	C1433	750-101
A14R58	0698-7220	9		RESISTOR 215 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-215R-F
A14R59	0698-7236	7	1	RESISTOR 1K +-1% .05W TF TC=0+-100	12498	C3-1/8-T0-1001-F
A14U1	1820-2998	0	1	IC LCH CMOS/74HC TRANSPARENT OCTL	04713	MC74HC373N
A14U2	1820-3082	5	2	IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC374N
A14U3	1820-3347	5	1	IC-10 MHZ PROGRAMMABLE INTERVAL TIMER	34649	P8254-2
A14U4	1820-2656	7	1	IC GATE TTL ALS NAND QUAD 2-INP	01295	SN74ALS00AN
A14U5	1820-4081	6	2	IC XLTR ECL/10KH TTL-TO-ECL QUAD	04713	MC10H124P
A14U6	1820-2823	0	3	IC GATE ECL/10KH NOR QUAD 2-INP	04713	MC10H102P
A14U7	1820-4159	9	2	IC CNTR ECL/10KH BIN SYNCHRO 4-BIT	04713	MC10H016P
A14U8	1820-3831	2	1	IC MUXR/DATA-SEL ECL/10KH 4-TO-1-LINE	04713	MC10H174P
A14U9	1820-3337	3	1	IC GATE ECL/10KH AND QUAD 2-INP	04713	MC10H104P
A14U10	1820-2849	0	5	IC FF ECL/10KH D-M/S DUAL	04713	MC10H131P

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A14U11	1820-2488	3	2	IC FF TTL ALS D-TYPE POS-EDGE-TRIG	01295	SN74ALS74AN
A14U12	1820-3082	5		IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC374N
A14U13	1820-3121	3	1	IC TRANSCEIVER TTL ALS BUS OCTL	01295	SN74ALS245AN
A14U14	1820-2691	0	2	IC FF TTL F D-TYPE POS-EDGE-TRIG	18324	74F74N
A14U15	1820-4079	2	2	IC XLTR ECL/10KH ECL-TO-TTL QUAD	04713	MC10H125P
A14U16	1820-1074	1	1	IC DRVR TTL NOR QUAD 2-INP	01295	SN74128N
A14U17	1820-4079	2		IC XLTR ECL/10KH ECL-TO-TTL QUAD	04713	MC10H125P
A14U18	1820-2822	9	2	IC GATE ECL/10KH OR-NOR TPL	04713	MC10H105P
A14U19	1820-4159	9		IC CNTR ECL/10KH BIN SYNCHRO 4-BIT	04713	MC10H016P
A14U20	1820-2849	0		IC FF ECL/10KH D-M/S DUAL	04713	MC10H131P
A14U21	1820-2822	9		IC GATE ECL/10KH OR-NOR TPL	04713	MC10H105P
A14U22	1820-2956	0	1	IC GATE ECL/10KH EXCL-OR/NOR TPL 2-INP	04713	MC10H107P
A14U23	1820-2849	0		IC FF ECL/10KH D-M/S DUAL	04713	MC10H131P
A14U24	1820-2488	3		IC FF TTL ALS D-TYPE POS-EDGE-TRIG	01295	SN74ALS74AN
A14U25	1820-2694	3	1	IC FF TTL F J-K NEG-EDGE-TRIG	18324	74F112N
A14U26	1820-2691			IC FF TTL F D-TYPE POS-EDGE-TRIG	18324	74F74N
A14U27	1820-3079	0	1	IC DCDR CMOS/74HC 3-TO-8-LINE	04713	MC74HC138N
A14U28	1820-2889	8	1	IC GATE TTL ALS AND TPL 3-INP	01295	SN74ALS11AN
A14U29	1820-1425	6	1	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
A14U30	1820-4081	6		IC XLTR ECL/10KH TTL-TO-ECL QUAD	04713	MC10H124P
A14U31	1820-2823	0		IC GATE ECL/10KH NOR QUAD 2-INP	04713	MC10H102P
A14U32	1820-3461	4	1	IC RCVR ECL/10KH LINE RCVR QUAD	04713	MC10H115P
A14U33	1820-2823	0		IC GATE ECL/10KH NOR QUAD 2-INP	04713	MC10H102P
A14U34	1820-2849	0		IC FF ECL/10KH D-M/S DUAL	04713	MC10H131P
A14U35	1820-2849	0		IC FF ECL/10KH D-M/S DUAL	04713	MC10H131P
A14U36	1820-2686	3		IC GATE TTL		
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	73957	GP24-063 X 250-17
	4040-0748	3	2	EXTR-PC BD BLK POLYC .062-IN-BD-THKNS	28480	4040-0748

See introduction to this section for ordering information

Table 6-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7W1	05350-60105	1	1	CABLE ASSEMBLY, KEYBOARD	28480	05350-60105
A4U8	05361-80010	2	1	EPROM (For Std 5361B, 5361B/Opt 026)	28480	05361-80010
A4U8	05361-80011	3	1	EPROM (For 5361BB/Opt 040)	28480	05361-80011
A4U8	05361-80012	4	1	EPROM (For Std 5361B, 5361B/Opt 026 with Opt 700 Mate)	28480	05361-80012
A8Y1	0960-0612	6	1	CRYSTAL-OSCILLATOR 10.0 MHZ; 0-55 DEG C	82567	03-02236-001
A12R7	0699-1748		1	RESISTOR 287K 1% .05WF (5361B OPT 026 AND 040)		
A12U1	05361-80016		1	EPROM (FOR STD 5361B AND OPT 040)	28480	05361-80016
A13	0960-0443	1	1	LINE MODULE-FILTERED	05245	F2058D
B1	0160-0464	0	1	CAP-FXD 470PF 500 V MICA	28480	0160-0464
C1	0160-3036	8	4	CAP-FXD 5000PF 0 V	09535	2425-011 X5V 502Z
C2	0160-3036	8		CAP-FXD 5000PF 0 V	09535	2425-011 X5V 502Z
C3	0160-3036	8		CAP-FXD 5000PF 0 V	09535	2425-011 X5V 502Z
C4	0160-3036	8		CAP-FXD 5000PF 0 V	09535	2425-011 X5V 502Z
DS1	05350-80001	8	1	LCD-14SEG 24CRTR	28480	05350-80001
F1	2110-0007	4	1	FUSE (INCH) 1A 250V TD FE UL	75915	313 001
	2110-0202	1	1	FUSE (INCH) .5A 250V TD FE UL	75915	313.500
H1	0380-1332	9	2	STANDOFF-HEX .18-IN-LG 6-32-THD	28480	0380-1332
H1U1	0624-0097	9	2	SCREW-TPG 4-40 .188-IN-LG PAN-HD-POZI	28480	0624-0097
H2	0380-1582	1	1	SPACER-SNAP-IN 1.25 IN LG; .28 IN DIA	28480	0380-1582
H3	0510-1148	2	4	RETAINER-PUSH-ON KB-TO-SHFT EXT	78553	C4154-017-27
H4	0515-1163		2	SCREW-MACH M5 X 0.8 45MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
H5	0515-0885	2	7	SCREW-MACH M4 X 0.7 8MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
H6	0515-0886	3	29	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
H7	0515-0890	9	5	SCREW-MACH M3 X 0.5 6MM-LG 90-DEG-FLH-HD	00000	ORDER BY DESCRIPTION
H8	0515-0897	6	10	SCREW-MACH 4-24 .375-IN-LG PAN-HD POZI	00000	ORDER BY DESCRIPTION
H9	0515-1060	7	4	SCREW-MACH M3 X 0.5 25MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
H10	0515-1232	5	8	SCREW-MACH M3.5 X 0.6 8MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
H11	0535-0004	9	4	NUT-HEX DBL-CHAM M3 X 0.5 2.9MM-THK	00000	ORDER BY DESCRIPTION
H12	0590-0505	1	1	NUT-KNRLD-R 5/8-24-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
H14	0515-0887	4	1	SCREW-MACH M3.5 X 0.6 6MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
H15	0624-0324	5	1	SCREW-TPG 4-20 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H16	2190-0068	5	6	WASHER-LK INTL T 1/2 IN .505-IN-ID	78189	1924-02
H17	2190-0084	5	2	WASHER-LK INTL T 1/4 IN .256-IN-ID	78189	1214-05
H18	2190-0124	4	2	WASHER-LK INTL T NO. 10 .195-IN-ID	16179	500222
H19	2190-0577	1	2	WASHER-LK HLCL NO. 10 .194-IN-ID	28480	2190-0577
H20	2190-0587	3	2	WASHER-LK HLCL 5.0 MM 5.1-MM-ID	28480	2190-0587
H21	2190-0644	3	4	WASHER-LK EXT T-B 3.0 MM 3.15-MM-ID	28480	2190-0644
H22	2190-0650	1	2	WASHER-LK 90 CTSK EXT T-B 3.0 MM	28480	2190-0650
H23	2360-0115	4	2	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H24	0515-1331	5	8	SCREW-METRIC SPECIALTY M4 X 0.7 THD; 7MM	00000	ORDER BY DESCRIPTION
H25	0515-0896	5	6	SCREW-MACH M4 X 0.7 10MM-LG	00000	ORDER BY DESCRIPTION
H26	0515-1132	4	2	SCREW-MACH M5 X 0.8 10MM-LG	00000	ORDER BY DESCRIPTION
H27				NOT ASSIGNED		
H28	2950-0078	9	3	NUT-HEX-DBL-CHAM 10-32-THD .067-IN-THK	28480	2950-0078
H29	2950-0196	2	1	NUT-HEX-DBL-CHAM 1/4-36-THD .06-IN-THK	00000	ORDER BY DESCRIPTION
H30	3050-0016	8	1	WASHER-FL NO. 6 .147-IN-ID BRASS	00000	ORDER BY DESCRIPTION
H32	0360-1610	4	1	TERMINAL-SLDR LUG PL-MTG FOR-#6-SCR	79963	608.136H
H33	0515-1124	4	6	SCREW-MACH M3 X 0.5 4MM-LG 90-DEG-FLH-HD	00000	ORDER BY DESCRIPTION
J2	1250-1899	9	1	ADAPTER-COAX STR F-BNC M-SMC	24931	29JJ166-1
J2F1	2110-0301	1	1	FUSE (INCH) .125A 125V AX	D3841	19275.125
MP1	0340-1101	6	1	INSULATOR THRM-CNDCT	55285	7403-09FR-AC
MP2	1460-1345	5	2	TILT STAND ST STEEL	28480	1460-1345
MP3	6960-0002	4	1	PLUG-HOLE TR-HD FOR .5-D-HOLE STEEL	71785	SS-48152-K1110
MP4	6960-0010	4	1	PLUG-HOLE TR-HD FOR .625-D-HOLE STEEL	71785	SS-48172-K1110
MP5	5021-8403	4	1	FRAME-FRONT	28480	5021-8403
MP6	5021-5804	3	1	FRAME-REAR	28480	5021-5804
MP7	5021-5835	0	4	STRUT-CORNER	28480	5021-5835
MP8	5021-8496	5	2	TRIM-FRONT HANDLE	28480	5021-8496
MP9	5041-8801	8	2	FOOT	28480	5041-8801
MP10	5041-8802	9	1	TOP-TRIM	28480	5041-8802

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP11	5041-8819	8	1	STRAP-HANDLE CAP FRONT	28480	5041-8819
MP12	5041-8820	1	1	STRAP-HANDLE CAP REAR	28480	5041-8820
MP13	5041-8822	3	2	FOOT-NON SKID	28480	5041-8822
MP14	5062-3702	2	1	STRAP HANDLE ASSY	28480	5062-3702
MP15	5062-3733	9	1	COVER-TOP	28480	5062-3733
MP16	5062-3745	3	1	COVER-BOTTOM	28480	5062-3745
MP17	5062-3778	2	1	COVER-SIDE	28480	5062-3778
MP18	5062-3799	7	2	SYS II HANDLES	28480	5062-3799
MP19	05334-40003	6	2	CROSS MEMBER	28480	05334-40003
MP21	05361-00002	4	1	PANEL-SUB	28480	05361-00002
MP22	05361-00003	5	1	PANEL-REAR	28480	05361-00003
MP23	05361-00006	8	1	COVER-RF CAVITY	28480	05361-00006
MP24	05350-00006	5	1	BRACKET-RF CAV	28480	05350-00006
MP26	05361-00009	1	1	BRACKET-MICROWAVE MODULE	28480	05361-00009
MP27				NOT ASSIGNED		
MP28				NOT ASSIGNED		
MP29	05350-00012	3	1	CLAMP-TO-220	28480	05350-00012
MP30	05361-00004	6	1	CARD CAGE	28480	05361-00004
MP31	05350-00026	9	1	COVER-SIDE, PERFORATED	28480	05350-00026
MP32	05361-00007	9	1	PLATE-TRANS	28480	05361-00007
MP33	05361-00008	0	1	BRACKET-TRANS	28480	05361-00008
MP35	05350-20203	6	1	WINDOW	28480	05350-20203
MP36	05350-20204	7	1	SPACER	28480	05350-20204
MP37	05343-20204		1	COLLAR-CONNECTOR (Opt 026 and 040)		
MP39	05361-00011	3	1	PANEL-FRONT	28480	05361-00001
T1	9100-4722	4	1	XFMR-PWR 100/120/220/240V MEET IEC348	05216	PX4842
W1	05350-60109	5	1	CABLE ASSY-INPUT **NOTE:** THE INPUT CONNECTOR FOR THE 5361A INPUT 1 IS PART OF THE W1 CABLE ASSEMBLY	28480	05350-60109
W2	8120-5254	0	1	CABLE-ASSY-COAX	28480	8120-5254
W3	05350-60102	8	1	CABLE ASSY-SYNTHESIZER	28480	05350-60102
W4	8120-5253	9	1	CABLE-ASSY-COAX	28480	8120-5253
W5	05372-60221	8	1	CABLE ASSY-SAMPLER POWER	28480	05372-60221
W6	8120-5252	8	2	CABLE ASSEMBLY .380MM LONG; GATE IN/OUT	28480	8120-5252
W7	8120-5252	8		CABLE ASSEMBLY .380MM LONG; GATE IN/OUT	28480	8120-5252
W8	05350-60105	1	1	CABLE ASSY-KEYBOARD	28480	05350-60105
W9	05350-60122	2	1	CABLE ASSY-DISPLAY	28480	05350-60122
W10	8120-1378	1	1	POWER CORD SET 18-AWG 3-COND 90-IN-LG	11383	PS-204-625
W10	05350-60111		1	CABLE ASSY, SYNTHESIZER (OPT 006)		
	0361-1196	3	2	RIVET-PLASTIC PUSH-ON .	02201	SR-4070W
	0400-0010	2	1	GROMMET-RND .25-IN-ID .375-IN-GRV-OD	18310	760-3103
	0590-1251	6	2	NUT-SPCLY 15/32-32-THD .1-IN-THK .562-WD	00000	ORDER BY DESCRIPTION
	0624-0562	3	2	SCREW-TPG 10-32 .375-LG PAN-HD POZI	00000	ORDER BY DESCRIPTION
	0624-0767		28	SCREW-TPG 6-32 .437-IN-LG PAN-HD W/LKWR	00000	ORDER BY DESCRIPTION
	1252-2256	6	2	CONNECTOR-ELASTOMERIC SPONGE RUBBER	28480	1252-2256
	2190-0646	5	1	WASHER-LK EXT T-B 4.0 MM 4.15-MM-ID	28480	2190-0646
	2360-0115	4	4	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2510-0192	6	8	SCREW-MACH 8-32 .25-IN-LG 100 DEG	28480	2510-0192
	7121-4555	3	1	LABEL-MES.003/80	28480	7121-4555
	8159-0005	0	1	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	11502	YZO 1/4
	8160-0097	3	1	RFI ROUND STRIP CNDCT-ELSTMR .07-IN-OD	18565	10-04-1687-1215
	05348-00011		1	PAD, FOAM		
	05350-00021	4	1	SHIELD-ESD	28480	05350-00021
	05361-20202	8	2	RF CAVITY	28480	05361-20202
	05350-40001	4	1	MOUNT-LCD DS1	28480	05350-40001
	05350-40003	6	1	REFLECTOR	28480	05350-40003
	05361-00005	7	1	RETAINER-PC BD	28480	05361-00005
	05361-00010	4	1	MODULE-MICROWAVE	28480	05361-00010
	05361-00015	9	1	BRACKET- POWER MODULE	28480	05361-00015
	05361-00016		3	RF BARRIER	28480	05361-00016
	05361-80007	7	1	LABLE VDE	28480	05361-80007
	05061-90027		1	5361A/B OPERATING & PROGRAMMING MANUAL	28480	05361-90027
	5062-3977		1	**OPTION 908**, RACK MOUNT KIT (WITHOUT HANDLES)	28480	5062-3977
	5062-4071		1	**OPTION 913**, RACK MOUNT KIT (WITH HANDLES)	28480	5062-4071

See introduction to this section for ordering information

Table 3-4. Replaceable Parts for Options

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				OPTION 001 - OVEN TIMEBASE		
H23	2360-0115	4	4	SCREW-MACH 6-32 .312-IN-LG PAN-HD POZI	00000	ORDER BY DESCRIPTION
A10Y1	10811-60111	8	1	QUARTZ CRYSTAL OSCILLATOR 10 MHZ	28480	10811-60111
				OPTION 006 – LIMITER		
AT1	5088-7049	2	1	LIMITER, 26.5 GHZ	28480	5088-7049
	05350-60111	9	1	CABLE ASSY, LIMITER	28480	05350-60111
				OPTION 010 – HIGH STABILITY OVEN TIMEBASE		
H23	2360-0115	4	4	SCREW-MACH 6-32 .312-IN-LG PAN-HD POZI	00000	ORDER BY DESCRIPTION
A10Y1	10811-60211	9	1	QUARTZ CRYSTAL OSCILLATOR - 10 MHZ	28480	10811-60211

See introduction to this section for ordering information

Table 3-4. Replaceable Parts for Options (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				5361B OPTIONS 026/040 – 26.5 AND 40 GHZ FREQUENCY EXTENSION		
A12	**05361-60013**	**3**	**1**	**MW MODULE ASSY (FOR 26.5/40 GHZ CNTRS ONLY)**	**28480**	**05361-60012**
				NOTE THE FOLLOWING A12 PARTS LIST APPLIES ONLY TO THE 5361-60003 ASSEMBLY INSTALLED IN THE 5361B OPTIONS 026/040. REFER TO THE A12 PARTS LIST IN TABLE 3-3 (STANDARD INSTRUMENT LIST) FOR THE 5361A AND 5361B STANDARD COUNTER A12 PARTS.		
				NOTE THE A12 MICROWAVE ASSEMBLY DOES NOT INCLUDE THE U1 SAMPLER. REFER TO CHASSIS PARTS.		
A12C1	0160-0576	5	12	CAPACITOR-FXD 0.1UF 50 V	09969	RPE121-105X7R104M50V
A12C2	0160-0576	5		CAPACITOR-FXD 0.1UF 50 V	09969	RPE121-105X7R104M50V
A12C3	0160-0576	5		CAPACITOR-FXD 0.1UF 50 V	09969	RPE121-105X7R104M50V
A12C4	0160-3875	3	2	CAPACITOR-FXD 22PF 200 V	09969	RPE121-105C0G220J200V
A12C5	0160-4385	2	1	CAPACITOR-FXD 15PF 200 V	04222	SR202A150JAA
A12C6	0180-3771	0	2	CAPACITOR-FXD 1UF 35 V TA	12344	T398A105K035AS
A12C7	0180-3771	0		CAPACITOR-FXD 1UF 35 V TA	12344	T398A105K035AS
A12C8	0160-4804	0	1	CAPACITOR-FXD 56PF 100 V	09969	RPA10C0G560J100
A12C9	0160-3879	7	2	CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X7R103M100V
A12C10	0160-0576	5		CAPACITOR-FXD 0.1UF 50 V	09969	RPE121-105X7R104M50V
A12C11	0160-0576	5		CAPACITOR-FXD 0.1UF 50 V	09969	RPE121-105X7R104M50V
A12C12	0160-3879	7		CAPACITOR-FXD 0.01UF 100 V	09969	RPE121-105X7R103M100V
A12C13	0160-4040	6	4	CAPACITOR-FXD 1000PF 100 V	09969	RPE121-105C0G102J100V
A12C14	0160-0576	5		CAPACITOR-FXD 0.1UF 50 V	09969	RPE121-105X7R104M50V
A12C15	0160-4040	6		CAPACITOR-FXD 1000PF 100 V	09969	RPE121-105C0G102J100V
A12C16	0160-3875	3		CAPACITOR-FXD 22PF 200 V	09969	RPE121-105C0G220J200V
A12C17	0160-4040	6		CAPACITOR-FXD 1000PF 100 V	09969	RPE121-105C0G102J100V
A12C18	0160-0576	5		CAPACITOR-FXD 0.1UF 50 V	09969	RPE121-105X7R104M50V
A12C19	0160-4491	1	2	CAPACITOR-FXD 0F 200 V	09969	RPE121-105C0G8R2D200V
A12C20	0160-0576	5		CAPACITOR-FXD 0.1UF 50 V	09969	RPE121-105X7R104M50V
A12C21	0160-4491	1		CAPACITOR-FXD 0F 200 V	09969	RPE121-105C0G8R2D200V
A12C22	0160-6428	8	1	CAPACITOR-FXD 39PF 200 V	56289	1C10C0G390J200B(C15)
A12C23	0160-0576	5		CAPACITOR-FXD 0.1UF 50 V	09969	RPE121-105X7R104M50V
A12C24	0160-3874	2	2	CAPACITOR-FXD 0F 200 V	09969	RPE121-105C0G100D200V
A12C25	0160-0576	5		CAPACITOR-FXD 0.1UF 50 V	09969	RPE121-105X7R104M50V
A12C26	0160-0576	5		CAPACITOR-FXD 0.1UF 50 V	09969	RPE121-105X7R104M50V
A12C27	0160-4040	6		CAPACITOR-FXD 1000PF 100 V	09969	RPE121-105C0G102J100V
A12C28	0160-4383	0	1	CAPACITOR-FXD 0F 200 V	09969	RPE121-105C0G6R8D200V
A12C29	0160-3874	2		CAPACITOR-FXD 0F 200 V	09969	RPE121-105C0G100D200V
A12C30	0160-0576	5		CAPACITOR-FXD 0.1UF 50 V	09969	RPE121-105X7R104M50V
A12J1	1250-1611	3	2	CONNECTOR-RF SMB M PC 50-OHM	98291	51-051-0289
A12J2	1250-1611	3		CONNECTOR-RF SMB M PC 50-OHM	98291	51-051-0289
A12J3	1251-6939	0	3	CONNECTOR-SGL CONT SKT .032-IN-BSC-SZ	98291	006-4801
A12J4	1251-6939	0		CONNECTOR-SGL CONT SKT .032-IN-BSC-SZ	98291	006-4801
A12J5	1251-6939	0		CONNECTOR-SGL CONT SKT .032-IN-BSC-SZ	98291	006-4801
A12J6	1252-0233	7	4	CONNECTOR-SGL CONT SKT .039-IN-BSC-SZ	00779	50865-3
A12J7	1252-0233	7		CONNECTOR-SGL CONT SKT .039-IN-BSC-SZ	00779	50865-3
A12J8	1252-0233	7		CONNECTOR-SGL CONT SKT .039-IN-BSC-SZ	00779	50865-3
A12J9	1252-0233	7		CONNECTOR-SGL CONT SKT .039-IN-BSC-SZ	00779	50865-3
A12L1	9140-0522	8	1	INDUCTOR RF-CH-MLD 360NH +-5%	91637	IM-2 .36UH 5%
A12L2	9135-0072	2	2	INDUCTOR 56NH +-5.893% 2.6D-MMX6.6LG-MM	24226	10M056X-1
A12L3	9135-0078	8	1	INDUCTOR RF-CH-MLD 82NH +-5.61%	24226	10M082X-1
A12L4	9135-0072	2		INDUCTOR 56NH +-5.893% 2.6D-MMX6.6LG-MM	24226	10M056X-1
A12L5	9135-0074	4	1	INDUCTOR RF-CH-MLD 47NH +-6.17%	24226	10M047X-1
A12L6	9135-0081	3	1	INDUCTOR RF-CH-MLD 68NH +-5%	06560	010150-056J
A12L7	9100-3922	4	1	INDUCTOR-FIXED 120-1300 HZ	28480	9100-3922
A12L8	9140-0531	9	6	INDUCTOR RF-CH-MLD 1UH +-5%	91637	IM-2 1UH 5%
A12L9	9140-0531	9		INDUCTOR RF-CH-MLD 1UH +-5%	91637	IM-2 1UH 5%
A12L10				NOT ASSIGNED		

See introduction to this section for ordering information

Table 3-4. Replaceable Parts for Options (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A12L11	9140-0531	9		INDUCTOR RF-CH-MLD 1UH +-5%	91637	IM-2 1UH 5%
A12L12	9140-0531	9		INDUCTOR RF-CH-MLD 1UH +-5%	91637	IM-2 1UH 5%
A12L13	9140-0531	9		INDUCTOR RF-CH-MLD 1UH +-5%	91637	IM-2 1UH 5%
A12L14	9135-0080	2	1	INDUCTOR 27NH +-5.556% 2.6D-MMX6.6LG-MM	24226	10M271X-1
A12L15	9135-0076	6	1	INDUCTOR RF-CH-MLD 39NH +-6%	06560	010150-054J
A12L16	9140-0518	2	1	INDUCTOR RF-CH-MLD 200NH +-5%	91637	IM-2 .2UH 5%
A12L17	9135-0068	6	1	INDUCTOR RF-CH-MLD 33NH +-6.36%	24226	10M033X-1
A12L18	9140-0520	6	1	INDUCTOR RF-CH-MLD 240NH +-5%	91637	IM-2 .24UH 5%
A12L19	9140-0531	9		INDUCTOR RF-CH-MLD 1UH +-5%	91637	IM-2 1UH 5%
A12MP1	1205-0213	4	1	HEAT SINK SGL TO-5/TO-39-CS	13103	2228B
A12Q1	1854-1003	7	1	TRANSISTOR NPN SI PD=200MW	S0562	2SC2876
A12Q2	1854-0990	9	1	TRANSISTOR NPN SI TO-39 PD=8.75W	04713	MRF630
A12R1	0698-7229	8	1	RESISTOR 511 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-511R-F
A12R2	0757-0280	3	1	RESISTOR 1K +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-1001-F
A12R3	0757-0400	9	2	RESISTOR 90.9 +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-90R9-F
A12R4	0698-7210	7	1	RESISTOR 82.5 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-82R5-F
A12R5	0698-7207	2	1	RESISTOR 61.9 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-61R9-F
A12R6	0698-7212	9	1	RESISTOR 100 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-100R-F
A12R7	0699-1748	6	1	RESISTOR 287K ±1% .05W TF TC=0+-100	28480	0699-1748
A12R8	0757-0400	9		RESISTOR 90.9 +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-90R9-F
A12R9	0698-0083	8	1	RESISTOR 1.96K +-1% .125W TF TC=0+-100	12498	CT4-1/8-TO-1961-F
A12R10	0698-7215	2	1	RESISTOR 133 +-1% .05W TF TC=0+-100	12498	C3-1/8-TO-133R-F
A12U1				SEE CHASSIS PARTS	28480	5088-7079
A12U2	1813-0213	3	1	IC WIDEBAND AMPL TO-39 PKG	04713	MWA130

See introduction to this section for ordering information

Table 3-4. Replaceable Parts for Options (Continued)

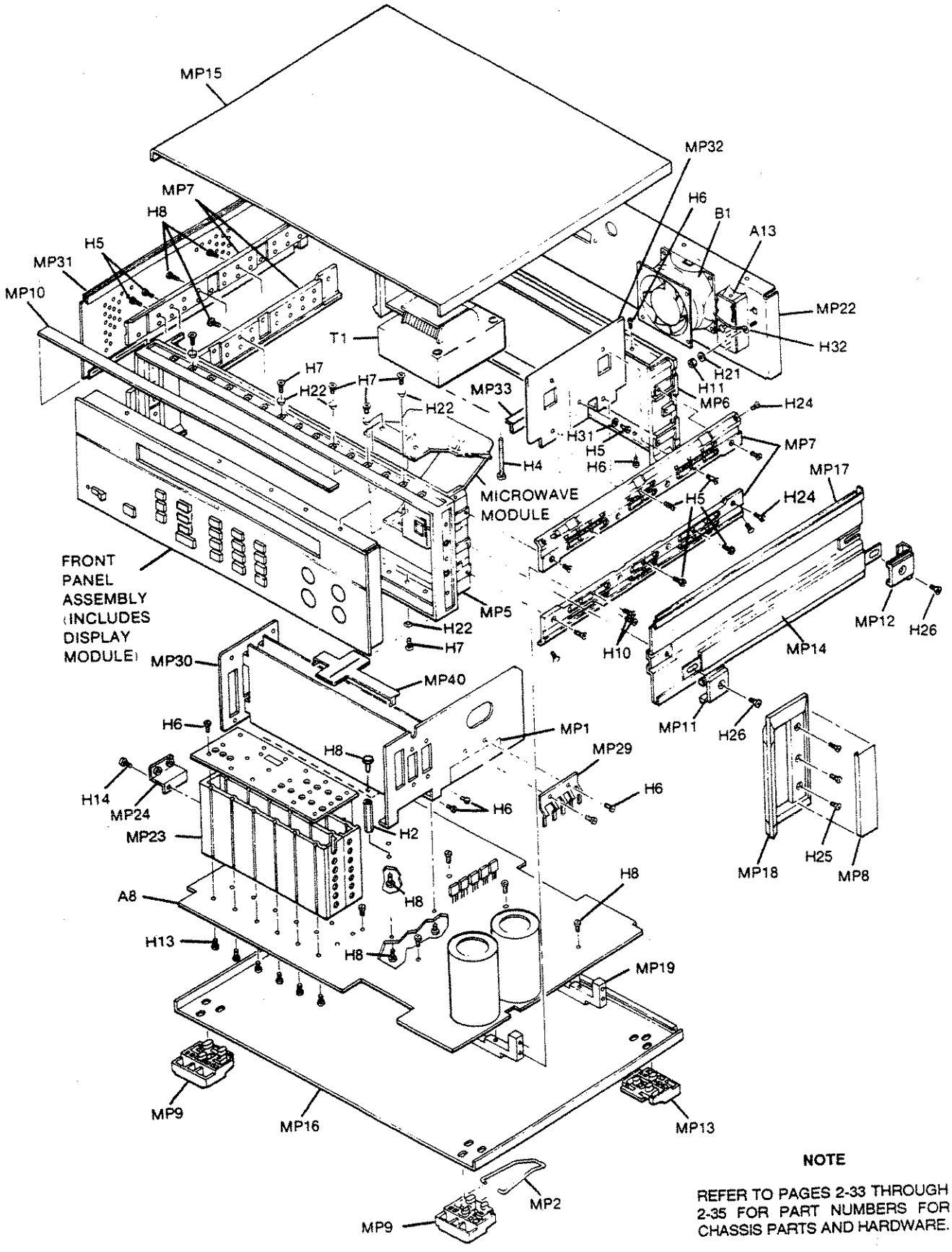
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				5361B OPTION 700 MATE		
A4	**05350-60024**	**3**	**1**	**MICROPROCESSOR BOARD (OPTION 700) SERIES 3049**	**28480**	**05350-60024**
				NOTE EPROM U8 IS NOT SUPPLIED AS PART OF THIS BOARD. REFER TO CHASSIS PARTS NEAR THE END OF THE PARTS LISTS FOR THE PART NUMBER TO ORDER. HOWEVER, IF YOU ALREADY HAVE A 05350-60024 ASSEMBLY (A4) AND ITS EPROM NEEDS REPLACE-ENT, YOU SHOULD REORDER THE SAME EPROM BY USING THE PART NUMBER ON THE OLD EPROM.		
C1	0160-4787	8	2	CAPACITOR-FXD 22PF +-5% 100WVDC CER	04222	SA102A220JAAH
C2	0160-4787	8		CAPACITOR-FXD 22PF +-5% 100WVDC CER	04222	SA102A220JAAH
C3	0160-4557	0	20	CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C4	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C5	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C6	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C7	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C8	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C9	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C10	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C11	0180-3770	9	1	CAPACITOR-FXD 2.2UF +-10% 35V TA	56289	299D225X9035BB1
C12	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C13	0160-4808	4	1	CAPACITOR-FXD 470PF +-5% 100VDC CER	04222	SA101A471JAAH
C14	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C15	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C16	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C17	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C18	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C19	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C20	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C21	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C22	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C23	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C24	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50WVDC CER	04222	SA305C104MAAH
C25	0180-3775	4	2	CAPACITOR-FXD 68UF +-10% 10V TA	56289	299D686X9010DB1
C26	0180-3775	4		CAPACITOR-FXD 68UF +-10% 10V TA	56289	299D686X9010DB1
CR1	1901-0050	3	3	DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
J1	1251-4775	8	1	CONNECTOR POST-TYPE .150-PIN SPCG 10-CONT	00779	87221-9
L1	9100-0541	7	1	INDUCTOR RF-CH-MLD 250UH +-10%	04213	1670-1
L2	9140-0990		1	INDUCTOR 1UH +-10% .172D-INX .43LG-IN	99800	1641-102
MP1	1480-0116	8	2	PIN-GROOVE .062-IN-DIA .25-IN-LG STL	73957	GP24-063 X 250-17
MP2	4040-0748	3	2	EXTRACTOR- PC BOARD BLACK	28480	4040-0748
P1A	1251-7986	9	2	CONNECTOR-POST-TYPE .100-PIN SPCG 50-CONT	00779	534204-1
P1B	1251-7986	9		CONNECTOR-POST-TYPE .100-PIN SPCG 50-CONT	00779	534204-1
R1	0698-3157	3	3	RESISTOR 19.6K +-1% .125W TF TC=0+-100	19701	SF425H
R2	8159-0005	0	3	RESISTOR- ZERO-OHM 22AWG	28480	8159-0005
R3	8159-0005	0		RESISTOR- ZERO-OHM 22AWG	28480	8159-0005
R4	0757-0442	9	6	RESISTOR 10K +-1% .125W TF TC=0+-100	19701	SF425H
R5	8159-0005	0		RESISTOR- ZERO-OHM 22AWG	28480	8159-0005
R6	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	19701	SF425H
R7	1810-0398	9	1	RESISTOR 10-SIP 22K-OHM	11236	750-101
R8	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	19701	SF425H
R9	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	19701	SF425H
R10	0698-3157	3		RESISTOR 19.6K +-1% .125W TF TC=0+-100	19701	SF425H
R11	0698-3157	3		RESISTOR 19.6K +-1% .125W TF TC=0+-100	19701	SF425H
R12	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	19701	SF425H
R13	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	19701	SF425H

See introduction to this section for ordering information

Table 3-4. Replaceable Parts for Options (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U1	1820-3159	7	1	IC MPU W/2 MHZ CLOCK 8-BITS 64K ADDRESS	04713	MC68B03L
U2	1810-0758	5	1	DELAY LINE 14-DIP	28480	1810-0758
U3	1820-2684	1	1	IC GATE TTL/F NAND QUAD 2-INP	18324	74F00N
U4	05361-80009	9	1	ADDRESS DECODER	28480	05361-80009
U5	1820-2488	3	1	IC-FF TTL/ALS D-TYPE POS-EDGE TRIG	01295	SN74ALS74AN
U6	1820-3121	3	1	IC TRANSCEIVER TTL/ALS BUS OCTL	01295	SN74ALS245AN
U7	1820-2724	0	6	IC LCH TTL/ALS TRANSPARENT OCTL	01295	SN74ALS573CN
U8				SEE CHASSIS PARTS		
U9	1820-3415		1	IC-TIMER MODULE (OPT 700 ONLY)	28480	1820-3415
U10	1818-3185	4	1	IC-CMOS 65536 (64K) STAT RAM 120-NS 3-S	S4013	HM6264ALP-12L
U11	1820-2724	0		IC LCH TTL/ALS TRANSPARENT OCTL	01295	SN74ALS573CN
U12	1820-3100	8	1	IC DECODER TTL/ALS BIN 3-TO-8-LINE 3-INP	01295	SN74ALS138N
U13	1820-2757	9	4	IC FF TTL/ALS D-TYPE POS-EDGE-TRIG COM	01295	SN74AALS574BN
U14	1820-2757	9		IC FF TTL/ALS D-TYPE POS-EDGE-TRIG COM	01295	SN74AALS574BN
U15	1820-2757	9		IC FF TTL/ALS D-TYPE POS-EDGE-TRIG COM	01295	SN74AALS574BN
U16	1820-2757	9		IC FF TTL/ALS D-TYPE POS-EDGE-TRIG COM	01295	SN74AALS574BN
U17	1820-2724	0		IC LCH TTL/ALS TRANSPARENT OCTL	01295	SN74ALS573CN
U18	1820-2724	0		IC LCH TTL/ALS TRANSPARENT OCTL	01295	SN74ALS573CN
U19	1820-2724	0		IC LCH TTL/ALS TRANSPARENT OCTL	01295	SN74ALS573CN
U20	1820-2724	0		IC LCH TTL/ALS TRANSPARENT OCTL	01295	SN74ALS573CN
XU8	1200-0567	1	1	SOCKET-IC 28-PIN DIP DIP-SLDR	09922	DILB28P-308T
Y1	0410-1386	8	1	CRYSTAL- QUARTZ 8MHZ HC-49/8-HLDR	28480	0410-1386

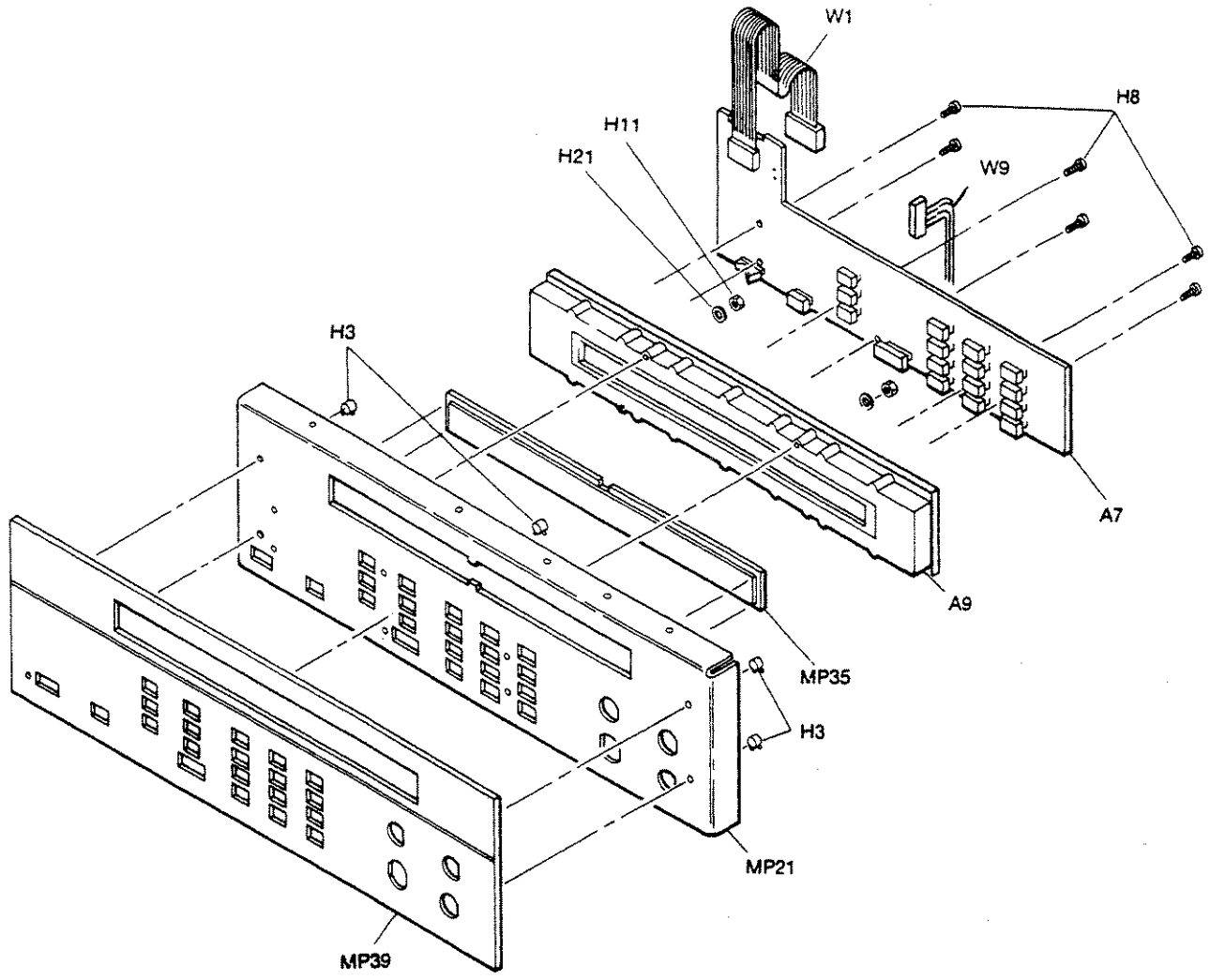
See introduction to this section for ordering information



NOTE

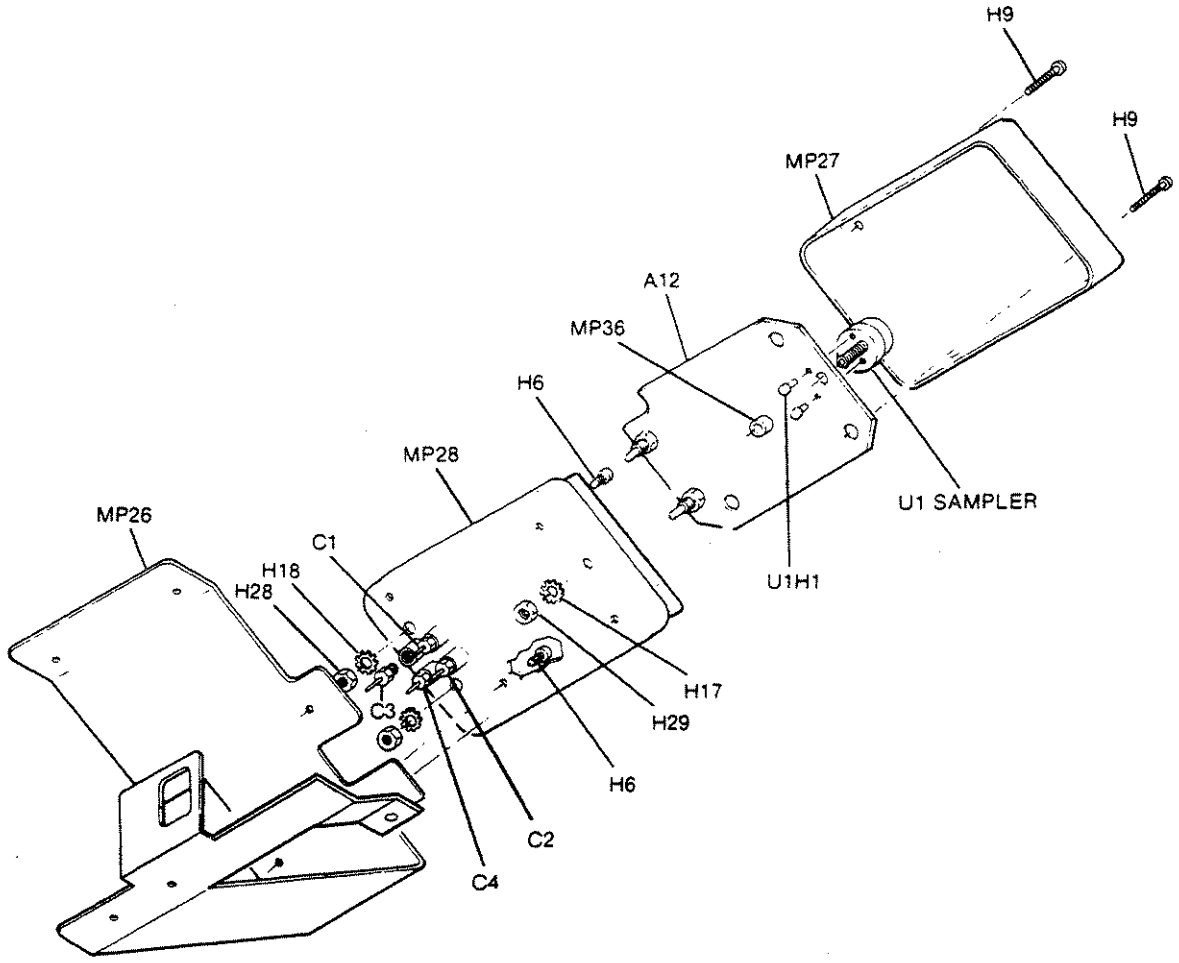
REFER TO PAGES 2-33 THROUGH 2-35 FOR PART NUMBERS FOR CHASSIS PARTS AND HARDWARE.

Figure 3-1. HP 5361B Exploded View



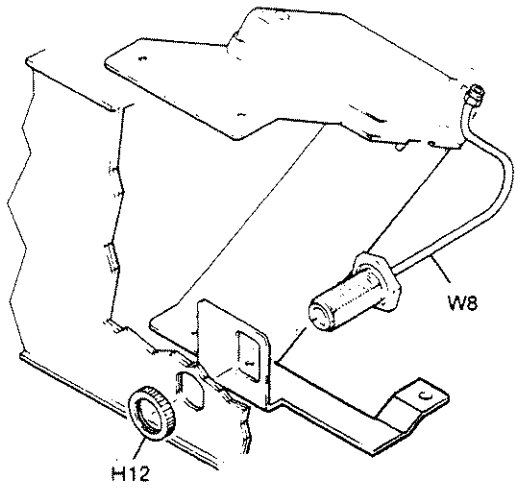
Reference Designation	HP Part Number	CD	Description
A7	05361-60007	5	KEYBOARD/ASSEMBLY
A9	05350-60019	6	DISPLAY/DRIVER ASSEMBLY
H3	0510-1148	2	RETAINER-PUSH ON KB-TO-SHIFT EXT
H8	0515-0897	6	SCREW-MACH M3 ×0.5 8MM-LG PAN-HD
H11	0535-0004	9	NUT-HEX DBL-CHAM M3 ×0.5 2.4MM-THK
H21	2190-0644	3	INTERNAL STAR WASHER
MP21	05350-00002	1	PANEL-SUB
MP25	05350-00007	6	SHIELD DISPLAY
MP35	05350-20203	6	WINDOW
MP39	05361-00001	2	PANEL-FRONT
W1	05350-60105	1	CBL AY-KEYBOARD
W9	05350-60122	2	CBL AY-DISPLAY

Figure 3-2. Front Panel Parts



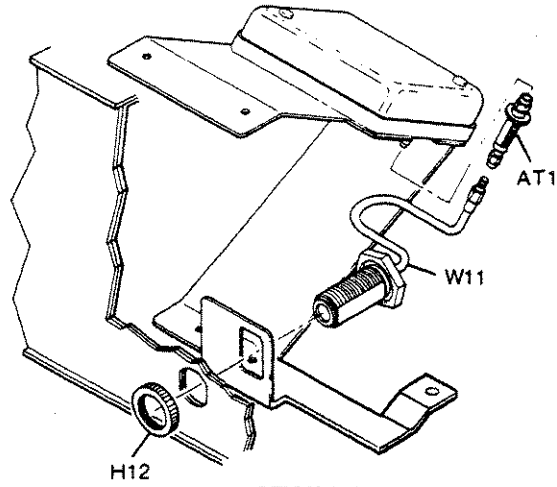
Reference Designation	HP Part Number	CD	Description
A12	05361-60012	2	MICROWAVE ASSEMBLY
C1	0160-0576	5	CAPACITOR-FDTHRU 5000PF +0 –20% 200V
C2	0160-0576	5	CAPACITOR-FDTHRU 5000PF +0 –20% 200V
C3	0160-0576	5	CAPACITOR-FDTHRU 5000PF +0 –20% 200V
C4	0160-3875	3	CAPACITOR-FDTHRU 5000PF +0 –20% 200V
H6	0515-0886	3	SCREW-MACH M3 ×0.5 6MM-LG PAN-HD
H9	0515-1060	7	SCREW-MACH M3 ×0.5 25MM-LG PAN-HD
H17	2190-0084	5	WASHER-LK INTL T 1/4 IN .256-IN-ID
H18	2190-0124	4	WASH-LK T NO. 10 .195-IN-ID
H28	2950-0078	9	NUT-HEX-DBL-CHAM 10-32-THD .067-IN-THK
H29	2950-0196	2	NUT-HEX-DBL-CHAM 1/4-36/THD .06-IN-THK
MP26	05361-00009	7	BRKT, U-WAVE MDL
MP27	05361-00010	8	COVER-SAMPLER
MP28	05350-00010	1	BASE-COVER
MP36	05350-20204	7	SPACER
U1	05361-60204	8	SAMPLER (FOR 5361A AND STANDARD 5361B)
U1	05361-60205	5	SAMPLER (FOR 5361B/OPT. 026/040)
U1H1	0624-0097	9	SCREW-TPG 4040 .188-IN-LG PAN-HD-POZI

Figure 3-3. Microwave Module Parts



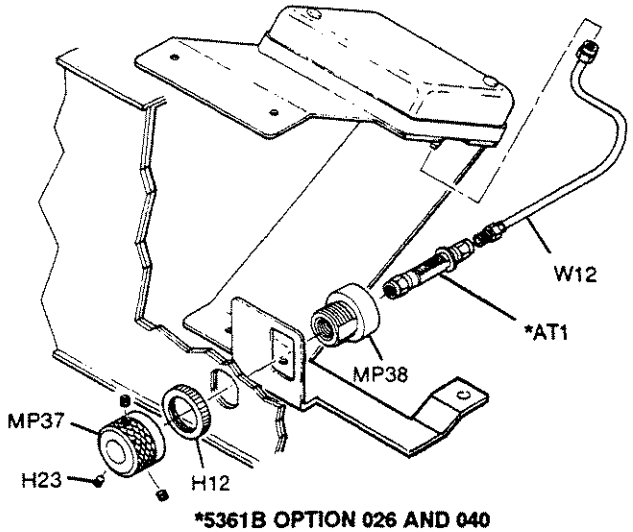
5361B STANDARD

Reference Designation	HP Part Number	CD	Description
H12	0590-0505	1	NUT-KNRLD-R 5/8-24-THD .125-IN-THK
W8	05350-60109	5	SEMI-RIGID ASSY-INPUT



5361B OPTION 006

Reference Designation	HP Part Number	CD	Description
AT1	5088-7049	2	26.5 GHZ LIMITER
H12	0590-0505	1	NUT-KNRLD-R 5/8-24-THD .125-IN-THK
W11	05350-60111	9	SEMI-RIGID ASSEMBLY-LIMITER OPTION

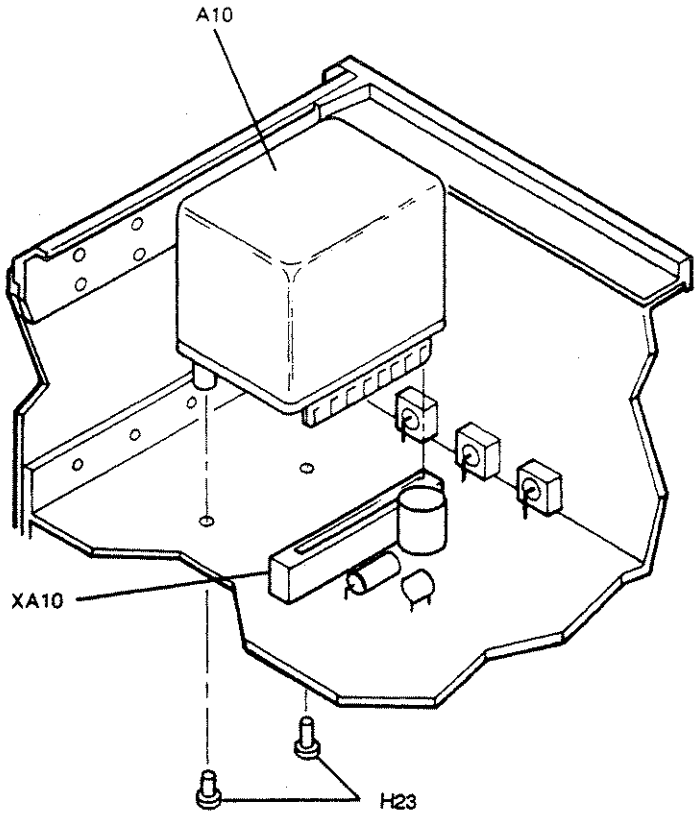


*5361B OPTION 026 AND 040

Reference Designation	HP Part Number	CD	Description
*AT1	5088-7049	2	26.5GHZ LIMITER
H12	0590-0505	1	NUT-KNRLD-R 5/8-24-THD .125-IN-THK
H23	3030-0033	7	SCREW-SET 6-32 .188-IN-LG SMALL CUP-PT
J1	05343-80001	9	INPUT 1 CONNECTOR ASSEMBLY
MP37	05350-20204	8	CONNECTOR-COLLAR
MP38	05350-20201	4	SPACER-THREADED
W12	05351-60101	8	CBL AY-INPUT

*OPTION 006 AND 040 ARE NOT COMPATIBLE. THUS, FOR THE ADJACENT FIGURE TO APPLY TO OPTION 040, OMIT THE LIMITER (AT1).

Figure 3-4. INPUT 1 Connectors



Reference Designation	HP Part Number	CD	Description
A10Y1	10811-60111	8	OPTION 001 OVEN OSCILLATOR
A10Y1	10811-60211	9	OPTION 010 HIGH STABILITY TIMEBASE
H23	2360-0115	4	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI

Figure 3-5. Option 001 and 010 Oven Oscillators

Table 3-5. Manufacturer's Code List

Mfr Code	Manufacturer Name	Address	Zip Code
01433	AB ELEKTRONIK GMBH	SALZBURG AU	A-501
03841	WICKMANN-WERKE A G	WITTEN-ANNEN GM	5870
08439	ROEDERSTEIN/RESISTA GMBH	LANDSHUT GM	8300
K8479	HOLSWORTHY ELECTRONICS LTD	HOLSWORTHY EG	
S0562	TOSHIBA CORP	TOKYO JP	
00000	ANY SATISFACTORY SUPPLIER		
00779	AMP INC	HARRISBURG PA US	17111
01295	TEXAS INSTRUMENTS INC	DALLAS TX US	75265
01686	RCL ELECTRONICS INC	NORTHBROOK IL US	60062
02114	FERROXCUBE CORP	SAUGERTIES NY US	12477
02768	ITW FASTEX	DES PLAINES IL US	60016
04072	BELL INDUSTRIES INC MILLER JW DIV	COMPTON CA	90224
04099	CAPCO INC	LUBBOCK TX	79407
04222	AVX CORP	GREAT NECK NY US	11021
04713	MOTOROLA INC	ROSELLE IL US	60195
05216	PHOENIX TRANSFORMER CO	PHOENIX AZ US	85040
05245	CORCOM INC	LIBERTYVILLE IL US	60048
06132	COMPUTER TERMINAL CORP	SAN ANTONIO TX	78784
06560	JEFFERS ELECTRONICS INC	NOGALES AZ US	85621
07393	COLSON CORP THE	JONESBORO AR	72401
09535	JOHNSON MATTHEY AND MALLORY LTD	TORONTO CN	
09969	DALE ELECTRONICS INC	YANKTON SD US	57078
18546	VARO INC	GARLAND TX US	75046
10392	GENERAL STAPLE CO INC	NEW YORK NY	10010
10454	GENERAL MFG CO	GLENDALE CA	91201
11214	HARDIGG IND INC	S DEERFIELD MA	01373
11236	CTS CORP	ELKHART IN US	46514
11383	AMETEK/ALUMINUM EXTRUSION	LOS ANGELES CA	90065
11502	IRC INC	BOONE NC US	28607
11961	SEMICON INC	BURLINGTON MA	01803
12344	TALLY CORP	KENT WA	98031
12360	ALBANY PROD CO DIV OF PNEUMO DYN	NORWALK CT	06850
12403	CANFIELD H O CO OF INDIANA INC THE	SEYMOUR IN	47274
12406	ELPAC INC	IRVINE CA	92664
12498	CRYSTALONICS, DIV TELEDYNE	CAMBRIDGE MA	02140
12515	TELEDYNE THERMATICS	ELM CITY NC	27822
12703	JUDD WIRE	TURNERS FALLS MA	01376
13103	THERMALLOY INC	DALLAS TX US	75234
16179	M/A-COM INC	BURLINGTON MA US	01803
17856	SILICONIX INC	SANTA CLARA CA US	95054
18310	CONCORD ELECTRONICS CORP	NEW YORK NY	10012
18324	SIGNETICS CORP	SUNNYVALE CA US	94086
18565	CHOMERICS INC	WOBURN MA	01801
19701	MEPCO/CENTRALAB INC	RIVIERA FL US	33404
2M627	ROHM CORP	IRVINE CA US	92713
24226	GOWANDA ELECTRONICS CORP	GOWANDA NY US	14070
24444	GENERAL SEMICONDUCTOR IND INC	TEMPE AZ US	85281
24931	SPECIALTY CONNECTOR CO	FRANKLIN IN US	46131
25403	NV PHILIPS ELCOMA	EINDHOVEN NE	02876
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA CA US	95052
27264	MOLEX INC	LISLE IL US	60532
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
30161	AAVID ENGINEERING INC	LACONIA NH US	03247
32159	WEST-CAP ARIZONA	SAN FERNANDO CA US	91340
32997	BOURNS INC	RIVERSIDE CA US	92507
34333	SILICON GENERAL INC	SAN JOSE CA US	95134
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE CA US	94086
34371	HARRIS CORP	MELBOURNE FL US	32901
34649	INTEL CORP	SANTA CLARA CA US	95054
50088	SGS-THOMSON MICROELECTRONICS INC	PHOENIX AZ US	85022
52648	PLESSEY SEMICONDUCTORS	SANTA ANA CA	92705
52763	STETTNER & CO	LAUF GM	D-856
54294	SHALLCROSS INC	NORTHBROK IL US	60062
55285	BERGQUIST CO	MINNEAPOLIS MN	55420
56289	SPRAGUE ELECTRIC CO	LEXINGTON MA US	02173
59880	THOMSON J L RIVET & MACH CO	WALTHAM MA	02154
71468	ITT CORP	NEW YORK NY US	10022
71785	TRW INC	CLEVELAND OH US	44124
73138	BECKMAN INDUSTRIAL CORP	FULLERTON CA US	92635
73957	GROOV-PIN CORP	RIDGEFIELD NJ	07657
75915	LITTELFUSE INC	DES PLAINES IL US	60016
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF	ELGIN IL	60126
78553	TINNERMAN PRODUCTS INC	CLEVELAND OH	44101
79963	ZIERICK MFG CO	MT KISCO NY	10549
82567	REEVES HOFFMAN	CARLISLE PA	17013
9N171	UNITRODE CORP	LEXINGTON MA US	02173
91506	AUGAT INC	MANSFIELD MA US	02048
91637	DALE ELECTRONICS INC	COLUMBUS NE US	68601
98291	ITT SEALECTRO CORP	TRUMBULL CT US	06611

4

MANUAL CHANGES

4-1. INTRODUCTION

This section contains information necessary to adapt this manual to apply to the HP 5361A instruments.

4-2. MANUAL CHANGES

This manual applies directly to HP 5361B Pulse / CW Microwave Counters with the serial prefix 3023.

As engineering changes are made, newer instruments may have higher serial prefix numbers than the one shown on the title page of this manual. The manuals for these instruments will be supplied with MANUAL CHANGES sheets containing the required information Replace the affected pages or modify existing manual information as directed in the MANUAL CHANGES pages. Contact the nearest Hewlett-Packard Sales and Support Office (listed at the back of this manual) if the change information is missing.

4-3. OLDER INSTRUMENTS

To adapt this manual to all HP 5361A instruments, perform the backdating that is listed in *Table 4-1.*

Table 4-1. Manual Backdating

IF INSTRUMENT HAS SERIAL NUMBER	MAKE THE FOLLOWING CHANGES TO YOUR MANUAL
FOR HP 5361A: All Serial Prefix Numbers All Serial Prefix Numbers	 1 2
FOR HP 5361B A4 Microprocessor Assembly Date code 92015	 3
5361B Serial Number 3023A00370	4

CHANGE 1

Make this change for HP 5361A instruments that contain the old A4 Microprocessor Assembly (05361-60004).

Table 3-3. Standard Instrument Replaceable Parts, A4 MICROPROCESSOR ASSEMBLY:

> Replace pages 3-15 and 3-16 with the revised pages 3-15 and 3-16 supplied in this section (the revised pages are placed at the back of this section).

Table 3-4. Replaceable Parts for Options:

> Delete A4U8, 05361-80010; 2; 1; EPROM (FOR STD 5361B, 5361B/OPT 026); 28480

> Delete A4U8, 05361-80011; 3; 1; EPROM (FOR 5361B/OPTION 040); 28480

> Delete the A12 Option 040 parts list.

Section 5-35. A4 Microprocessor Assembly Troubleshooting:

> Change the A4 Microprocessor Assembly troubleshooting procedures to read as follows:

5-35. A4 MICROPROCESSOR ASSEMBLY TROUBLESHOOTING

Diagnostics that may indicate an A4 Assembly failure:

- Diagnostic 41: RAM Test
- Diagnostic 42: ROM Test
- Diagnostic 43: Repeated Reset sequence

Points to consider when troubleshooting the A4 Assembly:

- Diagnostic 40 (Firmware revision code) should be used to confirm that the latest firmware is installed in the counter.
- The microprocessor itself (A4U2) must be functioning correctly for the instrument to begin its power-up cycle. A possible cause of failure to power on properly could be the L μP RST (Reset) and L μP NMI (Non-Maskable Interrupt) signals generated in the Power Supply control circuit on the A1 Assembly. Refer to the A8/A1 Power Supply Troubleshooting procedures for a description of these signals.

Possible symptoms of a faulty A4 Microprocessor Assembly:

- Instrument fails to initiate its power-on sequence properly.
- LCD display is blank or displays nonesense characters.
- Instrument fails to make measurements at both inputs, even though the power supplies and A3 Counter Assembly have been verified.

CHANGE 1 (Continued)

To troubleshoot the A4 Assembly, perform the following procedures:

Verify the following power supplies:

SUPPLY NAME	A4 TEST POINT	ACCEPTABLE RANGE
+5V	C28(+)	+4.8 to +5.2V
+Vcc	+Vcc test pin	+4.8 to +5.2V
+5V μP	U2(21) (measured when counter is in Standby mode)	+4.8 to +5.2V
+5V MEM	C23(+)	+4.8 to +5.2V

If the instrument fails to power on properly, verify the following signals:

1. The L_μP_RST signal (Test Point RST) at A4U2(6) should be a TTL high less than 200 ms after power is switched on.
2. The L μP NMI signal at A4U2(4) should be a TTL high.
3. The IRQ signal (Test Point IRQ) to A4U2(5) should be a dc level (i.e., no activity). It may be either a TTL high or low, but it should be a constant level. When checking this signal, disconnect the controller if one is being used, and do not press any front panel keys (doing either of these will cause activity on this line).
4. The clock signal (Test Point CLK) from A4U2(40) should be 2 MHz squarewave at TTL levels.

If the above signals are incorrect, trace back through the circuitry to determine the cause.

Section 5-61. A4 Microprocessor Assembly (Block Diagram Description):

In the fourth paragraph of this section:

- Change "8K byte" to "2K byte"
- Change "64K byte" to "32K/64K byte"

Section 5-138. A4 Microprocessor Assembly (Detailed Circuit Description):

- Replace text in Section 5-138 with the following text:

5-138. A4 Microprocessor Assembly

The A4 Microprocessor (MPU) Assembly controls the overall operation of the counter. This assembly receives instructions via the front panel keyboard or HP-IB interface, and sends instructions and data to the front panel display, HP-IB interface, synthesizer, and counter circuitry to control the measurement.

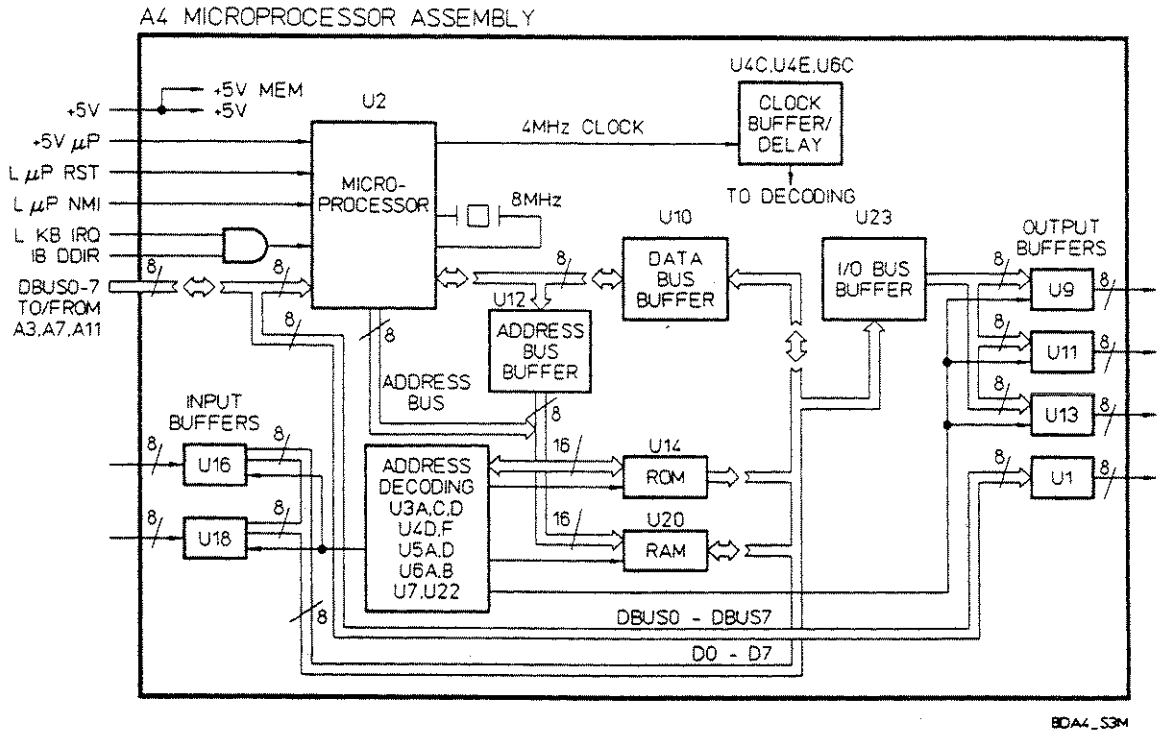


Figure 5-7A. A4 Block Diagram

The A4 Assembly (see *Figure 5-7A*) consists of the microprocessor (U2), a 36K/64K byte ROM IC (U14), a 2K Byte RAM IC (U20), two input buffers (U6, U18), four output buffers (U1, U9, U11, U13), an address buffer (U12), two data buffers (U10, U23), an I/O decoder logic (U7), and miscellaneous enabling and clock delay gates (u3, U4, U5, U6, U22). There are five main tasks the microprocessor executes: read from ROM, read and write to RAM, write to output buffers, read from input buffers, and transfer data over the two on-board bidirectional data buses.

All control functions are performed by LSI NMOS Motorola 6803 microprocessor. The processor contains an 8-bit CPU, 64 bytes of power-dowm RAM, 64 bytes of nonpower-down RAM, three 8-bit I/O ports, one 5-bit I/O port, clock generating circuitry, a programmer timer, and interrupt logic. The microprocessor performs all I/O transfers by reading and writing to memory (memory-mapped I/O), and uses seven 8-bit ports and one 5-bit port on the A4 Assembly for communication with other circuit assemblies. Three Static Output Ports (SOPRT1, SOPRT2, SOPRT3) are used for controlling other circuit assemblies, and two Static Input Ports (SIPRT1, SIPRT2) are used to sample circuit conditions in the instrument. An 8-bit Data Port (DPRT1) and a 5-bit Data Port (DPRT2) are used for bidirectional data transfer between other assemblies and the microprocessor.

RESET SEQUENCE. Microprocessor activity begins with the Reset sequence, after the +5V supply is first turned on. On the rise of the +5V supply, processor activity is held back by a logic low on the L μP RST line, U2(6). The L μP RST line, which comes from the Power Supply Control circuit on the A1 Assembly, goes logic high after a minimum delay of 100 ms, and then processor execution begins. The 100 ms delay enables the clock circuits in the 6803 to stabilize. The L μP RST line also gates the ~φ2 signal at U6C; no bus activity occurs when the L μP RST line is low.

At power-up, the microprocessor is latched into its proper operating mode by the setup conditions at U2(8-12). The latching of the operating mode is explained in more detail in the paragraph titled "Latching the Operating Mode", but for now it is only necessary to know that once the operating mode is set, the processor reads from a preset address (0FFFE;0FFFF). The addressed memory location contains the starting address of the operating program.

ADDRESSING AND DATA TRANSFER. The 6803 uses an 8-bit multiplexed address/data port (A/D0 - A/D7). This port is demultiplexed by latch U12 to provide the lower 8 bits of the on-board address bus (A0 - A7). The upper 8 bits of the address bus (A8 - A15) come directly from U2(22-29). The required address lines are applied directly to ROM U14 and RAM U20. The lower 8 bits of the address are latched by U12 on the falling edge of the strobing pulse from U2(39), causing the address to applied to U14 and U20 the remainder of the memory of the memory access cycle.

The multiplexed address/data lines are buffered by bidirectional transceiver U10 to provide the on-board 8-bit data bus (D0 - D7). The level at the DIR input at U10(1) determines the direction of the data transfer. The U10 outputs are enabled by the rising edge of a delayed and inverted system clock signal(~φ2D) so that U10 outputs are tri-stated during the address portion of the multiplexed bus cycle.

READ FROM ROM. ROM U14 is an NMOS LSI 32K/64K device, providing ROM space of 32K/48K bytes. It has 2 enable lines, 15/16 address lines, and 8 three-state data lines. The ROM is enabled when both the E (Enable) input at U14(20) and the OE (Output Enable) input at U14(22) are LOW. The E input is grounded so the device is always enabled. The ~ROMOE line is the logic-AND result (active low from U6B) of the delayed system clock (φ2D) with the upper two address lines (A15 and A14 via U3D and U6A). The delayed clock ensures that the device is not enabled during the address portion of the multiplexed bus cycle.

The address space of the ROM covers all addresses in which lines A14 and A15 are true. U3D and U6A provide the signal for both ROM address decoding (U6B) and non-ROM address decoding.

CHANGE 1 (Continued)

When the OE enabling line is low, the data from the addressed location appears on the data lines. The data is held until the OE input goes high. THe 6803 reads data on the bus on the falling edge of the system clock.

RAM READ AND WRITE. The RAM U20 is a 2K byte CMOS static RAM device. U20 has 3 enable lines, 11 address lines, and 8 bidirectional data lines. The CS (Chip Select) input at U20(18) is active low, and goes high to power-down the RAM during the address part of the multiplexed bus cycle to save power. The OE (Output Enable) input is always high during a write, and will be discussed later.

The ~RAMWE (Write Enable) signal at U20(21) is active low during a write. The ~RAMWE signal comes from NAND gate U22B, the inputs to which are the ~R/W line (active high during a write), the system clock, $\varphi 2$ (active high when data valid), ~ROM (active high outside the ROM's address space), and address line A13. Once enabled, data on the I/O lines at U20 (9-11, 13-17) is stored into memory on the rising edge of the WE signal. This completes the write cycle to RAM.

The read from RAM cycle is similar to the read from ROM cycle, but different decoders enable the devices. The ~RAMOE signal is driven by U22A from the logic-AND (active low0 of the R/~W line (active high during a read), the delayed system clock ($\varphi 2D$), ~ROM line (active high outside the ROM's address space), and address line A13. The ~RAMWE line is held high during the read operation.

READ FROM INPUT PORT. Status condition signals form other circuits are received at the SIPRT1 and SIPRT2 input ports, using 8-bit latches with three-state outputs (U16 and U18) as input buffers. Reading from an input port is similar to reading from the RAM, but different decoding is used. The Decoder U7 is enabled by three inputs, the inverted and delayed system clock ($\sim\varphi 2D$) from gate U4E, the ROM signal (active low) from U6A, and the AND product of ~A13, A12, and ~A11 (via U3A, U4D, U4F, and U5D). The selection inputs to U7 are the R/~W line and address lines A2 and A3. U7 provides active low outputs to drive the select line on the input and output ports. When the enable signal is low, data at the buffer inputs U16(2-9) and U18(2-9) is transferred onto the data bus (D0-D7). The processor reads this data on the falling edge of the system clock ($\varphi 2$), and the decoder disables the buffers before the next cycle begins.

WRITE TO OUTPUT PORT. Control signals to other circuits are transferred via the SOPRT1, SOPRT2, and SOPRT3 output ports, using 8-bit flip-flops U9, U11, and U13 as output buffers. The data signal paths for writing to an output port are similar to writing to RAM while the control signals are similar to reading an input port. The inverted system clock ($\sim\varphi 2$) U9(11), U11(11), and U13(11) is used to latch the data (SOBUS0-SOBUS7) to the buffer outputs. Data transfer through each buffer is enabled only when the corresponding enable signal from I/O Decoder U7 is active low and the $\sim\varphi 2$ signal makes the low-to-high transition. The outputs of U9, U11, and U13 are totem-pole outputs; thus, they are always active.

DATA PORT READ AND WRITE. The microprocessor uses two of its ports as static data buses for data transfer to and from other assemblies. Data Port 1 (DPRT1) is an 8-bit bidirectional port which is used for all data transfers directly to and from the processor via the DBUS0-DBUS7 lines. Three lines of 5-bit Data Port 2 (DPRT2) are used for handshaking with the HP-IB processor on the A11 HP-IB Interface Assembly. The three handshake lines (IB DVAL, IB DREC, IB DDIR) at U2(10,11,12), provide synchronization between the two asynchronous processors. The fourth DPRT2 line (L KB IRQ) is used to detect an interrupt caused by a front panel key being pressed. The fifth DPRT2 line is not used.

The pins of the DPRT1 and DPRT2 ports are individually programmable to be either inputs or outputs. Pull-up resistors R1, R2, and resistor network R3, make the DPRT1 and DPRT2 lines high level when configured ad inputs. When configured as outputs, the DPRT1 and DPRT2 lines are totem-pole outputs. A read or write via the DPRT1 and DPRT2 ports is controlled entirely within the 6803 processor.

WRITE TO SYNTHESIZER ASSEMBLY. The microprocessor programs the A5 Synthesizer Assembly via 8-bit latch U1. A write to the synthesizer is similar to writing to one of the SOPRT output ports, except that the latching signal (SYN LCH) comes from U9(9) via the motherboard. The u1 latch is always enabled by a ground connection at U1(1).

LATCHING THE OPERATING MODE. The 6803 processor is basically a 6801 single-chip microcomputer operating in mode 2. The operating mode is established on the rising edge of the L μP RST signal from the A1 Assembly. R12 and C24 produce a ramp input at U2(6). CR1 and CR2 are held low (1.5 Vdc maximum) by the L μP RST line and the processor reads DPRT2 at U2(8,9,10) to establish the mode. The levels read by the processor are 010 (binary 2), i.e., mode 2. After L μP RST goes high, CR1 and CR2 have no effect and DPRT2 operates as a bidirectional data port.

ENABLING AND CLOCK DELAY GATES. The 6803 processor provides a single system clock output (φ2) at U2(40). A number of delayed and/or inverted clock signals are derived from the single clock by hex inverter U4. The φ2 system clock at U2(40) is a 4 MHz squarewave which is active high for data valid and active low for address valid. Individual devices on the A4 Assembly are enabled based on two things: the address decoding logic, and a precisely timed edge of the system clock. The decoding logic outputs have many propagation delays, and are used only for device selection, not device de-selection. The ~R/W line is also used in some of the decoding: it is not used for device de-selection.

The φ2 signal is used to terminate the write to RAM so that the cycle ends **before** the outputs of the processor go to their three-state mode and write erroneous information to the RAM. An inverted clock signal (φ2) is used to terminate the write to the output buffers, for the same reason.

CHANGE 1 (Continued)

The delayed clock signals are used for de-selection of devices. A delayed version of the noninverted clock (φ2D) is provided by U4C. The φ2D signal is used to terminate the read from RAM so that the RAM hold its data for 10 ns after the 6803 reads it.

CRYSTAL CLOCK. The 6803 has an internal clock generating circuit which requires only an external 8 MHz crystal (Y1) and the proper load capacitance (C1, C3). The 8 MHz crystal frequency is divided by 4 to give a system clock frequency of 4 MHz.

POWER SUPPLY DECOUPLING. The +5V supply from the A8 Motherboard Assembly supplies Vcc for all the A4 circuitry except the memory devices. To keep power dissipation low, the RAM memory (U20) is turned on and off at a 4 MHz rate (on when data is valid). This generates system noise, so L2 and C23 provide extra filtering between the +5V MEM supply for the RAM, ROM, and timer, and the +5V supply for the rest of the A4 Assembly.

INTERRUPTS. Two interrupt inputs to the processor are available in addition to the L μP RST input. The L μP NMI input at U2(4) is a nonmaskable interrupt which is used in power-down situations to signal the CPU to save the contents of the internal standby RAM. This signal comes form the Power Supply Control circuit on the A1 Assembly.

The IRQ input at U2(5) is an active low maskable interrupt enabled by either HP-IB communication (IB DDIR) or the front panel keyboard when a key is pressed (L KB IRQ). The two interrupts are ANDed by U5B, and the output at U5(6) is applied to the IRQ input. When the processor is interrupted, it scans the DPRT2 lines to determine whether the L KB IRQ line at U2(8) or the IB DDIR line at U2(12) has gone low, and executes the appropriate program based on which interrupt occurred.

STANDBY RAM. A separate +5V standby supply (+5V μP) is available at U2(21), supplied from the Timebase Buffer circuit on the A1 Assembly. This voltage is always present when the instrument is connected to ac power, thus keeping the power-down RAM contents valid.

Section 5-146. Schematic Diagrams, A4 Microprocessor Assy Schematic Diagram:

> Replace page 5-203 with the revised page 5-203 supplied in this section (placed at the back of this section).

CHANGE 2

Make this change for HP 5361A instruments that contain the Revision C, A14 Gate Board Assembly.

Table 3-3. Standard Instrument Replaceable Parts, A14 GATE BOARD ASSEMBLY:

> Delete A14U36; 1820-2686; 3; 1; IC GATE TTL; 28480; 1820-2686.

Section 5-146. Schematic Diagrams, A14 Gate Board Assembly Schematic Diagram (Sheet 2 of 4)

> Delete U36A, and connect U14A(4) directly to the L TTL E RST line (U30 pin 11).

> Delete U36 from A14 component locator.

CHANGE 3

Make this change for HP 5361B instruments with A4 Microprocessor boards below 92051:

Table 3-3. Standard Instrument Replaceable Parts, A4 MICROPROCESSOR ASSEMBLY:

> Change A4U14 part number from 1821-0321 to 1820-2757, IC FF TTL ALS POS-EDGE-TRIG; 01295; SN74ALS574BN.

CHANGE 4

Make this change for HP 5361B instruments with Serial Numbers below 3023A00370:

Table 3-3. Standard Instrument Replaceable Parts, A5 SYNTHESIZER ASSEMBLY:

> Change A5C44 from 0160-4527 (56PF) to 0160-4511 CAPACITOR-FXD 220PF 5% 200V CER.

> Add A5Q1, Q2, 1855-0540, TRANSISTOR J-FET P-CHAN D-MODE TO-18 SI;27014; 2N5115(SEL).

> Add A5Q8, 1854-0215, TRANSISTOR NPN SI TO-92 PD=350MW; 04713; 2N3904.

> Add A5Q9, 1853-0036, TRANSISTOR PNP SI TO-92 PD=625MW; 04713; 2N3906(SEL).

> Add A5R2, 0698-3155, RESISTOR 4.64K ±1% .125W TF TC=0±100; 12498; CT4-1/8-TO-4641-F.

> Add A5R3 and R39, 0698-3156, RESISTOR 14.7K ±1% .125W TF TC=0+-100; 12498; CT4-1/8-TO-1472-F.

> Change A5R20 from 0698-3152 (3.48K) to 0757-0442, RESISTOR 10K ±1% .125W TF TC=0±100;12498;CT4-1/8-TO-1002-F.

> Add A5R40, 0757-0442, RESISTOR 10K ±1% .125W TF TC=0±100; 12498; CT4-1/8-TO-1002-F.

> Add A5R41, 0757-0465, RESISTOR 100K ±1% .125W TF TC=0+-100;12498;CT4-1/8-TO-1003-F.

Figure 5-22. A5 Synthesizer Assembly Component Locator/Schematic Diagram:

> Replace page 5-211 with the revised page 5-211 supplied in this section (placed at the back of this section.

CHANGE 5

Make this change for HP 5361B instruments with Serial Numbers below 3023A00213:

Table 3-3. Standard Instrument Replaceable Parts, A6 IF AMPLIFIER/DETECTOR ASSEMBLY:

> Delete A6C84, 0160-3875, CAPACITOR-FXD 22PF 200V; change quantity at C32 from 2 to 1.

Figure 5-23. A6 IF Amplifier/Detector Assembly Schematic Diagram:

> Delete A6C84 from the left of U4 and under R3/R4 on A6 component locator.

> Delete A6C84 from between R3 Pin 2 and R4 Pin 2 in the (J) Schmitt Trigger section of sheet 1 of 2.

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	05361-60004	2	1	MICROPROCESSOR ASSEMBLY NOTE EPROM A4U14 IS NOT SUPPLIED AS PART OF THIS BOARD. TO ORDER U14, USE HP PART NUMBER 05361-80004.	28480	05361-60004
A4C1	0160-4787	8	2	CAP-FXD 22PF 100 V	09969	RPA10C0G220J100
A4C2	0160-4557	0	21	CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C3	0160-4787	8		CAP-FXD 22PF 100 V	09969	RPA10C0G220J100
A4C4	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C5	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C6	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C7	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C8	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C9	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C10	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C11	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C12	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C13	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C14	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C16	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C17	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C18	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C19	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C22	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C23	0180-0197	8	1	CAP-FXD 2.2UF 20 V TA	56289	150D225X9020A2
A4C24	0160-4808	4	1	CAP-FXD 470PF 100 V	09969	RPA10C0G471J100V
A4C26	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C27	0180-3775	4	2	CAP-FXD 68UF 10 V TA	12344	T398H686K010AS
A4C28	0180-3775	4		CAP-FXD 68UF 10 V TA	12344	T398H686K010AS
A4C29	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C30	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4C31	0160-4557	0		CAP-FXD 0.1UF 50 V	09969	RPA30X7R104M50V
A4CR1	1901-0050	3	3	DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A4CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A4CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	9N171	1N4150
A4J1	1251-4775	8	1	CONN-POST TYPE .150-PIN-SPCG 10-CONT	28480	1251-4775
A4L1	9140-0990	4	1	INDUCTOR 1UH +-10% .172D-INX.43LG-IN	91637	IMS-5-01 1.0uH +/-10%
A4L2	9100-0541	7	1	INDUCTOR RF-CH-MLD 250UH +-10%	91637	ICS-1041-1
A4MP1	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	73957	GP24-063 X 250-17
A4MP2	4040-0748	3	2	EXTR-PC BD BLK POLYC .062-IN-BD-THKNS	28480	4040-0748
A4P1A	1251-7986	9	2	CONN-POST TYPE .100-PIN-SPCG 50-CONT	28480	1251-7986
A4P1B	1251-7986	9		CONN-POST TYPE .100-PIN-SPCG 50-CONT	28480	1251-7986
A4R1	0757-0449	6	2	RESISTOR 20K +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-2002-F
A4R2	0757-0449	6		RESISTOR 20K +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-2002-F
A4R3	1810-0398	9	1	NETWORK-RES 10-SIP 22.0K OHM X 9	C1433	750-101
A4R7	0757-0442	9	2	RESISTOR 10K +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-1002-F
A4R12	0757-0442	9		RESISTOR 10K +-1% .125W TF TC=0+-100	12498	CT4-1/8-T0-1002-F
A4U1	1820-2724	0	6	IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
A4U2	1820-3159	7	1	IC-MPU W/2 MHZ CLK,8 BITS,64K ADDRESS	04713	MC68B03L
A4U3	1820-2739	7	1	IC GATE TTL ALS NOR QUAD 2-INP	01295	SN74ALS02N
A4U4	1820-2634	1	1	IC INV TTL ALS HEX	01295	SN74ALS04BN
A4U5	1820-2635	2	1	IC GATE TTL ALS AND QUAD 2-INP	01295	SN74ALS08N
A4U6	1820-2775	1	1	IC GATE TTL ALS NAND TPL 3-INP	01295	SN74ALS10AN
A4U7	1820-3100	8	1	IC DCDR TTL ALS BIN 3-TO-8-LINE 3-INP	01295	SN74ALS138N
A4U9	1820-1858	9	4	IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
A4U10	1820-3121	3	1	IC TRANSCEIVER TTL ALS BUS OCTL	01295	SN74ALS245AN
A4U11	1820-1858	9		IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
A4U12	1820-2724	0		IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
A4U13	1820-1858	9		IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
A4U14	(SEE NOTE ABOVE)	4	1	EPROM PBM	28480	SEE NOTE ABOVE
A4U15	1820-1858	9		IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
A4U16	1820-2724	0		IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
A4U17				NOT ASSIGNED		

See introduction to this section for ordering information

Table 3-3. Standard Instrument Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4U18	1820-2724	0		IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
A4U19	1820-2724	0		IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
A4U20	1LJ6-0001	7	1	SRAM 2KX8 120NS	28480	1LJ6-0001
A4U22	1820-2689	6	1	IC GATE TTL F NAND DUAL 4-INP	18324	74F20N
A4U23	1820-2724	0		IC LCH TTL ALS TRANSPARENT OCTL	01295	SN74ALS573BN
A4W1	8159-0005	0	1	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	11502	YZO 1/4
A4XU8	1200-0639	8	2	SOCKET-IC-DIP 20-CONT DIP DIP-SLDR	01295	C8720-01
A4XU10	1200-0639	8		SOCKET-IC-DIP 20-CONT DIP DIP-SLDR	01295	C8720-01
A4XU14	1200-0567	1	1	SOCKET-IC-DIP 28-CONT DIP DIP-SLDR	01295	C8728-01
A4Y1	0410-1386	8	1	CRYSTAL-QUARTZ 8.000 MHZ HC-49/U-HLDR	28480	0410-1386

See introduction to this section for ordering information

ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN MICROFARADS;
   INDUCTANCE IN MICROHENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. TEST SOCKET XU8 IS USED FOR FACTORY TEST PURPOSES ONLY.
6. THE FOLLOWING COMPONENTS ARE NOT INSTALLED:
   C15, C20, C21, C25, CR4, R9, R10, R11, R13, R14, U15, U17, U19, U21.

REFERENCE DESIGNATORS

A4 ASSEMBLY	
C1-C14, C16-C19, C22-C24, C26-C31	U1-U7, U8-U14, U16, U18, U20, U22, U23
CR1, CR2, CR5	XU8, XU10, XU14
L1, L2	Y1
P1A, P1B	
R1-R3, R7, R12	

REFERENCE DESIGNATOR	HP PART NO.	MFG PART NO.
CR1, CR2, CR5	1901-0050	IN4150
U1, U12, U16, U18, U23	1820-2724	SN74ALS573BN
U2	1820-3159	MC68B03L
U3	1820-2738	SN74LS02N
U4	1820-2634	SN74LS04BN
U5	1820-2635	SN74LS08N
U6	1820-2775	SN74LS10N
U7	1820-3100	SN74LS138N
U8	1820-1858	SN74LS377N
U10	1820-3121	SN74LS245AN
U14	05350-80020	27512
U20	1818-1790	HM6116LP-2
U22	1820-2689	74F20PC

INTEGRATED CIRCUIT VOLTAGE AND GROUND CONNECTIONS

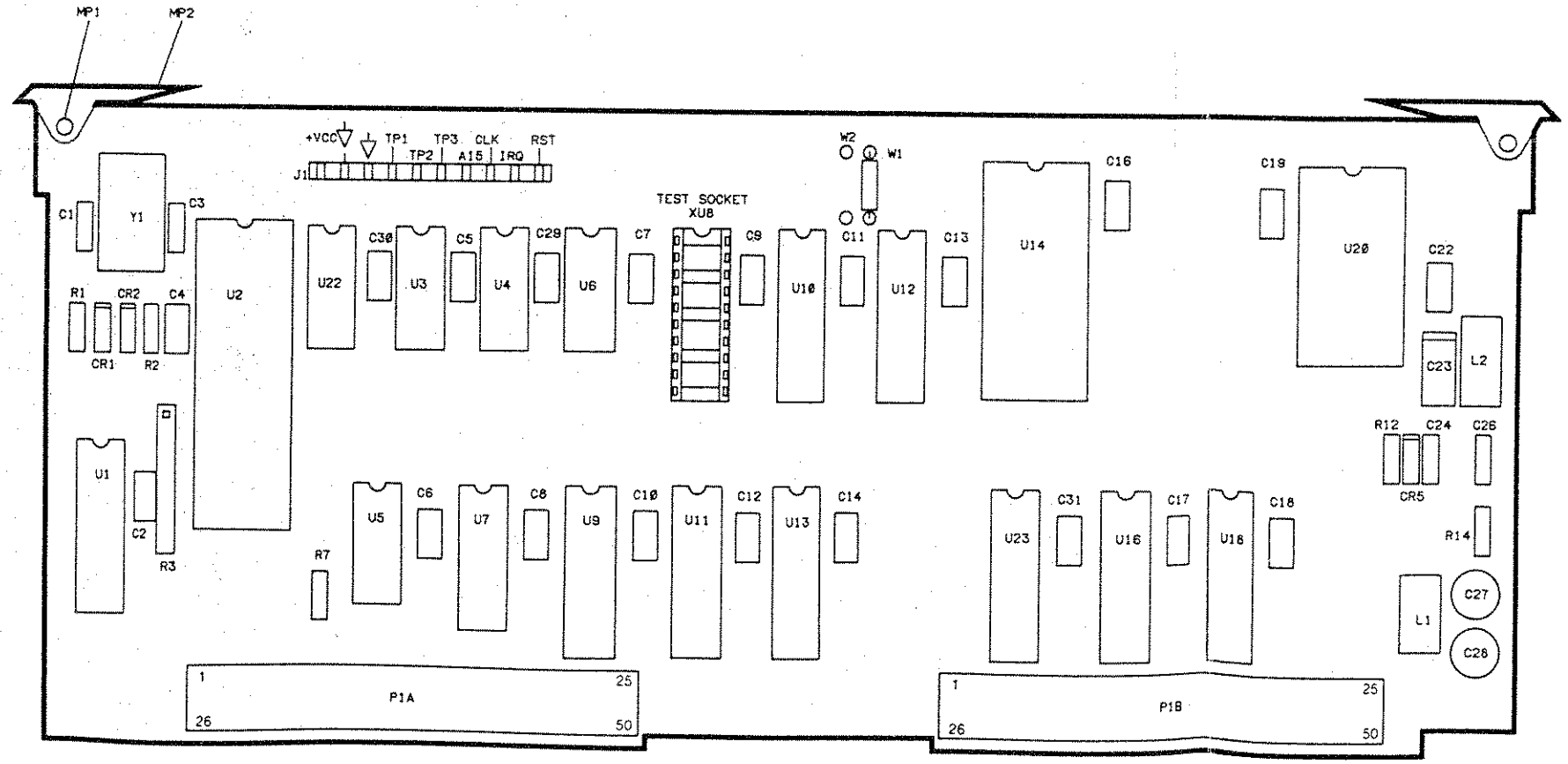
REFERENCE DESIGNATOR	PIN NUMBERS		
	+5V	+5V MEM	GND
U1	20		10
U2	7		1
U3	14		7
U4	14		7
U5	14		7
U6	14		7
U7	16		8
U8	20		10
U10	20		10
U11	20		10
U12	20		10
U13	20		10
U14		28	14
U16	20		10
U18	20		10
U20	24		12
U22	14		7
U23	20		10

NOTE

This A4 schematic diagram and accompanying information apply only to the standard A4 assembly (05361-60004) installed in the 5361A.

SYN DATA 1	26	1	SYN DATA Ø
SYN DATA 3	27	2	SYN DATA 2
SYN DATA 5	28	3	SYN DATA 4
SYN DATA 7	29	4	SYN DATA 6
GND, DIGITAL	30	5	GND, DIGITAL
IB DDIR	31	6	SYN LCH
IB DVAL	32	7	IB DREC
L KB IRQ	33	8	NOT USED
DBUS 1	34	9	DBUS Ø
DBUS 3	35	10	DBUS 2
DBUS 5	36	11	DBUS 4
DBUS 7	37	12	DBUS 6
GND, DIGITAL	38	13	GND, DIGITAL
NC	39	14	L µP RST
NOT USED	40	15	L µP NMI
NC	41	16	+5V µP
L DSP SYNC	42	17	SYN LCH
L DSP PWRON	43	18	L KB READ
L LF TEST	44	19	L µW OFF
LF OUT SEL	45	20	H LF 50
GND, DIGITAL	46	21	GND, DIGITAL
H INTP RST	47	22	L INTP EN
MRC RG0	48	23	L MRC STB
MRC RG1	49	24	H MRC CSEL
H GATE	50	25	H MRC READ

L TEST 1	26	1	L TEST 4
L TEST 3	27	2	L TEST 2
L OVLD RST	28	3	L NO IF RST
L IF OFF	29	4	L IF TEST
GND, DIGITAL	30	5	GND, DIGITAL
NC	31	6	NC
NC	32	7	NC
NC	33	8	NC
NC	34	9	NC
L EXT REF	35	10	L 10MHz OK
H PWRSP OK	36	11	L OVN COLD
NOT USED	37	12	L KB DAVL
L NO IF LCH	38	13	L OVLD LCH
GND, DIGITAL	39	14	GND, DIGITAL
L JMP 1	40	15	L IB SENSE
L JMP 3	41	16	L JMP 2
L JMP 5	42	17	L JMP 4
L JMP 7	43	18	L JMP 6
NC	44	19	NC
NC	45	20	NC
NC	46	21	NC
NC	47	22	NC
GND, DIGITAL	48	23	GND, DIGITAL
+5V	49	24	GND, DIGITAL
+5V	50	25	+5V



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD

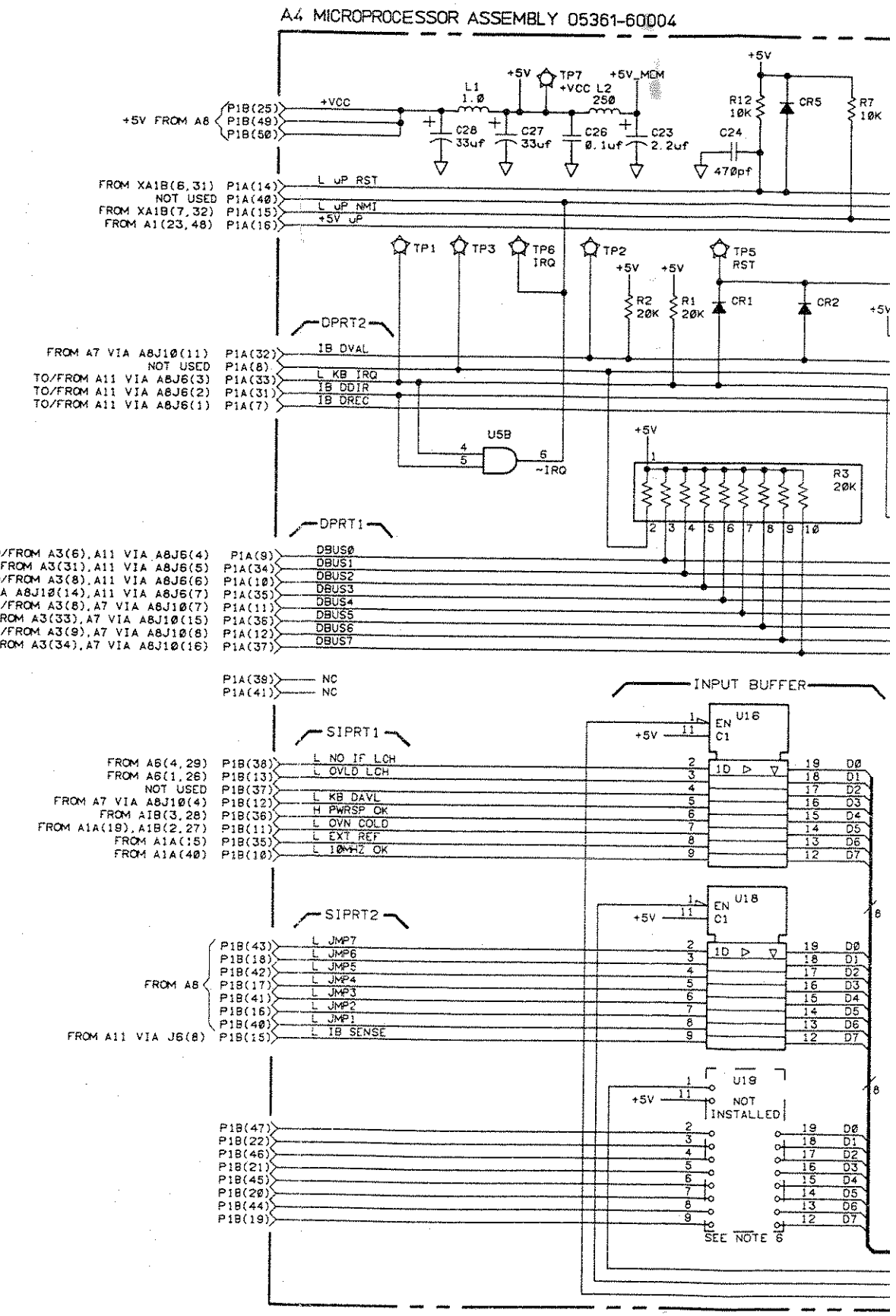
TABLE OF ACTIVE ELEMENTS

REFERENCE	HP PART NO.	MFG PART NO.

XA4A
CONNECTOR PINOUT
CIRCUIT SIDE OF MOTHERBOARD

XA4B
CONNECTOR PINOUT
CIRCUIT SIDE OF MOTHERBOARD

A4 MICROPROCESSOR ASSEMBLY 05361-60004



A4 MICROPROCESSOR ASSEMBLY 05361-60004

DPRT2

FROM A7 VIA A8J10(11) P1A(32) IB DVAL
NOT USED P1A(8)
TO/FROM A11 VIA A8J6(3) P1A(33) L KB IRQ
TO/FROM A11 VIA A8J6(2) P1A(31) IB DDIR
TO/FROM A11 VIA A8J6(1) P1A(7) IB DREC

U5B ~IRQ

DPRT1

TO/FROM A3(6),A11 VIA A8J6(4) P1A(9) DBUS0
TO/FROM A3(31),A11 VIA A8J6(5) P1A(34) DBUS1
TO/FROM A3(8),A11 VIA A8J6(6) P1A(10) DBUS2
A3(32),A7 VIA A8J10(14),A11 VIA A8J6(7) P1A(35) DBUS3
TO/FROM A3(8),A7 VIA A8J10(7) P1A(11) DBUS4
TO/FROM A3(33),A7 VIA A8J10(15) P1A(36) DBUS5
TO/FROM A3(9),A7 VIA A8J10(8) P1A(12) DBUS6
TO/FROM A3(34),A7 VIA A8J10(16) P1A(37) DBUS7

P1A(38) NC
P1A(41) NC

SIPRT1

FROM A6(4,28) P1B(38) L NO IF LCH
FROM A6(1,26) P1B(13) L OVLD LCH
NOT USED P1B(37)
FROM A7 VIA A8J10(4) P1B(12) L KB DAVL
FROM A1B(3,28) P1B(36) H PWRSP OK
FROM A1B(7,32) P1B(11) L OVN COLD
FROM A1A(19),A1B(2,27) P1B(35) L EXT REF
FROM A1A(15) P1B(35) L 10MHZ OK
FROM A1A(40) P1B(10)

SIPRT2

FROM A8 P1B(43) L JMP7
P1B(18) L JMP6
P1B(42) L JMP5
P1B(17) L JMP4
P1B(41) L JMP3
P1B(16) L JMP2
P1B(40) L JMP1
FROM A11 VIA J6(8) P1B(15) L IB SENSE

P1B(47)
P1B(22)
P1B(46)
P1B(21)
P1B(45)
P1B(20)
P1B(44)
P1B(19)

U19 NOT INSTALLED
SEE NOTE 6

INPUT BUFFER

U16 U18

U2

IRQ
P24(TX)
P23(RX)
NMI
STANDBY VCC
P22(SCLK)
P21(TO)
P20(TI)
(PLASTIC)
RST
VSS
Y1
C3 22pf
C1 22pf

INTERNAL PORT 1
P10 DBUS0
P11 DBUS1
P12 DBUS2
P13 DBUS3
P14 DBUS4
P15 DBUS5
P16 DBUS6
P17 DBUS7

R/~W
E
AS

P30 A/D0
P31 A/D1
P32 A/D2
P33 A/D3
P34 A/D4
P35 A/D5
P36 A/D6
P37 A/D7

P40 A8
P41 A9
P42 A10
P43 A11
P44 A12
P45 A13
P46 A14
P47 A15

TP8 A15

+5V FROM A8

P1B(25) P1B(49) P1B(50) +VCC
L1 1.0
TP7 +5V
+5V_MEM +VCC L2 250
C28 33uf
C27 33uf
C26 0.1uf
C23 2.2uf
C24 470pf
R12 10K
CR5
R7 10K

FROM XA1B(6,31) P1A(14) L uP RST
NOT USED P1A(40)
FROM XA1B(7,32) P1A(15) L uP NMI
FROM A1(23,48) P1A(16) +5V uP

TP1 TP3 TP6 IRQ TP2 TP5 RST
R2 20K R1 20K CR1 CR2
R3 20K

ADDRESS BUS BUFFER

U12 A/D0 A/D1 A/D2 A/D3 A/D4 A/D5 A/D6 A/D7 A0 A1 A2 A3 A4 A5 A6 A7

TP4 CLK

U4A ~R/W

U4E ~Ø2D
U4C Ø2D
U6C ~Ø2

DATA BUS BUFFER

U10 A/D0 A/D1 A/D2 A/D3 A/D4 A/D5 A/D6 A/D7

MEMORY

U3D ~ROM
U6A
U6B ~ROMOE
U22A
U22B ~RAMOE ~RAMWE
+5V_MEM

U4F U3A U5A U4D U3C U5D
U7 DMUX
U17 NOT INSTALLED SEE NOTE 6

SEE NOTE 6

R10 100K CR4 R11 10K U21A R13 10K U21B R14 10K C21 1uF R9 20K
C15 0.1 C20 0.1 C25 0.1

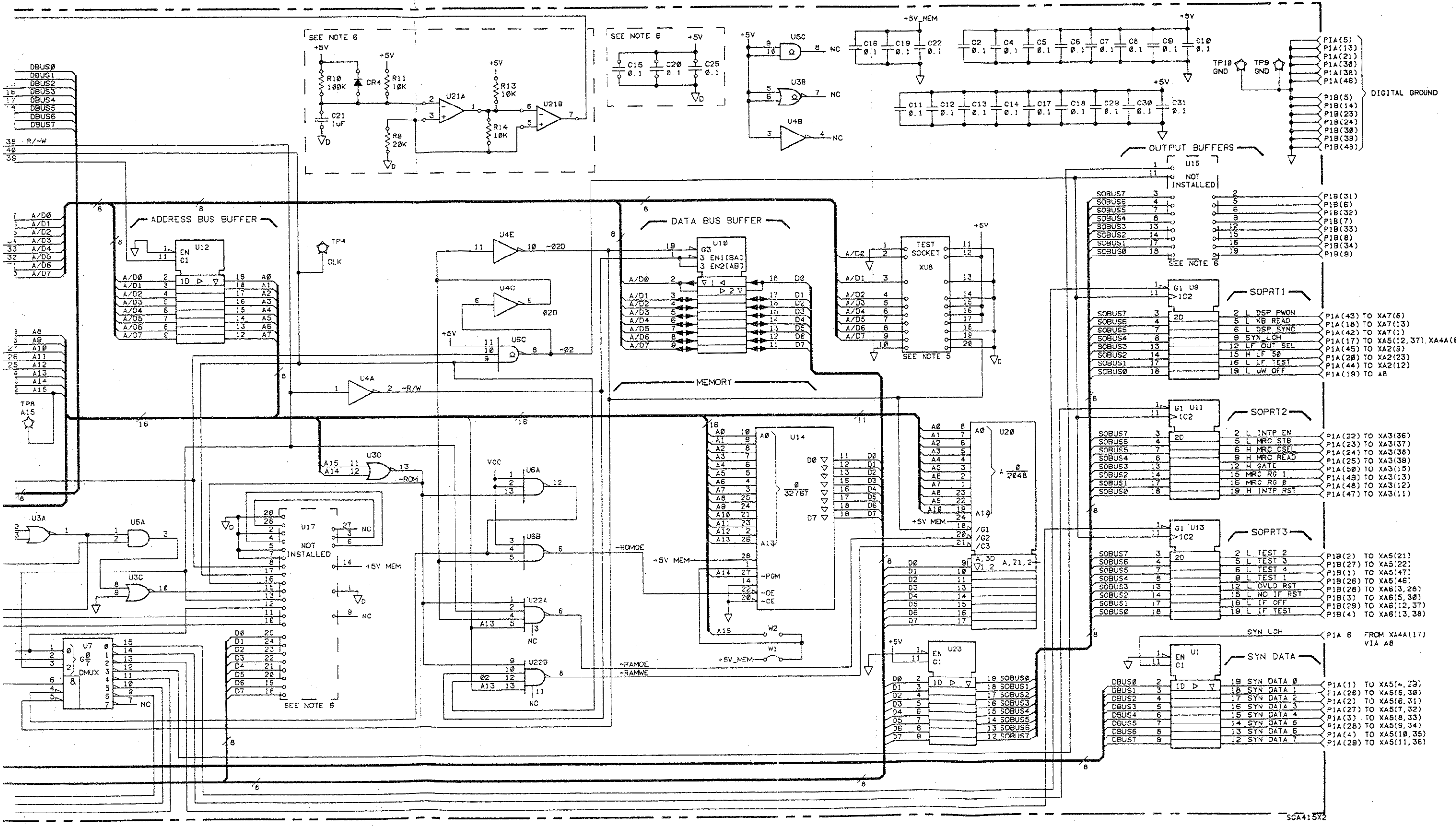
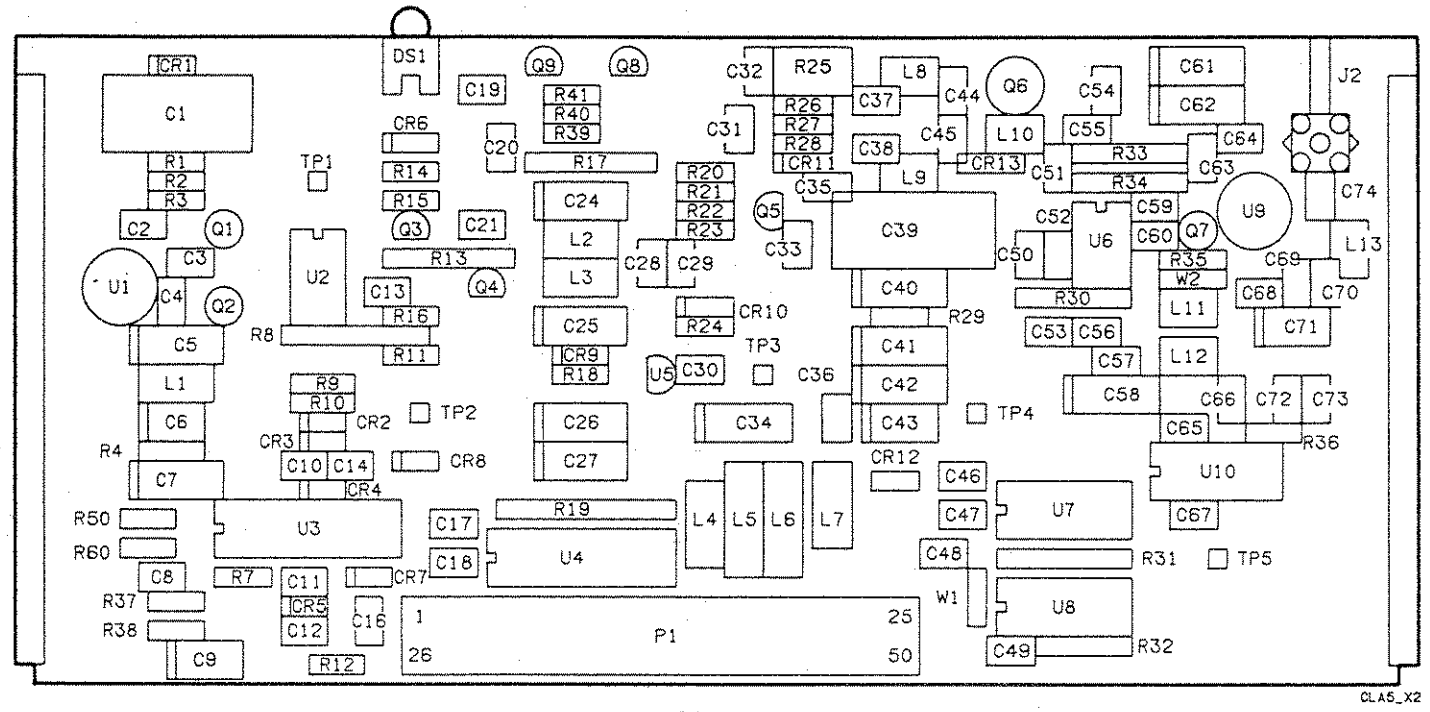


Figure 5-21. A4 Microprocessor Assembly (5361A) Component Locator/Schematic Diagram

A5 SYNTHESIZER ASSEMBLY 05350-60018

+5VD
R32 150Ω
NC
L_TEST_1
L_TEST_2
L_TEST_3
L_TEST_4
R31E 470
R31G 470
R31D 470
R31B 470
R31A 470
R31C 470
CTRDIV10 U7
C1 C2 RESET
S1 S2 S3 S0 [1] [2] [4] [5] Q1 Q2 Q3 Q0
VEE GND GND
MC10138
C46 1n
C47 0.01
C18 0.01
10 MHz ÷ R(100 KHz)
MODULUS CONTROL
LØ ÷ 5Ø
C65 100p
C67 1n
VCC1 VCC2 TTL VCC
E1 E2 E5 E4 E3
DIV 10/11 Q
U10
CL VBB TTL OUT VEE
MC12013
(+3.7V)
C72 0.01
C73 100p
R36 56.2
R31F 470
C66 100p
L7A 2
L7B 2
C43 3.3
C36 1n
C41 33
+5V
+5VA
+15V
L6 25Ø
C42 33
ROM A8
P1(19) P1(44) P1(18) P1(43) P1(16) P1(41)
R37 2150
R38 2000
R19 22K
SYN LATCH
SYN DATA Ø
SYN DATA 1
SYN DATA 2
SYN DATA 3
SYN DATA 4
SYN DATA 5
SYN DATA 6
SYN DATA 7
P1(12) P1(37) P1(4) P1(29) P1(5) P1(30) P1(6) P1(31) P1(7) P1(32) P1(8) P1(33) P1(9) P1(34) P1(10) P1(35) P1(11) P1(36)
U4 EN C1 1D
74LS573N
U3 D0 D1 D2 D3 A0 A1 A2 ST VDD VSS
C11 0.01
C9 3.3
C14 100p
(H=+5Ø)(L=+5Ø)
CR2 CR4 CR3
R16 215K
R8C 22K
CR8
C13 1n
R10 1330
R9 750
C10 0.1
R11 3160
U2B LM393N
NOT PHASELOCKED
DS1
R15 464
R13A 4700
Q3
CR12
R21 3160
R22 100K
R23 1330
Q5
C33 0.01
C16 0.01
CR5
10 MHZ INT SYN
P1(1) P1(27)
fR fIN MC LD OSC IN PD OSC OUT fV R V
MC145146
NC
GND, MTHRPLN
P1(2) P1(76)
L5 25Ø
-5.2V
C34 33
C17 0.01
CR7
R7 2150
R6 2150
C8 1n
film C1 27n
R39 14.7K
Q1
Q8
R40 10K
Q9
R41 100K
R17B 10K
R17A 10K
-20V
L8 1.2
C37 10p
C44 100p
Q6
C45 18p
SEE NOTE 5
2n
L10 39n
C51 100p
4n
L9 1.2
CR13
C39 0.1 film
C35 1n
C38 100p
R27 215
C28 1n
C29 270p
L2 1m
L3 1m
R33A 100
R34A 100
(10.2V, ±0.5V)
(-11.0V, ±0.5V)
R26 100K
R28 10K
R17D 10K
C24 6.8
C31 0.01
C32 100p
C61 6.8
C54 0.01
C55 100p
CR11
R20 681Ø
L4 1m
-24V
C27 4.7
CR9
-20V(±1V)
TP1 TP2 TP3 TP4
GND
P1(3) P1(28) P1(13) P1(38) P1(17) P1(42) P1(20) P1(45) P1(23) P1(48)
R18 46.4K
+5VA
R13B 4700
Q4
(-18.8 ±1V)
C25 6.8
CR10
R13D 4700
R24 316
-20V(±1V)
ADJ. IN OUT U5
LM337
C30 0.01
C26 6.8
R8B 22K
R5 215K
R4 3160
(+2.35V)
R8A 22K
C6 3.3
(+2.65V)
U1 LF351
NC
C2 0.01
C3 1n
R1 10K
L1 1m
C4 0.01
C5 6.8
CR1
R3 14.7K
R14 100
R2 4640
Q2
C19 0.01
CR6
C20 100p
C7 33



CLA5_X2

NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN MICROFARADS;
   INDUCTANCE IN MICROHENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. PC TRACE INDUCTANCE.
6. TOLERANCE FOR ALL DC VOLTAGES ON SCHEMATIC IS ±0.1 VOLT UNLESS OTHERWISE NOTED.

REFERENCE DESIGNATORS

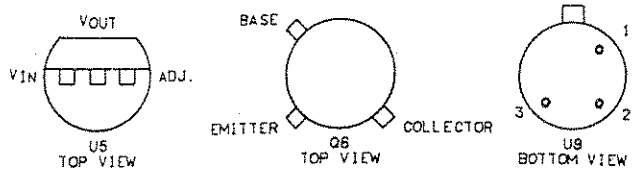
A5 ASSEMBLY	A5 ASSEMBLY
C1–C11, C13, C14, C16–C20, C24–C74	P1
CR1–CR13	Q3–Q7
DS1	R1–R11, R13–R38, R40–R41
J2	TP1–TP5
L1–L13	U1–U10
	W1, W2

TABLE OF ACTIVE ELEMENTS

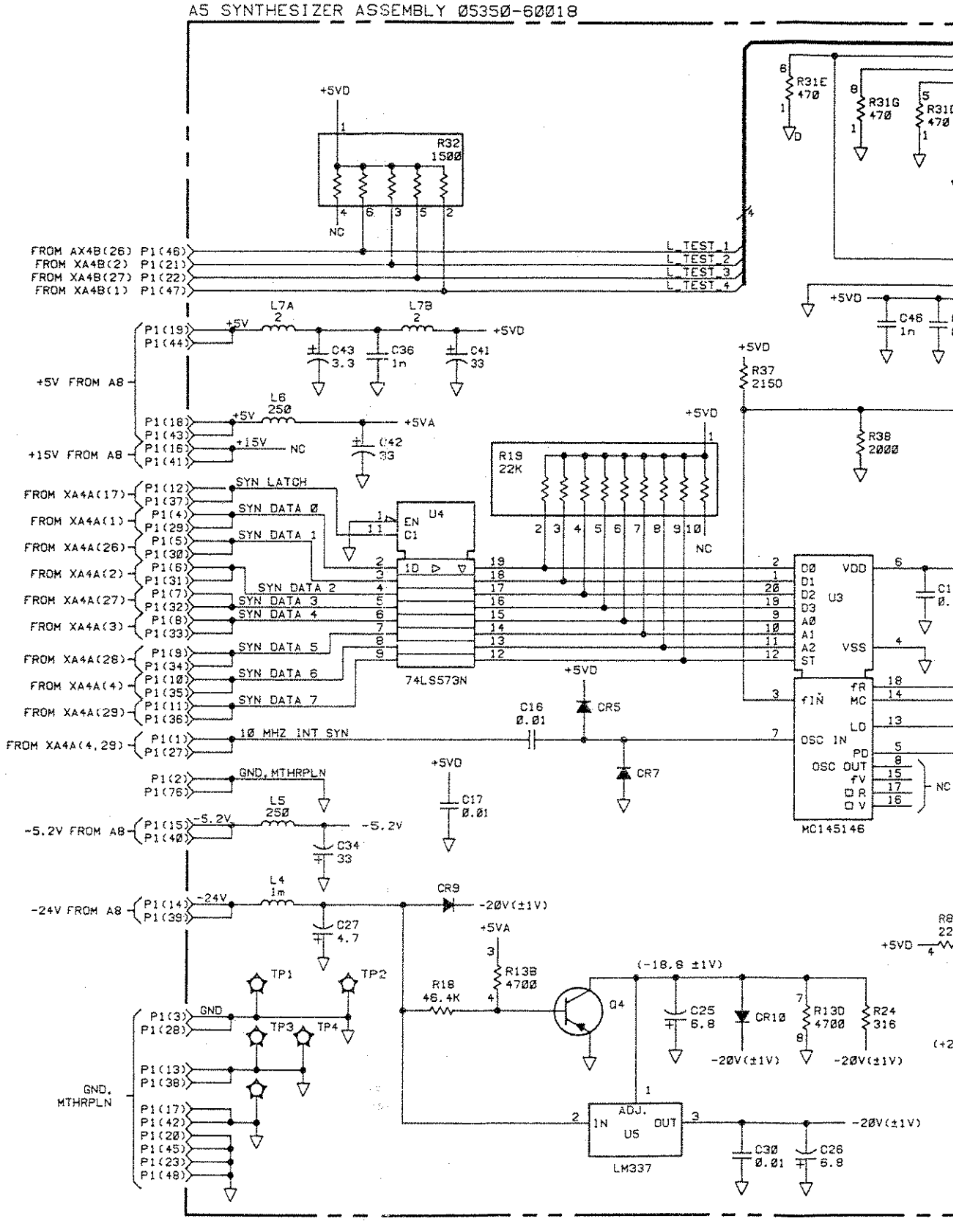
REFERENCE DESIGNATOR	HP PART NO.	MFG PART NO.
CR1–CR5, CR7–CR12	1901-0050	1N4150
CR6	1901-0734	1N5818
CR13	0122-0161	BB405B
DS1	1990-1022	HLMP-5030
Q3,Q8	1854-0215	2N3904
Q4, Q5	1853-0036	2N3906
Q6	1854-0591	BFR90
Q7	1854-0345	2N5179
U1	1826-0371	LF256N
U2	1826-0412	LM393N
U3	1820-3405	MC145146P
U4	1820-2724	2N74ALS573BN
U5	1826-1099	LM337LZ
U6	1826-0372	A251-0100
U7	1820-1383	MC10138L
U8	1820-3340	MC10H121P
U9	1813-0213	MWA130
U10	1820-1888	MC12013L

XA5
CONNECTOR PINOUT
CIRCUIT SIDE OF MOTHERBOARD

GND, MTHRPLN	26	1	10 MHz INT SYN
10 MHz INT SYN	27	2	GND, MTHRPLN
	28	3	GND, MTHRPLN
	29	4	SYN DATA 0
	30	5	SYN DATA 1
	31	6	SYN DATA 2
	32	7	SYN DATA 3
	33	8	SYN DATA 4
	34	9	SYN DATA 5
	35	10	SYN DATA 6
	36	11	SYN DATA 7
	37	12	SYN LCH
	38	13	GND, MTHRPLN
	39	14	-24V
	40	15	-5.2V
	41	16	+15V (NOT USED)
	42	17	GND, MTHRPLN
	43	18	+5V
	44	19	+5V
	45	20	GND, MTHRPLN
L TEST 1	46	21	L TEST 2
L TEST 4	47	22	L TEST 3
	48	23	GND, MTHRPLN
AUX B	49	24	AUX A
AUX B	50	25	AUX B



A5 SYNTHESIZER ASSEMBLY 05350-60018



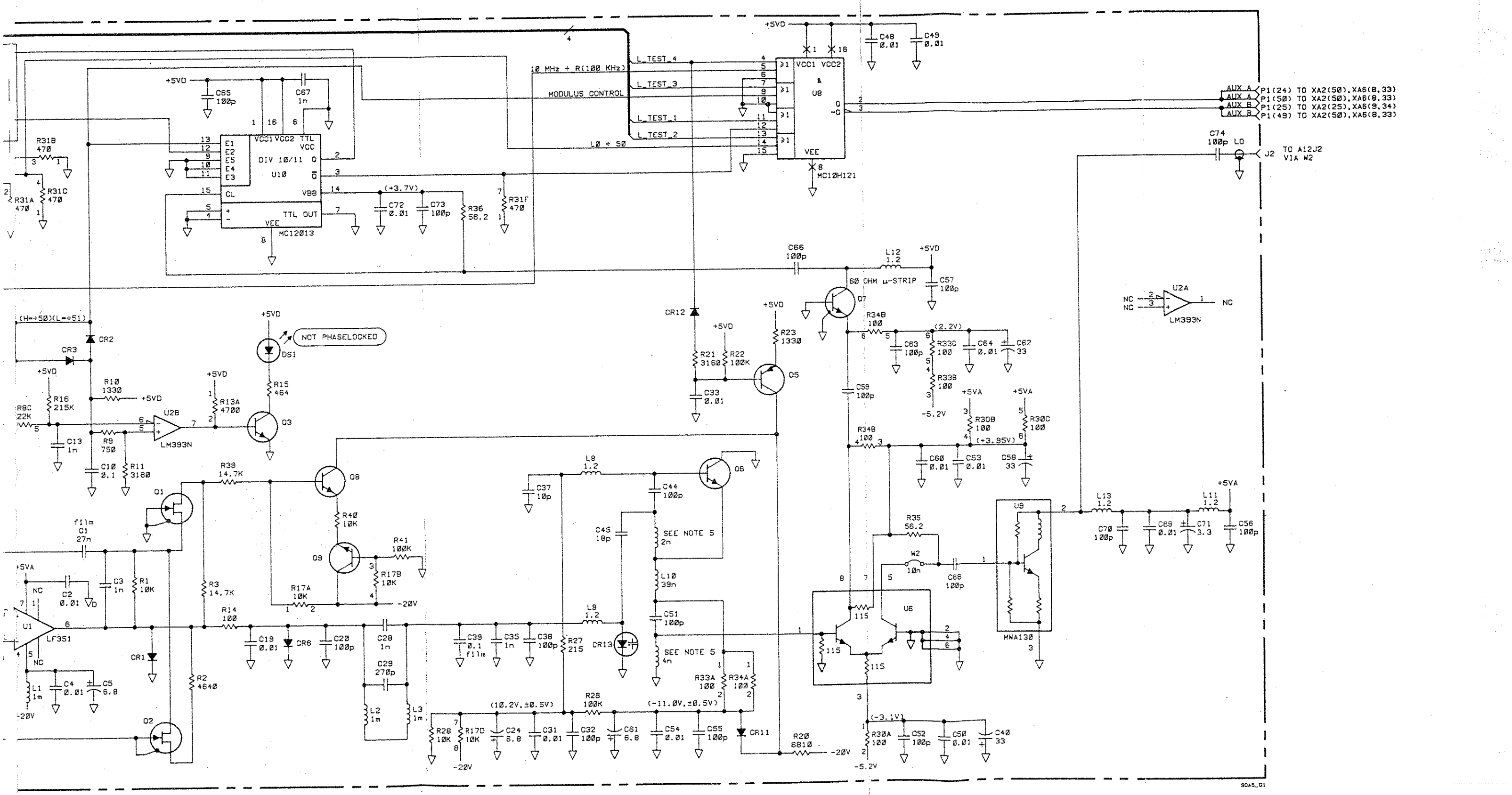


Figure 5-22. A5 Synthesizer Assembly Component Locator/Schematic Diagram

5

SERVICE

5-1. INTRODUCTION

This section contains the information needed to service the HP 5361B. Service information includes troubleshooting procedures, diagnostics, theory of operation, component locators, and schematic diagrams. The information contained in this section is organized as follows:

- Safety Considerations, Section 5-2: Describes the safety considerations applicable during maintenance, adjustments and repair.
- Recommended Test Equipment, Section 5-4: Refers to test equipment specified in *Table B-1* of Appendix B (Recommended Test Equipment).
- Repairs and After Service Checks, Sections 5-5 through 5-9: Describes Hewlett-Packard recommendations for preventing corrosion and electrostatic damages to printed-circuit boards and assemblies. After servicing safety checks are also described.
- Service Accessories, Section 5-10: Describes the function and use of extender boards available for testing printed-circuit boards, and provides a list of contents in an available Service Accessories Kit.
- Schematic Diagram Symbols and Reference Designations, Section 5-11: Describes the symbols used on the schematic diagrams and the reference designations used for parts, subassemblies and assemblies.
- Identification of Boards and Assemblies, Section 5-13: Describes the method used by Hewlett-Packard for identifying printed-circuit boards and assemblies, and lists all HP 5361B assemblies and their part numbers.
- Logic Symbols, Section 5-17: References to ANSI/IEEE standards.
- **Troubleshooting**, Sections 5-18 through 5-42: Provides troubleshooting information and procedures, diagnostics information, signal tracing techniques that are designed to isolate trouble to the assembly and then to the component group level.

- Disassembly and Reassembly, Section 5-43: Describes procedures for removal of covers and assemblies to gain access to parts.

- Theory of Operation, Section 5-49: Provides a block diagram description of the overall instrument operation.

- **Description of User-Callable Diagnostics**, Section 5-66: Lists and describes all of the built-in diagnostics which can be used to verify various functional subsections of the HP 5361B circuitry.

- Detailed Circuit Descriptions, Section 5-133: Provides detailed description of the circuits of each assembly.

- **Schematic Diagrams**, Section 5-146: Provides front and rear panel views, top and bottom internal views, an overall block diagram, and a schematic diagram for each of the circuit-board assemblies in the HP 5361B. Each schematic diagram includes a component locator for each field-repairable assembly. Where applicable, test and troubleshooting waveforms are placed adjacent to the schematic diagram.

5-2. SAFETY CONSIDERATIONS

Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition. Service instructions, and adjustment procedures requiring removal of the instrument top or bottom covers, are for use by service-trained personnel only. To avoid dangerous electric shock, do not perform any servicing or make any adjustments with the covers removed, unless qualified to do so.

WARNING

THE AC POWER CIRCUITS TO TRANSFORMER T1, UNREGULATED DC VOLTAGES ON THE MOTHERBOARD, AND REGULATED DC VOLTAGES FROM THE POWER SUPPLY CIRCUITRY TO THE MICROPROCESSOR BOARD AND THE OSCILLATOR ARE ALWAYS ON WHEN AC POWER IS CONNECTED TO THE INSTRUMENT, EVEN WHEN THE POWER SWITCH IS SET TO STANDBY. CONTACT WITH THESE CIRCUITS CAN RESULT IN PERSONAL INJURY OR DAMAGE TO EQUIPMENT.

WARNING

BEFORE APPLYING AC POWER, THE INSTRUMENT AND ALL PROTECTIVE EARTH TERMINALS, EXTENSION CORDS, AUTOTRANSFORMERS, AND DEVICES CONNECTED TO THE INSTRUMENT SHOULD BE CONNECTED TO A PROTECTIVE EARTH GROUNDED SOCKET.

ANY INTERRUPTION OF THE PROTECTIVE GROUNDING CONDUCTOR INSIDE OR OUTSIDE THE INSTRUMENT OR DISCONNECTION OF THE PROTECTIVE EARTH TERMINAL WILL CAUSE A POTENTIAL SHOCK HAZARD THAT COULD RESULT IN PERSONAL INJURY. INTENTIONAL INTERRUPTION IS PROHIBITED.

Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, if necessary, should be carried out only by a skilled person who is aware of the hazards involved. Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

Make sure that only fuses with the required current and voltage ratings, and of the specified type (normal blow, time delay, etc.), are used for replacement. DO NOT USE short-circuited fuseholders or repaired fuses.

5-3. Safety Symbols

The safety symbols used on equipment and the manual are shown on the Safety Considerations page at the front of this manual.

5-4. RECOMMENDED TEST EQUIPMENT

Test equipment recommended for testing and troubleshooting the HP 5361B is listed in *Table B-1* of Appendix B (Recommended Test Equipment). Substitute equipment may be used if it meets or exceeds the required characteristics listed in the table.

5-5. REPAIRS AND AFTER SERVICE CHECKS

5-6. Cleaning Printed-Circuit Boards

After soldering a component to a printed-circuit (PC) board, HP recommends that you DO NOT remove the flux from the soldered area. It has been found that after a hand soldering operation, the solder flux from RMA-P2 (Rosin, Mildly Active) solder does no harm if left in place on a PC board; the flux residue is inert and nonconductive. However, when the flux is dissolved with a chemical, in an attempt to remove it from the board, it spreads over the board, releasing several activators (chlorides, bromides, etc.). Now, instead of having a harmless flux residue with the water soluble activators trapped inside, you have a potential corrosion problem. If the instrument is stored in a humid environment, over time moisture will be absorbed which can start the corrosion process.

5-7. Repair of Multilayer Circuit Boards

Multilayer circuit boards can be damaged if excessive heat or force is used when removing or replacing parts. Static-free vacuum devices that pull the molten solder out of the circuit board holes are required. With the solder removed, parts should be easy to remove without excessive prying or pulling on components.

5-8. Electrostatic Discharge

Electronic components and assemblies in the HP 5361B can be permanently degraded or damaged by electrostatic discharge. Use the following precautions when servicing the instrument:

- **ENSURE that static sensitive devices or assemblies are serviced at static safe work stations providing proper grounding for service personnel.**
- **ENSURE that static sensitive devices or assemblies are stored in static shielding bags or containers.**
- **DO NOT wear clothing subject to static charge buildup, such as wool or synthetic materials.**
- **DO NOT handle components or assemblies in carpeted areas.**
- **DO NOT remove an assembly or component from its static shielding protection until you are ready to install it.**
- **AVOID touching component leads. (Handle by the packaging only.)**

5-9. After Service Product Safety Checks

The following safety checks must be performed after any troubleshooting and repair procedures have been completed to ensure the safe operation of the instrument.

WARNING

RESISTANCE CHECKS DESCRIBED BELOW REQUIRE THAT THE POWER CORD BE CONNECTED TO THE INSTRUMENT AND THAT AC POWER BE DISCONNECTED. BE SURE THAT THE POWER CORD IS NOT CONNECTED TO POWER BEFORE PERFORMING ANY SAFETY CHECKS.

1. VISUAL INSPECTION. Visually inspect the interior of the instrument for any signs of abnormal internally generated heat, such as discolored printed-circuit boards or components, damaged insulation, or evidence of arcing. Determine and remedy the cause of any such condition.

2. GROUND CONTINUITY TEST. Plug the power cord into the rear panel power module. (DO NOT connect the instrument to ac power.) Using a suitable ohmmeter, check resistance from the instrument enclosure (chassis) to the ground pin on the power cord plug. The reading must be less than 1Ω. Flex the power cord while making this measurement to determine whether intermittent discontinuities exist.

3. Check any indicated front or rear panel ground terminals marked, using the above procedure.

4. INSULATION RESISTANCE TEST. Tie the line and neutral pins of the power cord plug together. Measure the resistance from the instrument enclosure (chassis) to the line and neutral pins of the power cord plug. The minimum acceptable resistance is 2MΩ. Replace any component which results in a failure.

5. POWER MODULE CHECK. Check the line fuse and voltage selector card in the rear panel power module to verify that the correctly rated fuse is installed and that the instrument is properly set for the ac power source to be applied.

5-10. SERVICE ACCESSORIES

Service accessories to aid in troubleshooting the HP 5361B are available from Hewlett-Packard. *Table 5-1* lists the items in HP 5361B Service Accessory Kit. The list includes the name, the HP part number, and a brief description of each item use.

Table 5-1. Service Accessories Kit (05361-67001) Contents

ACCESSORY	HP PART NUMBER	DESCRIPTION AND USE
Extender Boards (2 each)	5060-0175	50-pin dual connector extender board used for A1, A2, A3, A4, A5, and A6 assemblies.
Extender Board	05361-60050	60-pin dual connector extender board for A14 Assembly (05361-60009). **NOTE: the A14 Assembly plugs into the XA9 connector of the Motherboard.**
Extender Cable	05350-60102	SMB (male) to SMB (female) identical to W2 cable in the instrument, but is not attached to a metal RF shielding cover. Allows connection of A5 Synthesizer Assembly output (W2) to Microwave Module when A5 Assembly is mounted on an extender board, outside of RF shielding can.
IF Test Cable	05350-60121	90° SMB (female) to BNC (male). Allows viewing of the Microwave Module IF output (A12J1) with spectrum analyzer or oscilloscope.
LO Test Cable	05350-60120	90° SMB (male) to BNC (male). Allows viewing of LO output (W2) of A5 Synthesizer Assembly with a spectrum analyzer.
HP-IP Verification Floppy Discs	05361-13502 (5 1/4-inch) 05361-13501 (3 1/2-inch)	5 1/4-inch and 3 1/2-inch floppy discs with HP-IB Verification Tests written in BASIC.
Service Manual	05361-90003	This manual contains information that describes how to test and repair the HP 5361B.
Operating and Programming Manual	05361-90018	This manual contains information that describes how to operate and program the HP 5361B.

5-11. SCHEMATIC DIAGRAM SYMBOLS AND REFERENCE DESIGNATIONS

Figure 5-1 shows the various common symbols used on the schematic diagrams. At the bottom of *Figure 5-1*, the identification system for reference designations, assemblies, and subassemblies is shown.

5-12. Reference Designations

Reference designations are assigned to indicate the class and the location of printed-circuit assemblies (boards), subassemblies (if any), and all of the component parts, as shown in the example in *Figure 5-1*. Assemblies are assigned numbers in sequence, A1, A2, etc. Component parts are numbered in sequence, from left to right, top to bottom, according to the physical location on the board.

Subassemblies within an assembly are given a subordinate A number. For example (see *Figure 5-1*), rectifier subassembly A1 has the complete designation of A25A1. For individual components, the complete designation is determined by adding the assembly number and subassembly number, if any. For example, CR1 on the rectifier assembly would have a complete reference designation of A25A1CR1.

5-13. IDENTIFICATION OF BOARDS AND ASSEMBLIES

5-14. Identification Markings On Printed-Circuit Boards

Printed-circuit boards in this instrument (see *Figure 5-1*) have three identification numbers: an assembly part number, a revision letter, and a production code. The assembly part number has 10 digits (such as 05350-60002) and is the primary identification. All assemblies with the same part number are interchangeable. When a production change is made on an assembly that makes it incompatible with previous assemblies, the part number is changed.

Revision letters (A,B, etc.) denote changes in printed-circuit layout. For example, if a capacitor type is changed (electrical value may remain the same) and requires different spacing for its leads, the printed-circuit layout is changed and the revision letter is incremented to the next letter. The production code is a four-digit seven-segment number used for production purposes.

5-15. Identification of Multilayer Circuit Boards

Multilayer circuit boards with conductors in three or more layers have a rectangular pattern of 4, 6, or 8 windows with single digits visible in the windows when the circuit boards are held over a light. The square windows appear on both sides of the circuit board. The number of identifiable numbers indicates the number of layers in the circuit board. For example, a circuit board having four windows with "1" in one window, "4" in a second window (on the opposite side), a "2" or "3" visible through the third window, and one blank window will have three layers.

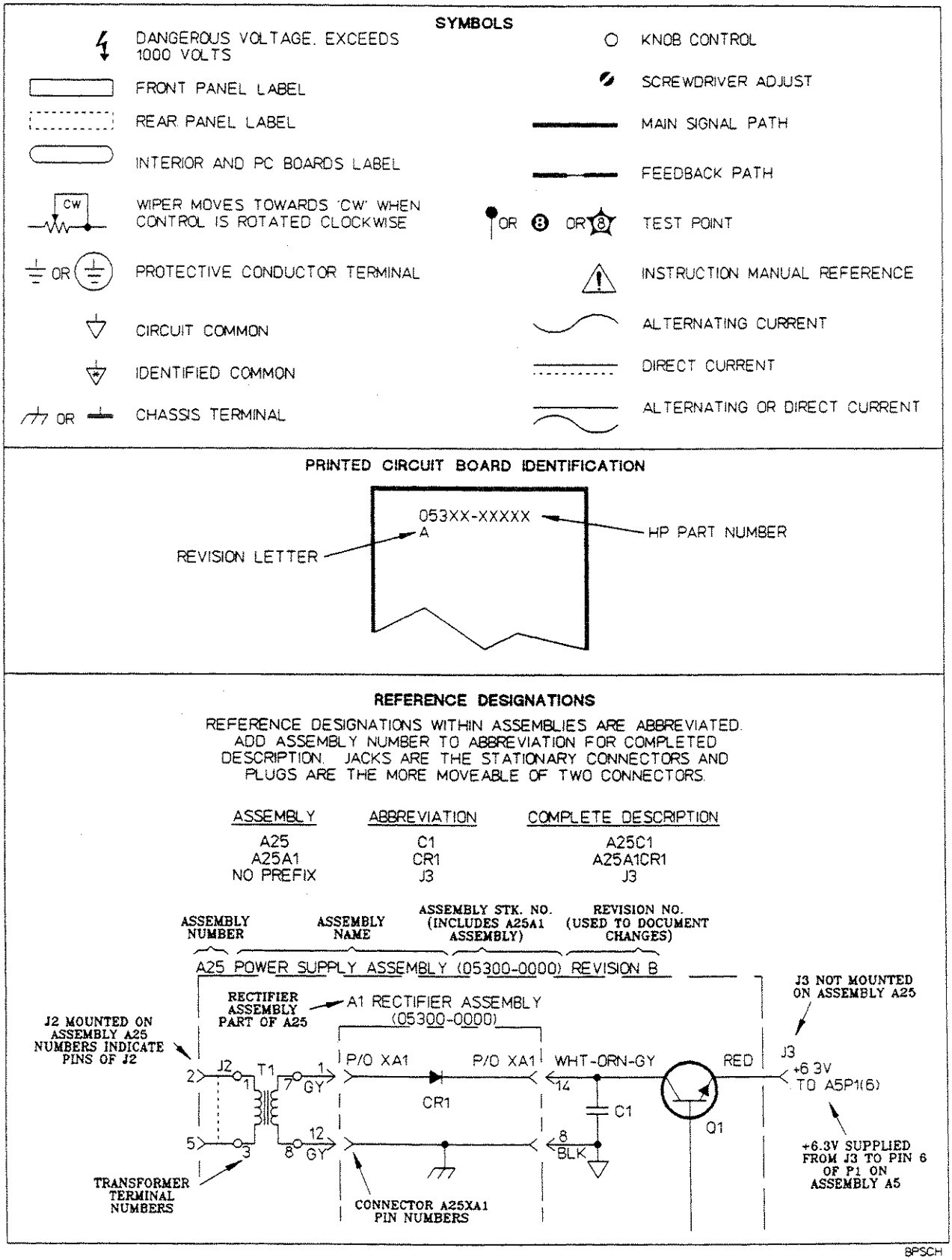


Figure 5-1. Schematic Diagram Notes

5-16. Assembly Identification and Location

The assembly number, name and Hewlett-Packard part number of HP 5361B assemblies are listed in *Table 5-2*. A top internal view of the instrument is shown in *Figure 5-14*.

Table 5-2. Assembly Identification and Location

ASSEMBLY	NAME	HP PART NO.
A1	Timebase Buffer/Power Supply Control	05361-60001
A2	Low Frequency Input	05350-60002
A3	Counter	05361-60003
A4	Microprocessor	05350-60023
A5	Synthesizer	05350-60018
A6	IF Amplifier/Detector	05361-60006
A7	Keyboard/Display Logic	05361-60007
A8	Motherboard	05361-60008
A9	Display/Driver	05350-60123
A10	Temperature Compensated Crystal Ocillator (TXCO) Timebase or Option 001 Oven Oschllator Timebase or Option 010 High Stability Oven Oscillator Timebase	0960-0602 10811-60111 10811-60211
A11	HP-IB Interface	05350-60011
A12	Microwave Module (A12 Assembly/U1 Sampler)	05361-60012
A13	Power Input Module and Transformer	0960-0443
A14	Gate Board	05361-60009

5-17. LOGIC SYMBOLS

Logic symbols used in this manual conform to the American National Standard publication *IEEE Standard Graphic Symbols for Logic Functions, ANSI/IEEE Std. 91-1984*. This standard supersedes MIL-STD-806B. Another useful reference source is the *The TTL Data Book*, "Explanation of New Logic Symbols" by F.A. Mann (Texas Instruments Incorporated).

5-18. TROUBLESHOOTING

The following paragraphs contain troubleshooting procedures for the HP 5361B. The procedures begin with overall troubleshooting procedures to isolate the problem to a specific board assembly, followed by procedures for each of the field-repairable assemblies in the HP 5361B. The troubleshooting procedures are listed in *Table 5-3*.

Table 5-3. Troubleshooting Procedures

TROUBLESHOOTING PROCEDURE	SECTION NUMBER
Overall Troubleshooting • Diagnostics • Inference Chart • Assembly Troubleshooting Techniques	5-19
Power Supply Block Troubleshooting (A8 Motherboard/Part of A1)	5-29
Timebase Buffer Block Troubleshooting (Part of A1)	5-32
A2 Low Frequency Input Assembly Troubleshooting	5-33
A3 Counter Assembly Troubleshooting	5-34
A4 Microprocessor Assembly Troubleshooting	5-35
A5 Synthesizer Assembly Troubleshooting	5-36
A6 IF Amplifier/Detector Assembly Troubleshooting	5-37
A7 Keyboard/Display Logic Assembly Troubleshooting	5-38
A9 Display/Driver Assembly Troubleshooting	5-39
A11 HP-IB Interface Assembly Troubleshooting	5-40
Microwave Module Troubleshooting (A12 Assembly/U1 Sampler)	5-41
A14 Gate Board Assembly Troubleshooting	5-42
Whenever repairs or adjustments are made, the instrument should be checked for proper performance. Refer to the adjustments in Section 2, and to the Operational Verification procedures and Performance Tests in Section 1.	

WARNING

TROUBLESHOOTING PROCEDURES REQUIRE INTERNAL ACCESS TO THE INSTRUMENT WITH THE PROTECTIVE COVERS REMOVED. THESE PROCEDURES MUST BE PERFORMED ONLY BY SERVICE-TRAINED PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED.

CAUTION

Electronic components and assemblies can be permanently degraded or damaged by electrostatic discharge. Use the following precautions:

ENSURE that static sensitive devices or assemblies are serviced at static safe work stations providing proper grounding for service personnel.

ENSURE that static sensitive devices or assemblies are stored in static shielding containers.

DO NOT wear clothing subject to static charge buildup, such as wool or synthetic materials.

DO NOT handle components or assemblies in carpeted areas.

DO NOT remove a replacement assembly from its static shielding container until you are ready to install it.

AVOID touching component leads. (Handle by the package only.)

5-19. OVERALL TROUBLESHOOTING

Before removing the top cover of the instrument, the front panel diagnostic routines should be used to identify the faulty assembly. Once a particular assembly has been identified, exercising all of the diagnostic tests relating to it may help determine the specific portion of circuitry that is at fault.

5-20. General Diagnostics and Extended Functions Information

There are 59 diagnostics/extended functions with identifying numbers from 0 to 99. All of the diagnostics and extended functions are listed in *Table 5-12*, by order of the diagnostic/extended function number. The difference between the diagnostics and extended functions is described in the following paragraph.

The diagnostics are tests that allow you to verify operation of specific assemblies in the HP 5361B; hence, diagnostics help you to troubleshoot and repair the HP 5361B. Extended functions are parameter changers that allow you to customize and/or measure a specific measurement factor such as gate width or local oscillator (LO) frequency for either an INPUT 1 or INPUT 2 measurement. All diagnostics and extended functions for the HP 5361B are described in detail starting at Section 5-66.

In some cases, a combination of both the diagnostics and extended functions must be used to enable troubleshooting.

NOTE

The terms "diagnostic" and "extended function" are the same when used for troubleshooting purposes; thus, the term diagnostics, which is more appropriate for troubleshooting, is used throughout this service section when feasible.

The diagnostics in the HP 5361B have been designed using the kernel technique (that is, the diagnostic test relies on not more than one untested assembly to perform the test). Therefore, it is important to know the status of all the assemblies involved in a particular test in order to confirm a diagnosis. The arrangement of the Self Check tests, and the Inference Chart shown in *Figure 5-2* facilitate this.

There are three types of diagnostics:

1. Power-Up Self Test: A sequence of tests **automatically executed** on power-up. These tests include subsets of the user-callable diagnostics. (Refer to Section 5-27.)

2. User-Callable Diagnostics: Individual tests which can be initiated manually or via the HP-IB. (Refer to Section 5-66.)

3. Self Check: A sequence of tests executed by pressing the **Self Check/Cal** key. The Self Check tests are a subset of the user-callable diagnostics. (Refer to Section 5-28.)

The user-callable diagnostics that are primarily used for for testing, troubleshooting, and repairing are listed in *Table 5-4*, by order of the assembly number tested.

The Power-Up Self Test, Self Check, and Diagnostic (DIAG) routines execute individual tests in a sequence that verifies assemblies in a critical order. For example, the tests first verify that the timebase is functional before attempting to verify that the low frequency circuitry can count the timebase signal.

Table 5-4. User-Callable Diagnostic Functions Used for Troubleshooting

ASSEMBLY TESTED	NAME	DIAG OR EFUN NO.
A1/(P/O A8) A8/(P/O A1)	Timebase Verification Power Supply Verification	10 11
A2	Low Frequency 50 Ω Verification Low Frequency 1 MΩ Verification	20 21
A3	Display Interpolator Short Calibration Display Interpolator Long Calibration Display Interpolator Measurement MRC Channel A Verification: 10 MHz Timebase MRC Channel B Verification: 35 MHz Interpolator Check	07 08 09 30 31 32
A4	Firmware Revision Code RAM Test ROM Test Repeated Reset	40 41 42 43
A5	LO Synthesizer Verification: 29.5 MHz and 35 MHz LO Synthesizer Verification: User-Entered Frequency LO Synthesizer Sweep LO Synthesizer Lower and Upper Frequency Bounds	50 51 52 53
A6	IF Verification: 35 MHz; Disable Input 1 and IF IF Verification: 35 MHz; Disable Input 1	60 65
A7	Keyboard Test Display Test	70 71
A11	HP-IB Test	80
A14	Display Gate Bias Error Gate Bias Calibration	34 54

5-21. Diagnostics Inference Chart

Once a particular assembly has been identified as failing a diagnostic or self test routine, the operater should refer to the Diagnostics Inference Chart, *Figure 5-2*, to determine further checks to perform. The "flow" of the Inference Chart is from left to right. In order to verify a particular assembly, all assemblies in the direct path to the left of the suspect assembly should be verified. For example, if executing a Self Check resulted in displaying an A6 assembly failure (DIAG 60, 61, 62, 63, 64, or 65 failure), the next step would be to verify the A4, A1, A3, and A5 assemblies, using the associated diagnostics. In addition, for any A14 failures (DIAG or EF 34 and 54), the next step is to verify the A4, A11, A3, and A6 assemblies using the associated diagnostics.

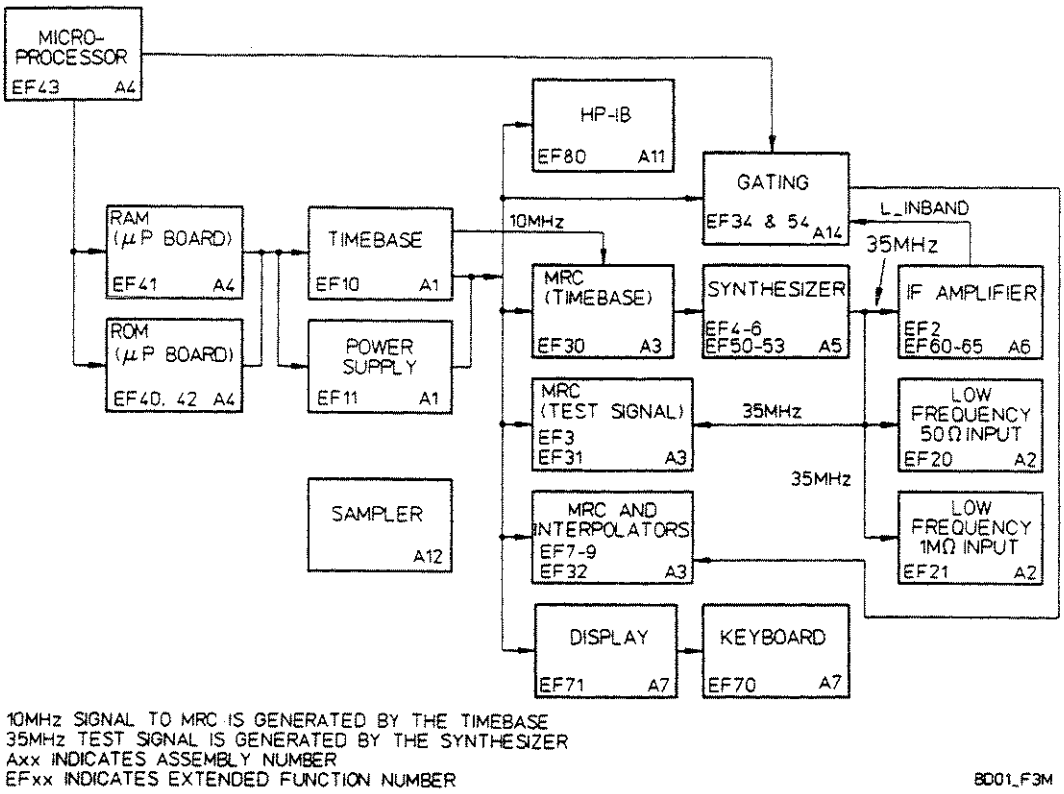


Figure 5-2. Diagnostics Inference Chart

It is important to understand that the diagnostic routines are not foolproof. In some cases, it is not feasible to test 100% of a given circuit. These cases are pointed out in the appropriate troubleshooting procedure. It is also possible that the circuitry employed to test the board may cause a diagnostic test failure, even though the HP 5361B continues to make correct measurements. The possibility of test circuit failure has been minimized, but it is possible for this type of failure to occur. The only assembly which is not tested in some form by the diagnostics is the Microwave Module (A12 Microwave Assembly/U1 Sampler).

Refer to Section 5-66 for detailed information on every diagnostic.

5-22. Assembly Troubleshooting Techniques

In most cases, signal measurements can be made with a high impedance oscilloscope probe. It is important to minimize capacitance loading effects by using the appropriate probe. (Refer to *Table B-1*, Recommended Test Equipment, in Appendix B). In addition, it is crucial that minimal ground lead lengths be used. Following these precautions will aid in achieving oscilloscope displays which match the waveform illustrations shown in this manual.

In many cases, dc bias voltages are noted in the troubleshooting procedures or on the schematics. These voltages will vary due to typical variations from component to component. However, it is helpful to verify that an active component is appropriately biased to determine if it is faulty. Generally look for relatively large deviations from these dc values to indicate a potential fault.

The troubleshooting procedures for each assembly are arranged in the following order:

1. Possible symptoms which may appear if the assembly is faulty.
2. A list of diagnostic tests that pertain directly to the assembly.
3. Points to consider when troubleshooting the assembly.
4. Power supply voltages to verify on the assembly.
5. Inputs to the assembly to be verified.
6. Outputs from the assembly to be verified.
7. A general approach to verifying the assembly operation.

In the following troubleshooting procedures, reference is often made to physical locations of components (for example, the right leg of a resistor, the bottom leg of an inductor, etc.). Additionally, reference will be given in terms of actual circuit location; that is, the base of Q1, junction of R1 and C12, etc. All physical locations discussed in procedures and in tables are referenced looking toward the component side of the board, with the board oriented in its normal plugged-in position in the instrument (that is, the board is in its upright position with the instrument's front panel facing the operator). It is assumed that the board in question, where applicable, is mounted on an extender board (HP P/N 5060-0175 or 05361-60050, as applicable). (See *Table 5-1.*)

While diagnostics may be individually called from the front panel, they are best used in particular combinations and sequences to obtain the maximum amount of testing and troubleshooting information. Detailed descriptions of the user-callable diagnostics begin in Section 5-66. For information on using the user-callable diagnostics, refer to Sections 5-23 through 5-28 and the troubleshooting procedures in this section (Section 5).

5-23. Diagnostics Mode Entry (Not for HP-IB Only Diagnostics)

The diagnostics mode may be entered by pressing the front panel **Extended Function** key once. After the key is pressed, the HP 5361B will carry out the current diagnostic routine. The current diagnostic is the last one called by the user, or if the HP 5361B has just been turned on, Diagnostic 1 (Self Test – Front Panel only).

The diagnostic mode may also be entered by using the parameter entry mode, which allows you to change the diagnostic number. A new diagnostic number (from 1 to 99) may be entered using the following key sequence:

Set/Enter,
Extended Function,
digit(s) (Function/Data keys),
Set/Enter

For example, to enter the diagnostic mode and set Diagnostic 32 (Interpolator Check, A3 Counter Assembly), prsss the following key sequence:

Set/Enter
Extended Function
3
2
Set/Enter

The HP 5361B display contents will depend on the diagnostic in progress. Most of the diagnostic displays will show "FUNC XX" or "F XX" in the message portion on the right-hand side of the display (where XX represents a diagnostic number from 01 to 99). Most displays will also include the assembly number, preceded by the letter "A", just to the left of the diagnostic number. For example, the DIAG (or FUNC) 60 display will show "A6" just to the left of "F 60".

Once the diagnostic mode is entered, the diagnostic number may be changed by using the key sequence described above, or by pressing the **INC** (increment) or **DEC** (decrement) key to move through the list of diagnostics in numerical order (exceptions: DIAG 98 and 99 cannot be entered using **INC** or **DEC** keys; once entered, DIAG 70 cannot be exited using the **INC** or **DEC** keys). If the diagnostic mode is entered by pressing the **Extended Function** key without using the **Set/Enter** key sequence, the last test entered will be executed. When the HP 5361B is first powered on, the diagnostic mode defaults to the following settings: DIAG 1,OFF.

5-24. Diagnostics Mode Exit and Special Conditions

For most diagnostics, the diagnostics mode can be exited by pressing **Extended Function** key a second time, or by pressing the **Reset/Local** key. There are some exceptions, however, in which the **Extended Function** key cannot be used to exit the mode because the key is used for other functions during the test. In these cases, pressing the **Reset/Local** key will exit the mode. Note that if the **Reset/Local** key is pressed to clear an "OUT OF RANGE 3 ERROR" (resulting from the entry of an invalid HP-IB address or Manual Center Frequency value), the error will be cleared and the diagnostic number will be exited at the same time.

There are also a few diagnostics which have special conditions attached to their use; for example, some diagnostics are not accessible via HP-IB. *Table 5-5* lists these and other special conditions. Refer to Section 5-26 for more information on the diagnostics not available over the HP-IB.

Table 5-5. Special Diagnostic Conditions

DIAGNOSTIC	SPECIAL CONDITION
DIAG 1 - Self Test	Not accessible via HP-IB. (Refer to Section 5-26 for explanation.)
DIAG 41 -RAM Test	Not accessible via HP-IB. (Refer to Section 5-26 for explanation.)
DIAG 42 - ROM Test	Not accessible via HP-IB. (Refer to Section 5-26 for explanation.)
DIAG 43 - Repeated Reset	Not accessible via HP-IB. (Refer to Section 5-26 for explanation.)
DIAG 51 - LO Verification, User-Entered Frequency via HP-IB only.	a) **Set/Enter** key interpreted as "1"; Press **Reset/Local** key to exit. b) Parameter entry possible after enabling. Defaults to current LO frequency when enabled.
DIAG 61 - Check Level Detector	**Reset/Local** key exits, clears overload status flag; **Set/Enter** key exits, leaves overload status flag as is.
DIAG 70 - Keyboard Test	Pressing **Extended Function** key displays message, but will not exit; **Reset/Local** key must be pressed to exit. INC and DEC (arrow) keys can be used to enter, but not to exit.
DIAG 80 - HP-IB Verification	Not accessible via HP-IB. (Refer to Section 5-26 for explanation.)
DIAG 98 - Keyboard Lockout	Once enabled, counter automatically returns to measurement mode. Special key sequence is required to exit, all other keyboard entry is ignored. (Refer to Section 5-131.)
DIAG 99 - Display Lockout	Once enabled, counter automatically returns to measurement mode. Keyboard functions normally while display is disabled. Special key sequence is required to exit this mode. (Refer to Section 5-132.)

5-25. Invalid Diagnostic Numbers

If you attempt to enter an invalid diagnostic number via the HP-IB, the HP 5361B will display the message: "NOT AVAILABLE FUNC XX", where XX represents the invalid number. The only exception is if 00 is entered as the diagnostic number, in which case the HP 5361B will automatically default to DIAG 1. If the **INC** or **DEC** key is being used to move through the list of diagnostics, the HP 5361B will display the "NOT AVAILABLE" message until the next valid diagnostic in the sequence is reached.

5-26. Calling Diagnostics Over the HP-IB

Most of the user-callable diagnostics available from the front panel are also available over the HP-IB by using the "EFUN", "EFUNPARM", and "EFUN?" commands. Diagnostics are enabled over the HP-IB using the "EFUN" command. For example, the command "EFUN,32,ON" will cause the HP 5361B to cycle through the Interpolator Check until the command "EFUN,OFF" is sent. Diagnostic results can be obtained over the HP-IB by using the EFUN? command. The EFUNPARM command is used only with EFUN 51 to allow you to enter a frequency parameter for local oscillator verification. Refer to Section 4 (Remote Operation via the HP-IB) in the Operating and Programming Manual for detailed information on use of the HP-IB. **Five diagnostics are not available over the HP-IB, because they may erase needed memory or reset hardware. The diagnostics not available are:**

DIAG 1: Self Test
DIAG 41: RAM Test
DIAG 42: ROM Test
DIAG 43: Repeated Reset
DIAG 80: HP-IB Verification

5-27. Power-Up Self Test

When the HP 5361B is powered up, an automatic internal check (an expanded version of DIAG 43 Repeated Reset) is made of several major components, including the microprocessors and related circuitry. During this cycle, all front panel display segments and annunciators will light for about 3 seconds, after which the current HP-IB address will be displayed for about 15 seconds. On successful completion of all tests, the normal measurement display will appear.

The failure messages for the Power-Up test will depend on which diagnostic fails (similar to DIAG 43). Refer to the descriptions of the individual diagnostics for examples of the possible failure messages resulting from a Power-Up test failure (refer to Section 5-66).

If any test fails during the Power-Up sequence, the failure message will remain until the user presses the **Reset/Local** key. At that point, the next test is executed (if possible). By pressing the **Reset/Local** key, most failures can be bypassed to allow the HP 5361B to proceed with the Power-Up test sequence. When the last test is complete, the HP 5361B will proceed to the normal operation mode, if possible. Refer to troubleshooting procedures in this section if a failure message appears during the Power-Up sequence.

During the power-up cycle, the HP 5361B performs the following test sequence:

1. Turns on all Display segments and annunciators.

2. DIAG 41 – RAM Test.

3. Initializes input/output ports.

4. Initializes RAM.
5. DIAG 42 – ROM Test.
6. DIAG 01 – Self Test:
   a. DIAG 11 – Power Supply Verification
   b. DIAG 10 – Timebase Verification
   c. DIAG 30 – MRC Channel A Verification: 10 MHz Timebase
   d. DIAG 50 – LO Verification: 29.5 MHz, 35.0 MHz
   e. DIAG 31 – MRC Channel B Verification: 35 MHz
   f. DIAG 60 – IF Verification: 35 MHz; Disable INPUT 1 and IF
   g. DIAG 32 – Interpolator Check
   h. DIAG 20 – Low Frequency 50Ω Verification: 35 MHz
   i. DIAG 21 – Low Frequency 1MΩ Verification: 35 MHz
   j. DIAG 54 – Gate Bias Calibration
7. DIAG 80 – HP-IB Verification, and display address or a message indicating that HP-IB is not installed.
8. Sets instrument status and annunciators to default conditions: Counter mode measuring from INPUT 1.
9. Checks for external reference, overload: update annunciators.
10. Tests for HOLD mode: if so, display "HOLDING—" message.
11. Tests for lockouts in effect: if so, display lockout message.
12. Sets current diagnostic number to 1.
13. Begins measurement.

In addition to failure messages, the HP 5361B may display "HP-IB NOT INSTALLED" if the ribbon cable from the A11 HP-IB Interface Assembly to the A8 Motherboard Assembly is not properly connected.

When performing the Self Test over the HP-IB using the "TEST?" command, only the first failure result will be returned over the bus, then the HP 5361B will exit the Self Test routine.

5-28. Self Check/Cal

When the **Self Check/Cal** key is pressed, a particular sequence of diagnostics (a subset of the user-callable diagnostics) is executed to test the measurement circuitry of the HP 5361B. This diagnostic performs the same sequence of tests as DIAG 1 (Self Test), but will only perform the test sequence once, and will show a different set of display messages.

The Self Check diagnostic routines are arranged so that each routine involves only one untested assembly. The Self Check routines and the order in which they occur are shown in *Table 5-6*.

Table 5-6. DIAG 1 Self Test Sequence

DIAG NUMBER	TEST	ASSEMBLY TESTED
DIAG 11	Power Supply Verification	A1/A8
DIAG 10	Timebase Verification	A1
DIAG 30	MRC CH A Verification: 10 MHz Timebase	A3
DIAG 50	LO Verification: 29.5 MHz, 35.0 MHz	A5
DIAG 31	MRB CH B Verification: 35 MHz	A3
DIAG 60	IF Verification: 35 MHz, Disable INPUT 1 and IF	A6
DIAG 32	Interpolatpor Check	A3
DIAG 20	Low Frequency 50Ω Verification: 35 MHz	A2
DIAG 21	Low Frequency 1MΩ Verification: 35 MHz	A2
DIAG 54	Gate Bias Calibration	A14

If the instrument passes Self Check, it will display the "pass" messages (listed below) for approximately 3 seconds then return to its previous measurement mode. The following pass messages are displayed:

PASS 35 000 0xx SELF
PASS 35 000 0 LVL SC**

If the instrument fails Self Check, it will display one of two "fail" message formats. If instrument fails DIAG 11, 10, of 32, the following fail messages are displayed:

FAIL POWER A1 SELF
FAIL TIMEBASE A1 SELF
FAIL INTERPOL A3 SELF

If any of the other Self Check tests fail, the message format is as follows:

FAIL xx xxx xxx Ay SELF

where x's are random numbers, and y is the number of the assembly involved in the failure.

If the Self Check passes, the instrument automatically returns to its previous measurement mode. If a Self Check failure occurs, the fail message will remain on the display, and the instrument will wait for the **Reset/Local** key to be pressed. Pressing the **Reset/Local** key causes the instrument to proceed to the next test in sequence, which will be performed, if possible. In this way, the user can scroll through all of the diagnostics in the Self Check sequence, even though one or more of the tests may be failing.

When performing the Self Check over the HP-IB using the "TEST?" command, only the first failure result will be returned over the bus, after which the instrument exits the Self Check routine.

5-29. POWER SUPPLY BLOCK TROUBLESHOOTING (A8 AND PART OF A1)

WARNING

IF THE W8 RIBBON CABLE FROM THE A7 KEYBOARD/DISPLAY LOGIC ASSEMBLY TO THE A8 MOTHERBOARD/POWER SUPPLY REGULATOR ASSEMBLY IS DISCONNECTED, THE POWER SUPPLY CIRCUITS WILL ALWAYS BE ON WHEN THE INSTRUMENT IS CONNECTED TO AC POWER.

5-30. Fuse Replacement

There are four fuses in the HP 5361B. One fuse (line fuse, F1) is located on the rear panel in the Line Power Module (A13). Two fuses (A8F1, A8F2) are located on the A8 Motherboard Assembly. The remaining fuse (J2F1) is located in the front panel BNC connector for INPUT 2.

The primary or main line fuse (F1) protects the instrument from excessive current. To replace the line fuse (F1), perform the following (see *Figure B-1* of Appendix B in the Operating and Programming Manual):

1. Remove the ac power cord from the rear panel.
2. Slide the clear plastic cover over the ac power cord male connector, exposing the fuse.
3. Pull on the tab labeled "FUSE PULL" to pry the blown fuse out of the holder.
4. Remove the blown fuse and push the FUSE PULL tab to its original position.
5. Insert the replacement fuse in the holder and slide the plastic cover over the fuse.

A8F1 protects the fan. An open A8F1 can be detected by failure of the fan to operate during normal operation. A8F2 protects the +15V secondary. An open A8F2 can be detected by checking the +15V test point at the Power Supply Test Connector (A8J7). Replacement of these fuses requires desoldering the blown fuse and soldering in the replacement.

The J2F1 fuse protects the low frequency port, INPUT 2. Refer to the OPERATOR'S MAINTENANCE section of Appendix B in the Operating and Programming Manual for replacement instructions for this fuse.

Part numbers for replacement fuses can be found in *Table 3-3*, Replaceable Parts.

5-31. Failure Symptoms

The two most probable power supply failure symptoms are as follows:

- An open AC Line fuse (F1) in the rear panel Line Power Module.
- Incorrect voltage level for a particular power supply voltage, indicated by a Diagnostic 11 (A1 Power Supply Verification) failure message during power-up.

When verifying power supply voltages in the HP 5361B, it is recommended that as many measurements as possible be made at the Power Supply Test Connector (A8J7) located on the motherboard. The test pin circuitry is designed so that accidental shorting at these pins

will not damage the power supply circuit. In addition, provisions have been made to measure the current being supplied by the circuitry. The difference between voltages measured at the "V/X" test point and the corresponding "I/X" test point divided by the current sense resistor value found on the A8 schematic diagram will give the current supplied. Refer to *Table 5-8*, Power Supply Test Connector Voltages.

BLOWN REAR PANEL LINE FUSE. First verify the proper orientation of the line voltage selector card in the Line Power Module on the rear panel. Once this has been checked, plug the HP 5361B into a variable transformer and slowly increase the voltage, monitoring the current. Use the variable transformer to supply enough current to locate a short circuit, but not blow (or open) the main fuse. Typically this current should be about one-third of that of the ac line fuse current rating.

The transformer secondaries are connected to the instrument at A8J8 and A8J9 via cable W8. Disconnecting these connectors one at a time may help isolate which secondary is shorted. The transformer may be shorted or open internally (if it is open, the fuse will probably not be blown, but the HP 5361B will not power ON).

Incorrect voltages at the test connector may be caused by a transformer unable to supply sufficient current for the load. Apply power with a variable transformer to the instrument with the W8 cable connectors at both A8J8 and A8J9 disconnected, and verify that the current is nearly zero amperes. Check the output of the transformer secondary with an oscilloscope.

The unregulated voltages in the instrument and their ranges are shown in *Table 5-7*.

Table 5-7. Unregulated Voltages

TEST POINT (ON A8)	SIGNAL NAME	ALLOWABLE RANGE (normal line voltage applied)
C19(+)	+5V UNREG	+6 to +10 V
C18(–)	–5.2V UNREG	–6 to –10 V
C3(+)	+15V UNREG	+16 to +25 V
C4(–)	–24V UNREG	–27 to –45 V

Problems with these unregulated voltages could be caused by shorted diodes in the rectifiers or shorted capacitors C3, C19, C18, and C4. Also, the A1 Assembly uses these unregulated voltages. It may be helpful to remove the A1 Assembly to help isolate the source of the problem.

POWER SUPPLY OUT OF RANGE. The following procedures assume that the instrument is in a state where it can be connected to an ac power line and powered ON without blowing the rear panel fuse. Use the normal line voltage (not a variable transformer) for the following troubleshooting procedure.

The pass or fail indication of Diagnostic 11 (Power Supply Verification) is a quick check of the status of the power supplies without having to remove the cover of the instrument. In addition, once the cover has been removed, the red LED at the top of the A1 Assembly indicates the status of the power supply. The LED should be on when the HP 5361B is in the Standby (STBY) mode. When the HP 5361B is switched to ON, the LED should be off. If the LED stays on during normal operation, or is off in Standby mode, there is a fault in the power supply. The status circuit will detect problems in most cases, however, the Power Supply Test Connector voltages should be verified for a thorough check.

If the LED does not function as described above or Diagnostic 11 (Power Supply Verification) fails, probe the test connector to determine which supply is faulty. The current sense/voltage sense measurements (for example, I/+5 and V/+5, etc.) are useful to determine if the +5V, –5.2V, or +15V supplies are being current limited. Refer to *Table 5-8*.

Check the +5V reference at TP4 on A1 (+4.94V to +5.06V). Also check the +12V at TP5 on A1 (+11.2V to +12.8V). If either of these references is not correct, check the appropriate regulator (A1U1, A1U2). Both of these voltages must be operative for the A1 Power Supply Control circuit to function properly.

If the +5V, –5.2V, or +15V supply is faulty, check the regulator circuitry on the A1 Assembly as outlined below.

+5V REGULATOR. Note that this supply is different from the +5V μP Standby RAM supply and timebase supplies located on the timebase buffer portion of the A1 Assembly. The +5V μP Standby RAM supply is connected to the +5V supply via CR1 on the A8 Motherboard Assembly. The +5V supply will serve as a backup only if the +5V μP regulator fails (opens).Determine if another assembly is faulty, causing the +5V supply to be pulled down. *Table 5-9* lists the assemblies which use the +5V supply.

Verify the unregulated +5V at the positive terminal of A8C19 (+6V to +10V). The voltage should never drop below +5.2V. Locate the analog OR gate node for the +5V regulator (anode of CR12). For normal operation, CR12 should be forward biased and U14D should control the node. The voltage at U14D(13) should be close to that of TP4, causing the U14D(14) to be low enough to forward bias CR12.

Since the +5V regulator circuit is a "foldback" type of regulator (refer to the detailed circuit description), it is difficult to determine if the supply is current limited by measuring the voltage across the current sense resistor on the A8 Motherboard Assembly. The best method to determine if the supply is current limited is to determine which circuit is controlling the analog OR gate node (on the A1 assembly).

Table 5-8. Power Supply Test Connector Voltages

SIGNAL NAME	VOLTAGE RANGE	COMMENTS
V/+5μP *	+4.70 to +5.25V	Located on timebase buffer portion of A1 Assembly.
V/–24 *	–22.6 to –25.9V	Standard timebase TCXO, or warm Option 001 or 010.
	–23.0 to –30.0V	Cold Option 001 or 010
V/+12PS *	+11.2 to +12.8V	
REF/+5 *	+4.94 to +5.06V	
V/+15	+14.75 to +15.25V	
I/+15	(The difference in voltage between this test pin and V/+15 [(I/+15) – (V/+15)] should be +0.15 to 0.50 volts.)	
V/+5OSC *	+4.60 to +5.25V	Internal timebase reference.
	0 to +0.5V	External timebase reference (located in timebase buffer portion of A1 Assembly).
V/+12OSC *	+11.25 to +12.60V	Internal timebase reference.
	0 to +0.5V	External timebase reference (located in timebase buffer portion of A1 Assembly).
V/+3	+2.97 to +3.03V	Adjustment on A3 Assembly.
V/–FAN	–16.5 to –20.0V	30 seconds after power on.
I/+5	(The difference in voltage between this test pin and V/+5 [(I/+5) – (V/+5)] should be +0.05 to +0.18 volts.)	
V/+5	+4.93 to +5.07	
I/–5.2	(The difference in voltage between this test pin and V/–5.2 [(I/–5.2) – (V/–5.2)] should be –0.15 to –0.27 volts.)	
V/–5.2	–5.11 to –5.29V	
* *Denotes that this supply is active in Standby mode.*		

The remaining portion of the +5V regulator circuitry is devoted to controlling the microprocessor Reset (L_μP_RST) and Non-Maskable Interrupt (L_μP_NMI), and turning the LED on if there is a failure with the +5V regulator. Check that A1U8C(14) is HIGH (about +5V) when A1U14D is controlling the analog OR gate node (A1CR12 is forward biased). A1U8C(14) should go low when the HP 5361B is switched to Standby, interrupting the processor to store state variables before power completely goes away.

A1U8D monitors the voltage across A1CR12 exactly as A1U8C does. Verify similar operation of these two comparators by monitoring their ouptuts when switching from STBY to ON, and vice versa. The logic high for A1U8D(13) should be +12V, and logic high for A1U8D(14) should be +5V. When measuring at A1U8D(13), use a 10MΩ probe such as the HP 10014A since the pull-up impedance is 2.15 MΩ.

If the instrument fails to power up properly or fails to save constants when switched to Standby, and the A4 Microprocessor Assembly has been verified, the problem may be due to the reset circuitry for the microprocessor. *Figure 5-3* shows the relationship between the L_μP_NMI signal and the L_μP_RST signal at power on and power off. Verify that these signals have the appropriate timing relationship. The setup notes in the figure are for use with an HP 1744A Storage Oscilloscope. If the correct timing is not observed, the problem probably is caused by A1U7D and A1U8D, or A1U8C.

Verify A1Q20, A8Q1, and A8Q10 by checking base-emitter and collector-emitter voltages. The collector-emitter voltage of the series pass transistor A8Q10 should never exceed 10V. A1CR6 should be forward biased when the HP 5361B is in Standby.

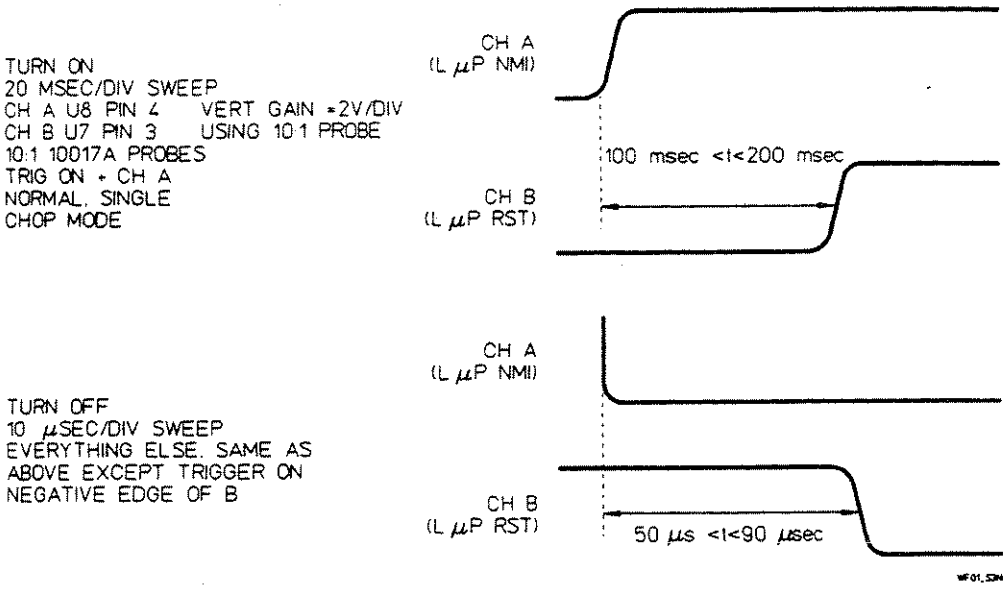


Figure 5-3. L_μP_NMI and L_μP_RST Timing Diagram

+15V REGULATOR. Determine if another assembly is causing the +15V supply to be pulled down. Refer to *Table 5-9* to determine which assemblies use the +15V supply.

Check the +15V UNREG voltage at the positive terminal of A8C3 (+16V to +25V). Next, check that A1CR11 is forward biased and A1U14A is controlling the analog OR gate node of the +15V regulator. The voltage at A1U14A(2) should be close to that of A1U14A(3), causing the output at A1U14A(1) to be low enough to forward bias A1CR11.

If the difference between the I/+15 and V/+15 lines is greater than 0.85V (as verified at the Power Supply Test Connector on A8), the supply is current limited causing A1Q12 and Q13 to pull the analog OR gate node to ground, thereby controlling the node. In this case, CR11 should be forward biased. Check A1Q10 and A8Q7 for proper junction voltages. The collector-emitter junction should never exceed 25V. A1CR9 should be forward biased when the HP 5361B is in Standby.

–5.2V REGULATOR. Determine if a fault on another assembly is loading the supply. Refer to *Table 5-9* to determine which assemblies use the –5.2V supply.

Verify the –5.2V UNREG voltage at the negative terminal of A8C18 (–6V to –10V). On the A1 Assembly, check that A1CR29 is forward biased and controlling the analog OR gate node. A1U14B(5) and A1U14B(6) should be close to ground potential; thus, A1U14B(7) should stay low enough to to keep A1CR29 forward biased.

If the difference between the I/–5.2 and V/–5.2 lines is greater than –0.6V (as verified at the Power Supply Test Connector, A8J7), then the –5.2V supply is current limited and A8Q9 should be on, controlling the analog OR gate node. The A8Q9 collector-emitter voltage should not exceed 10V. A1CR8 should be forward biased only when the instrument is in Standby.

The remainder of the A1 circuitry consists primarily of the –5.2V Current Limit and Drive circuits.

If power is not available at the Microwave Module, verfiy the microwave module turn off circuit (A8Q1, A8Q3, A8Q4, and A8Q5). These transistors turn off two of the dc supplies (+5V SW, +13V SW) to the A12 Microwave Module Assembly during certain measurements. The supplies should be OFF when the HP 5361B is set for INPUT 2 measurements, and ON when the HP 5361B is set to INPUT 1. The "SLEEP" HP-IB command will also turn off these supplies.

The fan circuitry is divided between the A8 and A1 assemblies (A1Q22, A8Q2, and A8Q6). Check the junction voltages of these transistors to locate a faulty transistor.

A8U1 provides -24V regulation. It is recommended that the bottom cover be removed to probe this regulator when troubleshooting the –24V supply.

Table 5-9. Assemblies and Corresponding Power Supplies

ASSEMBLY	POWER SUPPLY								
	+5V	+5V SW	+5V μP	+15V	+13V SW	–5.2V	–24V	+5V OSC	+12V OSC
A1*	X		X	X		X		X	X
A2	X			X		**			
A3	X					X			
A4	X		X						
A5	X			**		X	X		
A6	X			X		X			
A7/A9	X			X					
A8 ***	X	X	X	X	X	X	X	X	X
A10							X	X	X
A11	X								
A12		X			X	X			
A14	X					X			

*The voltage lines of A1 Power Supply Control circuit are for voltage sense purposes only. The A1 circuit draws no current from the voltage sense lines during normal operation.

**The indicated power supply is routed to the listed assembly, but it is not used on the assembly.

***All power supply lines run via the A8 Motherboard connectors.

5-32. TIMEBASE BUFFER BLOCK TROUBLESHOOTING (PART OF A1)

Possible symptoms of a faulty Timebase Buffer circuit:

- No reference signal at rear panel (10 MHz Out, 1 MHz Out).
- Failure on Diagnostic 10, but the HP 5361B functions properly otherwise.
- Option 001 or Option 010 always indicates "cold" or "warm". (This symptom could also originate in the timebase oscillator itself.)
- HP 5361B fails to recognize an external reference.
- HP 5361B always displays 00 000 000 000. (The 10 MHz reference signal is not present. This may also be a fault in the timebase oscillator.)

Diagnostics that may indicate a faulty Timebase Buffer circuit on A1 Assembly:

- Failure on Diagnostic 10: Timebase Verification, but HP 5361B functions properly otherwise.
- Failure on Diagnostic 11: Power Supply Verification. (Refer to Power Supply Troubleshooting, Section 5-29.)
- Diagnostic failures on the A2 through A7 assemblies. (See the Inference Chart, *Figure 5-2.*)
- Self Check or Diagnostic 1 failure.

Some important points to keep in mind when troubleshooting the Timebase Buffer are as follows:

- Most of the circuitry involves detecting and conditioning the external reference signal. Verify that the HP 5361B works with the internal timebase before attempting to troubleshoot this circuit.
- The microprocessor power supply (+5V μP) is on this board. If this supply is faulty, the HP 5361B may not power up at all.
- The 10 MHz timebase is essential for the A3 and the A5 assemblies to function properly.

Before attempting to troubleshoot any portion of this block, verify the power supply voltages listed in *Table 5-10*.

Verify that the internal 10 MHz signal is correct by tracing the signal flow from U10B(5) through U10A, and out to the line drivers (U9A, B, and C). This should be done without an external reference connected to the rear panel.

Connect an external reference (1, 2, 5, or 10 MHz source) to the rear panel **Ref Ext In** connector, A8J1. If the HP 5361B will not recognize an external reference, trace the signal path from the EXT REF IN point at C44 to the output of U4D(11). (See the waveforms in *P/O Figure 5-18*.) Verify that TP3 is logic low (0 V) when an external reference is connected. Also check that TP2 is logic low (assuming that 10 MHz was verified at pin 3 of U10A).

Table 5-10. Timebase Buffer Block Supply Voltages Verification

SIGNAL NAME	TEST POINT	VOLTAGE RANGE	CONDITION OR COMMENT
+12V OSC	Collector of Q9 (top leg)	+11.25 to +12.6V	Critical for Option 001 or 010.
+5V OSC	Collector of Q8 (right leg)	+4.60 to +5.25V	Critical for standard timebase.
+5V μP	Output leg of L5 (top leg)	+4.70 to +5.25V	
+5V	Output leg of L4 (top leg)	+4.65 to +4.25V	
+5V D1	Output leg of L6 (top leg)	+4.65 to +5.25V	
+5V D2	Output leg of L3 (top leg)	+4.65 to +5.25V	
+15V UNREG	Upper leg of U13	+16 to +25 Vdc with up to 0.75 Vp-p ripple.	Full wave rectified, unregulated.
+5V UNREG	Input side of L9 (bottom leg)	+6 to +10 Vdc with up to 0.6 Vp-p ripple.	Full wave rectified, unregulated.

5-33. A2 LOW FREQUENCY INPUT ASSEMBLY TROUBLESHOOTING

Possible symptoms of a faulty A2 Assembly:

- The HP 5361B counts on INPUT 1, but not on INPUT 2.
- The HP 5361B fails to count in both the 50Ω and 1MΩ channels: the input fuse J2F1 is bad, there are connector problems, or power supply problems. In addition, check that the A3 Assembly is counting properly (Diagnostics 30: MRC CH A Verification and Diagnostic 31: MRC CH B Verification). See the Inference Chart, *Figure 5-2*.
- The HP 5361B fails to count properly on either the 50Ω or the 1MΩ channel: a component or components are faulty in the appropriate amplifier/signal conditioning chain.

Diagnostics that may indicate an A2 Assembly failure:

- Diagnostic 20: Low Frequency 50Ω Verification — if the 50Ω channel is faulty.
- Diagnostic 21: Low Frequency 1MΩ Verification — if the 1MΩ channel is faulty.
- Self Check and Diagnostics 20 and 21 during a Diagnostic 1 routine.

Points to consider when troubleshooting the A2 Assembly:

- The 50Ω and 1MΩ channels share the INPUT 2 connector. Therefore, if both channels do not operate properly, the fault could be a bad input fuse (J2F1), cable assembly A2W1, or a bad power supply.
- Diagnostics 20 and 21 depend on the AUX A/B (35 MHz) test signal from the A5 Synthesizer Assembly being good and the A3 Counter Assembly working properly.
- If both Diagnostic 20 and 21 pass, but a channel does not work properly, note that the 35 MHz test signal enters the 1MΩ channel after Q9, and enters the 50Ω channel after U5. Faults in the signal path before these points may be undetected by the diagnostics.
- The 50Ω channel contains a ÷10 counter (U1). The microprocessor firmware multiplies the A3 count by 10 to correct for the division. Since the disabling circuit for the 1MΩ channel is at the U3 multiplexer, a fault in U3 could cause the 1MΩ signal to be sent to the A3 Counter Assembly even though the microprocessor has selected the 50Ω channel, resulting in the displayed count being multiplied by 10.

Check the following power supplies at the listed node before attempting further troubleshooting:

SUPPLY NAME	A2 TEST POINT	ACCEPTABLE RANGE
+15V	CR11 cathode	+14.75 to +15.25 V
+5V	U8(1)	+4.93 to +5.07V

Check the following inputs to the A2 Assembly (refer to Sections 5-23 and 5-24 for information on how to enter and exit the Diagnostics mode):

1. Enter Diagnostic 20, and check U8 pin 6 and pin 4 for the 35 MHz test signal. Note that this signal pulses on and off as the microprocessor loops through the diagnostic routine.

2. Enter Diagnostic 21, and check U8 pin 6 and pin 4 for the 35 MHz test signal. Note that this signal pulses on and off as the microprocessor loops through the diagnostic routine.

3. Check that the L LF TEST signal (bottom leg of R33) is TTL low during Diagnostic 20 and 21, and that it is TTL high during normal operation.

4. Verify that the front panel input fuse J2F1 is good (i.e., that the signal reaches R54 and CR13). (These two components are not the first in the signal path after the fuse, but they do provide the best connection point for the oscilloscope probe.)

5. Probe the bottom leg of R15 and verify that the LF OUT SEL line is TTL high for 1MΩ operation, and TTL low for the 50Ω operation. (Note that the front panel 50Ω and 1MΩ annunciators indicate input impedance mode of INPUT 2.)

> *NOTE*
> *Once the HP 5361B is set to 50Ω, further pressing of the* **50Ω** *key should pulse the LF OUT SEL line high momentarily.*

6. Verify that the H LF 50 line (U9 pin 3) is TTL low for 1MΩ operation, and during Diagnostics 20, 21, the H LF 50 line should be TTL high for 50Ω operation.

Check the following outputs of the A2 Assembly:

1. Set the HP 5361B to the 50Ω mode by setting INPUT 2 for 50Ω operation, and connect a 50 MHz signal at –10 dBm to INPUT 2. Compare LF OUT A (collector of Q1) with waveform A in *P/O Figure 5-19*. Note the dc level and check that the frequency is a factor of 10 less than the input frequency. (The MRC, U5, on the A3 Assembly requires a dc level of +2.65 volts).

2. Verify that the LF OUT A signal does not vary with input signal level as long as the input stays above the sensitivity of the 50Ω channel (25 mV rms). When the signal goes below the sensitivity, LF OUT A should be about 2 volts, dc (i.e., the ac portion of the signal is not present).

3. Switch the HP 5361B to the 1MΩ mode and repeat steps 1 and 2. Compare the signal with waveform B in *P/O Figure 5-19*. Note that the signal is not divided by 10 in this case. For signals with levels below the sensitivity, the output may be about 2 or 3 volts dc, but the ac portion of the signal should disappear.

4. Repeat steps 1, 2, and 3 for LF OUT B (collector of Q2). This signal should be similar to LF OUT A, but inverted.

If the above inputs and outputs are verified and the counter does not count in INPUT 2, refer to the troubleshooting procedure for the A3 Counter Assembly.

If the HP 5361B passes Diagnostics 20 and 21, but fails to count properly in normal operation, check the circuitry before the point where the test signal enters the circuit. For the 50Ω mode, connect a 50 MHz, 100 mV p-p signal to INPUT 2 of the counter and select the 50Ω channel. Connect an oscilloscope probe to the junction of CR7 and CR8. Observe that the signal goes away when switching the HP 5361B to 1MΩ. Set the HP 5361B to the 50Ω mode again and connect the scope probe to the output of U7 (lower leg of R36) or U5(5). Compare this waveform with waveform C in *P/O Figure 5-19*. Note that the level of this signal is about 300 mV p-p. U7 should have a gain of 2.6 to 3.4.

Reduce the level of the signal source so the output of U7 is 100 mV. Move the probe to the output of U5 (lower leg of R27) or U4(1). Compare with waveform D in *P/O Figure 5-19*. Note that U5 should also have a gain of about 3 (2.6 to 3.4).

To check the 1MΩ channel before the point where the test signal enters the circuit, press the **1MΩ** key and connect the oscilloscope probe to the source of Q9 (lower leg of R48). Set the input to –10 dBm level, 50 MHz. Compare this signal with waveform E in *P/O Figure 5-19*. Note that Q8 must be turned off by Q7 during normal operation and turned on by Q7 during diagnostic tests.

For failures on the 50Ω channel, check the output levels of U7 and U5 as described in the previous paragraphs. Set the signal level at the output of U5 to 100 mV p-p (input level at INPUT 2 –5 mV) and compare the output or U4 pin 2 (lower leg of R24) to waveform F in *P/O Figure 5-19*. The U4 output should be about 300 mV p-p; U4 should have a gain of about 3 (2.6 to 3.4).

Next, check U1(8) for proper output as shown in waveform G in *P/O Figure 5-19*. Vary the input level and note that this signal is independent of input level as long as the input is above the sensitivity of INPUT 2. When the signal level becomes too low, the output of U1 should be approximately +5 volts.

Verify the proper operation and adjustment of the peak detector circuit by monitoring the voltage at TP1. Select the 50Ω channel of the HP 5361B and connect a 400 MHz, 17 mV signal to INPUT 2. Vary the signal level above and below 17 mV and note that the detector switches between about +4 volts for signals greater than 17 mV and about +2 volts for signals less than 17 mV.

Verify that U3C and U3D pass the output of U1 to Q1 and Q2 when the HP 5361B is in the 50Ω channel.

For failures in the 1MΩ channel, set the HP 5361B to the 1 MΩ mode and adjust a 50 MHz input signal level for a 100 mV p-p level at U6(10). Compare the output of U6(7) with waveform H in *P/O Figure 5-19*. The output should be about 400 mV p-p for a gain of about 4.

Repeat this procedure for U6A by setting the input (pin 5) to 100 mV and comparing the output (pin 2) to waveform I in *P/O Figure 5-19*. The gain should be between 4 and 6.

Next, check the output of the Schmitt trigger, U6C, at pin 15. Observe the waveform shown in waveform J in *P/O Figure 5-19*.

Verify that the signal is passed through U3B and U3D to Q1 and Q2 when the HP 5361B is in the 1MΩ mode.

5-34. A3 COUNTER ASSEMBLY TROUBLESHOOTING

Possible symptoms of a faulty A3 Assembly:

- Diagnostics that count a test signal fail.
- HP 5361B does not count or counts improperly in one or both inputs.
- Pulse envelope parameters measured incorrectly.

Diagnostics that may indicate an A3 Assembly failure:

- Diagnostics 20: Low Frequency 50Ω Verification and 21: Low Frequency 1MΩ Verification
- Diagnostics 30: MRC CH A Verification and 31: MRC CH B Verification
- Diagnostic 43: Repeated Reset sequence
- Diagnostic 50: LO Verification 29.5 MHz, 35.0 MHz
- Diagnostics 60: IF Verification (Disable INPUT & IF) and 65: IF Verification (Disable INPUT 1)
- Self Check and any of the above diagnostics during a Diagnostic 1 test.

Diagnostics that may provide additional information on the status of the A3 Assembly:

- Diagnostic 7: Display Interpolator Short Calibration — the short calibration counts are displayed for "start" and "stop". U5 (MRC) outputs two 100 ns pulses and the display shows the results after expansion by the interpolation circuitry. Typically, this data should be about 160 counts each. The difference between the start and stop counts should be less than 20.
- Diagnostic 8: Display Interpolator Long Calibration — similar to Diagnostic 7 except 200 ns pulses are expanded and counted. Typically, these are about 380 counts. It is important that the difference between long and short calibration counts are always greater than 128 and less than 256 counts. Typically, this difference is 210.
- Diagnostic 9: Interpolator Measurement — displays the counts derived from the start and stop interpolators due to the input signal and will vary according to the phase between the input signal and the internal reference signal. The value varies between 140 and 395.

NOTE

An input signal must be provided to the HP 5361B (INPUT 1 or INPUT 2) for the above diagnostics to display results other than 00.

- Diagnostic 30: MRC CH A Verification, 10 MHz Timebase — the internal 10 MHz timebase reference signal is counted by U5 (MRC). If this diagnostic passes, but Diagnostic 31: MRC CH B Verification fails, the A5 Synthesizer may be faulty.

- Diagnostic 31: MRC CH B Verification, 35 MHz — similar to Diagnostic 30 except that the AUX B (35 MHz) test signal is counted by U5 (MRC). If this diagnostic passes, but Diagnostic 30 fails, the 10 MHz reference signal may be faulty.

- Diagnostic 32: Interpolator Check — this diagnostic fails if the difference between the two short or the two long calibration counts is greater than 20.

Points to consider when troubleshooting the A3 Counter Assembly:

- Most of the other assemblies in the HP 5361B rely on the A3 Counter Assembly to be operating properly in order for them to pass diagnostic tests. Therefore, if most of the assemblies are failing diagnostic tests and the A4 Microprocessor Assembly, power supplies, and A5 Synthesizer are good, then the A3 circuitry may be at fault.

- If Diagnostics 7 and 8 pass, then most of the circuitry on A3 is operating correctly. The only part not tested is the circuitry in front of U5(MRC) inputs A, B, and C.

- The A5 Synthesizer Assembly must be operative in order for Diagnostic 31 to pass, but not for Diagnostic 30. Diagnostic 30 exercises the A3 Assembly with the 10 MHz reference signal, not the LO frequency.

- U5, the MRC integrated circuit, requires a 3 volt supply. This voltage is regulated from the +5 volt supply and the regulator circuitry on the A3 Assembly (A3U7).

Check the following power supplies at the listed node before attempting further troubleshooting:

SUPPLY NAME	A3 TEST POINT	ACCEPTABLE RANGE
V/+5V	U8(24)	+4.93 to +5.07 V
V/+3V	TP1	+2.97 to +3.03 V (adjustable at R1)
V/–5.2V	U12(8)	–5.11 to –5.29 V

Check the following inputs to the A3 Counter Assembly:

1. Input a 50 MHz signal at –20 dBm into INPUT 2 and select the 1MΩ channel. Set the HP 5361B to minimum resolution (10 kHz) and fastest sample rate. Verify that there is activity on data bus lines 0 through 7 (DBUS – DBUS 7).

2. Verify that there is activity on the following control lines. The HP 5361B should be in the normal (Measurement) operating mode as in step 1.

TEST NAME	A3 TEST POINT	ACTIVITY LEVEL
H MRC READ	U5(40)	Positive pulses
MRC RG 0	U5(1)	Positive pulses
MRC RG 1	U5(2)	Positive pulses
H MRC CSEL	U5(3)	Positive pulses
L MRC STB	U5(8)	Negative pulses
L INTP EN	U8(21)	Negative pulses

3. Input a 1 GHz signal at –20 dBm to INPUT 1 of the HP 5361B. Set the HP 5361B to the Manual mode with a 1 GHz center frequency.

TEST NAME, A3 TEST POINT	CORRECT WAVEFORM (refer to *P/O Figure 5-20*)	
+EVENTS	U12(7)	A
ENVELOPE CTR	U12(10)	B
INPUT SWITCH OUTPUT	U12(2)	C
EXPANDED STI	U10(7)	D
EXPANDED SPI	U3(7)	E
COUNTER/TIMER OUTPUT	U8(17)	F

5-36. A5 SYNTHESIZER ASSEMBLY TROUBLESHOOTING

Possible symptoms of a faulty A5 Synthesizer Assembly:

- HP 5361B fails to acquire signals at INPUT 1 in either Auto or Manual mode, but makes measurements at INPUT 2.
- Diagnostics which rely on counting the 35 MHz test signal fail and the A3 Assembly has been verified (i.e., INPUT 2 counts correctly).
- The red "NOT PHASELOCKED" LED at the top of the A5 Assembly is always on.
- Using a stable source such as a synthesized signal generator with its timebase locked to the HP 5361B, INPUT 1 measurements fluctuate on higher resolution digits, but INPUT 2 measurements are correct and stable. In this case, the LO frequency may not be stable.

Diagnostics that may fail or give further information if the A5 Synthesizer Assembly is faulty:

- Diagnostics 50 (LO Verification 29.5 MHz, 35.0 MHz) and 51 (LO Verification User-Entered Frequency).

  Refer to Section 5-96 for an explanation of the PASS/FAIL indication of Diagnostic 51.

- Diagnostics 52 (LO Sweep 275.0 > 375.0 MHz) and 53 (LO Lower/Upper Frequency Bounds) — will not display PASS OR FAIL information, but may give further insight to the failure.
- Diagnostics 2 (Display IF), 4 (Display LO Frequency), 5 (Display N (integer) and Sideband), and 6 (Display N (fraction) and Sideband) — will give measurement parameter information (LO frequency, harmonic number, and IF).

Points to consider when troubleshooting the A5 Assembly are as follows:

- If the HP 5361B fails to operate properly for inputs to INPUT 1, it is important to use the above diagnostics to determine what data the HP 5361B is using to determine the input frequency. Verify that the A5 Assembly has detected an IF by using Diagnostic 2 (Display IF). Next, verify what LO frequency and what harmonic of the LO has been used. Use these values in the fundamental tuning equation:

  $$f_X = N \cdot LO \pm IF$$

  If Diagnostics 5 (Display N – Integer) and 6 (Display – fraction) indicate the input frequency is on the lower sideband (LSB), the IF must be subtracted from N • LO. If the upper sideband is indicated (USB), the IF must be added to N • LO.

- Note the fractional portion of the harmonic number displayed by Diagnostic 6 (Display – Fraction). If this fractional portion deviates more than 0.30 from an integer value (e.g., 3.30 to 3.70), the HP 5361B will not display a measurement. For fractional portions less than 0.30 from an integer value, the nearest integer value is used in the tuning equation. A large fractional portion of the harmonic number indicates that the counting circuitry is counting a signal with a relatively wide variation in frequency. This may be due to the input signal at the front panel (e.g., frequency modulation) or faults internal to the HP 5361B (e.g., the LO frequency is fluctuating).

- The red LED at the top of the A5 Assembly when lit, indicates that the synthesizer circuitry is NOT phaselocked.

- Diagnostic 51 (LO Verification, User-Entered Frequency) allows the synthesizer to be set to a particular frequency from the front panel. However, to actually use a particular LO frequency to make measurements at INPUT 1, the Manual mode (via HP-IB) can be used. The center frequency (and also the input frequency) to be used for a desired LO can be calculated from the following equation:

  $CF = (LO_{des} \cdot 2) + 70\ MHz$

  where CF = MANUAL mode center frequency

  LO_{des} = desired LO frequency

  70 MHz is the IF generated by this configuration

- The output of the synthesizer should be +15 dBm ±3 dB. Use sufficient attenuation when making spectrum analyzer measurements.

- While the spectrum analyzer should be used when making measurements above the oscilloscope bandwidth (275 MHz), the oscilloscope may be used to indicate the presence of a relatively high frequency signal, but not the amplitude.

- A handy way to verify the A5 Synthesizer frequency is to connect the A5 output to the front panel INPUT 2 connector via a 6, 10, or 20 dB attenuator. First select INPUT 2, 50Ω. Next enter Diagnostic 51 (LO Synthesizer Verification: User-Entered Frequency), and set the LO to various frequencies to be measured at INPUT 2. Pressing the **Reset/Local** key will display the frequency measurement at INPUT 2. Pressing the **Extended Function** key allows a different LO frequency to be entered. Intermediate frequencies in the synthesizer circuit may also be measured using a standard 10:1 oscilloscope probe connected to INPUT 2.

- A5U10 can oscillate if it does not have a signal at its clock input, pin 15 (driven by the VCO circuit). Typically, the oscillating frequency will be about 440 MHz producing a 44 MHz signal at U10's output, pin 2. If a diagnostic which normally counts the

35 MHz test signal fails and shows a frequency of about 44 MHz, the VCO and related circuitry is a likely fault.

Make the following measurements before removing the RF shielding to gain further insight into the cause of the failure:

1. Check the following supplies at the Power Supply Test Connector on the motherboard (A8J7):

SUPPLY NAME	TEST PIN ON A8J7	ALLOWABLE RANGE
V/+5	14	+4.93 to +5.07 V
V/–5.2	16	–5.11 to –5.29 V
V/–24	2	–22.6 to –25.9 V

NOTE

If the HP 5361B is equipped with an Option 001 or 010 Oven Oscillator which has not yet warmed to its operating temperature, the V/–24 Test Connector voltage may be up to –30V (maximum).

2. The A5 Assembly actually uses a –20V supply which is regulated from the –24V supply. This supply can be verified at U5(3). The allowable range at this pin is –18.7V to –21.5V when the HP 5361B is on. When the HP 5361B is in Standby the voltage at this pin should be about –1.35V.

3. Verify that the base of Q5 is approximately +4.75V. If this signal is near ground, it will turn off the VCO.

4. Using Diagnostic 53 (LO Lower/Upper Frequency Bounds), verify that the lower frequency limit of the synthesizer is less than 275 MHz and the upper limit is greater than 375 MHz.

5. Verify the output level of the synthesizer as follows:

   a. Connect the BNC end of the SMB male to BNC adapter cable (HP P/N 05350-60120) to a spectrum analyzer. Set the spectrum analyzer as follows:

      Input Attenuation: 20 dB
      Reference Level: 20 dBm
      Freq. span/div: 20 MHz
      Resolution BW: 300 kHz
      Center frequency at 325 MHz
      Sweep source: internal

b. Disconnect the output of the A5 Assembly from the A12 Assembly at A12J2. Connect the SMB male end of the adapter cable to A5J2.

c. Enter Diagnostic 52 (LO sweep) and note that the output sweep is flat from 275 to 375 MHz at a level of +15 dBm ±3 dB. See waveform A in *P/O Figure 5-22*.

6. Without a signal connected at INPUT 1, and with the HP 5361B in Auto mode, measure the waveform at U1(6) with an oscilloscope. Compare with waveform B *P/O Figure 5-22*. This is the signal that drives the VCO. The output frequency of the VCO varies inversely with voltage (i.e., the most negative voltage corresponds to the highest frequency). The LED at the top of the A5 Assembly will be dimly lit during this test.

7. With an oscilloscope connected to U1(6), set the HP 5361B to Diagnostic 52 (LO Sweep 275.0 > 375.0 MHz). A relatively slow time varying voltage should be seen ranging from approximately –1V to –12V. This is the VCO drive signal during the LO sweep.

Power supplies and their allowable ranges on the A5 Synthesizer Assembly are listed below:

SUPPLY NAME	A5 TEST POINT	ALLOWABLE RANGE
+5VD	C41(+)	+4.93 to +5.07 V
+5VA	C42(+)	+4.91 to +5.06 V
–5.2V	C34(–)	–5.10 to –5.29 V
–24V	C27(–)	–22.4 to –25.8 V (after oscillator warmup)
–20V	U5(3)	–18.7 to –21.5 V (–1.35 V when in OFF – Standby)

Verify the following inputs to the A5 Assembly:

1. Verify the 10 MHz reference signal at pin 1 of A5P1 (pin 2 is a convenient ground). Compare to waveform C in *P/O Figure 5-22*. Note that measuring this signal at U3(7) may cause the dc bias to be shifted slightly. At A5P1, the signal is ac coupled.

2. Set the HP 5361B to Diagnostic 52 (LO sweep) and verify that there is activity on the SYN DATA lines, U4 (pins 2 through 7 and pin 9). These signals should be at TTL levels. The SYN LATCH signal at U4(11) should have activity during this diagnostic. U4(8) should always be low, as this address line is only used during the initialization process at power-up.

3. Enter Diagnostic 50 (LO Verification 29.5 MHz, 35.0 MHz) and verify that U8(11) toggles between 0 and 4 volts during this diagnostic.

Enter Diagnostic 50 and verify the pulsed 29.5 MHz and 35 MHz signal at U8(2) and U8(3). These signals should have a dc offset of about +3.7V with a peak-to-peak amplitude of about 0.8V.

The tests described above should help isolate the specific symptoms to one or more of the following:

- The synthesizer output level is below +12 dBm.
- The synthesizer output is "stuck" at one end of the frequency range.
- The red LED at the top of the A5 Assembly is always on.
- The synthesizer is phase locked (red LED off), but a frequency other than what is programmed is seen at the synthesizer output.
- The synthesizer output is not stable or is noisy.

Suggestions for how to troubleshoot each of the symptoms listed above are as follows:

If the synthesizer output level is below +12 dBm, proceed as follows:

1. The suspect circuitry is U6, U9, or the VCO. The schematic denotes important bias voltages for these components. Verify these to determine if a component is shorted or open. An output signal at some amplitude will probably be seen even if U9 or U6 is faulty, however, it will not be at the typical +15 dBm level.

2. An easy way to check if the VCO is operating at all is to enter Diagnostic 50 and check that the diagnostic passes and displays a frequency of 35 MHz. If a frequency of approximately 44 MHz is displayed, it is probable that U10 is not being clocked (pin 15) or, in other words, not receiving a signal from the VCO. U10 can oscillate at about 440 MHz (the output will be about 44 MHz) if no signal is present at the input to U10. Also check that the amplifier circuitry is operating properly (U6 and Q7).

If the synthesizer is "stuck" at one end of the frequency range, proceed as follows:

1. This symptom can be verified by monitoring the output on a spectrum analyzer while in Diagnostic 53 (LO Lower/Upper Frequency Bounds). The output should be alternating between the high-end frequency and the low-end frequency for normal operation. Monitoring the PLL OUT at U1(6) with an oscilloscope will reveal the same symptom as this is the VCO drive voltage. It is likely that the drive voltage will also fail to alternate between levels.

2. Set the HP 5361B to Diagnostic 51 with an entered frequency of 300.1 MHz. As a starting point to troubleshooting the phase-lock loop, verify that U3 is generally functional. Begin by verifying that the 10 MHz reference signal is present at U3 pin 7 (A5P1 pin 1). Pin 8 of U3 should then have a 100 kHz signal which is the 10 MHz signal divided by 100.

3. Use an oscilloscope to verify activity at U3(3). The frequency at this node should be between 5 and 8 MHz typically. However, at this point it is not important to measure an exact frequency, but rather to determine that a signal exists at all and is stable. If the signal is absent at U3(3), trace back through U7 to U10 to locate the faulty component. Refer to waveform H in *P/O Figure 5-22* (channel A trace).

4. Next, check for activity at U3(15). This should be a 100 kHz signal. If activity has been verified at U3(3) as described above and the signal at U3(15) is not 100 kHz, U3 may be faulty or may not be programmed correctly.

5. If checking the above nodes fails to isolate the problem, the phase-lock loop may be "broken" by desoldering one leg of A5R14. The VCO can then be manually tuned by connecting a power supply to PLL IN at the junction of R14, C19, and CR6. The tuning voltage ranges from +0.5V to –19V. Monitor the LO output with a spectrum analyzer to verify that the VCO frequency can be varied.

6. If the VCO frequency cannot be tuned manually, troubleshoot the notch filter circuitry consisting of C19, CR6, C20, C28, L2, L3, C29, C39, C35, C38, and L9. This can be done by removing power from the A5 Assembly and using an ohmmeter to look for open components or shorted components. With the A5 Assembly installed and the HP 5361B set to ON, verify the dc bias measurements around the VCO circuitry.

7. If the VCO can be tuned manually, the problem probably exists in U10, U7, U3, or the integrator circuitry (U1 and associated components). The measurements described in the following paragraphs to check these components require that the HP 5361B be set to Diagnostic 51 with an LO frequency of 300.0 MHz.

8. First, verify the signal at U10(2) as shown in waveform J in *P/O Figure 5-22*, using an oscilloscope. Display this trace on Channel A of the oscilloscope.

9. Display the signal at U7(11) on Channel B of the oscilloscope. Compare to waveform D in *P/O Figure 5-22*. Now display the signal at U7(3) on Channel B. Compare to waveform E in *P/O Figure 5-22*. These are the signal relationships represented in *Figure 5-8* of the detailed circuit description for the A5 Assembly. Note that it is not possible to probe U7(13) as shown in *Figure 5-8*, as this output is not used in the circuit and does not have a pull-down resistor to facilitate oscilloscope probing.

10. Display the signal at U7(4) on channel A of the oscilloscope and the signal at U7(14) on channel B. Compare to waveform F in *P/O Figure 5-22* and note how the signal at pin 14 lags the signal at pin 4. Repeat this procedure, comparing the signals at U7 pin 3 (Channel A) and U7 pin 14. Compare with waveform G in *P/O Figure 5-22*. These measurements should isolate failures of U7 or U10.

11. To check U3, display the signal at U3(3) on channel A of the oscilloscope and the signal at U3(14) on channel B. Set the LO to 300.1 MHz using Diagnostic 51. Compare to waveform H in *P/O Figure 5-22*. If the LO frequency is a multiple of 5 MHz, the signal at U3(14) will be a constant dc level (Modulus Control).

12. The only remaining circuitry which has not been verified at this point is the integrating circuitry (U1 and associated components). First check the dc bias voltages noted on the schematic. Note that with the phase lock loop broken at R14, the output of the integrator will be held to approximately +0.7V or –18.5V.

If the red LED at the top of the A5 Assembly is always on, proceed as follows:

1. The red LED being on continuously denotes that the synthesizer is never becoming phase locked. Monitor the output of the synthesizer with a spectrum analyzer with the HP 5361B in Diagnostic 52 (LO Sweep). If the output is completely absent, refer to the procedure described under the paragraph "If the synthesizer output level is below +12 dBm ..."; if the output is "stuck" at a particular frequency, refer to the procedure under the paragraph "If the synthesizer is 'stuck' at one end of the frequency range ...". Finally, if the output is oscillating, refer to the following troubleshooting suggestions.

2. Diagnostic 52 (LO Sweep) may give an indication as to what frequencies or set of conditions made the phase-lock loop oscillate. For example, if the VCO is unable to function above or below a particular frequency, the feedback nature of the circuit will cause oscillations as it attempts to drive the VCO to a particular frequency, but is unable to do so.

3. Transistors Q1 and Q2 are used to keep the PLL loop gain approximately constant at lower synthesizer frequencies. If the synthesizer oscillates at lower LO frequencies, these transistors may be a possible cause.

4. A faulty U1 could also cause the phase-lock loop to oscillate. Verify the dc bias voltages around U1 as noted in the schematic.

5. Typically if Q1, Q2, or U1 are causing the oscillations, the PLL OUT signal which drives the VCO will be oscillating sinusoidally or in a smooth, continuous fashion. Alternately, it the oscillations are the result of a problem in the VCO, U6, Q7, U7, or U10 causing an intermittent feedback, the PLL OUT signal will have a much more rough or jagged appearance.

If the synthesizer is phaselocked (LED off), but a frequency other than what is programmed appears at the LO output, proceed as follows:

1. A quick way to verify the condition is to connect the synthesizer output to INPUT 2 (50Ω) via a 6, 10, or 20 dB attenuator. Next, set the LO to a particular frequency using Diagnostic 51. Press **Reset/Local** key, and the LO frequency should be displayed on the HP 5361B.

2. Set the HP 5361B to Diagnostic 52 (LO Sweep) and verify that there is activity on the SYN DATA lines, U4 (pins 2 through 7 and pin 9). These signals should be at TTL levels. The SYN LCH signal, U4(11), should have activity during this diagnostic. U4(8) should always be low, as this address line is only used during the initialization process at power-up. These checks will verify that data from the microprocessor is reaching the synthesizer. If one or more of these lines is inactive during the LO sweep, check U4 by verifying that pin 12 and pins 14 through 19 have activity on them, and pin 13 is low. Check that U3 is operating by verifying a signal at U3 pin 5 (use a 10 MΩ probe).

3. For a specific starting point to troubleshoot, monitor U3(14) while setting various LO frequencies using Diagnostic 51. Choose LO frequencies which are not multiples of 5 MHz to ensure that this line toggles. LO frequencies which are not multiples of 5 MHz will cause the U7-U10 combination of counters to divide by 50 always. Thus, U3(14) will be in a static state. See waveform K in *P/O Figure 5-22.*

4. After verifying the signal at U3(14), check the CMOS-to-ECL converter circuit (CR2, CR3, CR4, CR10, C14, and R9-R11). Verify that the cathode of CR3 (anode of CR2) is approximately +3.75V. Compare the input and output of this circuit with waveform I in *P/O Figure 5-22.*

5. If U3(14) has activity as verified above, U10, U7, and U3 can be checked as described in the next three steps. (The HP 5361B should be set to Diagnostic 51 with an LO of 300.0 MHz for the following measurements.)

6. Display the signal at U10(2) on Channel A of the oscilloscope. Next, display the signal at U7(11) on Channel B of the oscilloscope. Compare to waveform D in *P/O Figure 5-22.* Now, display the signal at U7(3) on Channel B. Compare to waveform E in *P/O Figure 5-22.* These are the signal relationships represented in *Figure 5-8* of the detailed circuit description for the A5 Assembly. Note that it is possible to probe U7(13) as shown in *Figure 5-8,* as this output is not used in the circuit and does not have a pull-down resistor to facilitate oscilloscope probing.

7. Display the signal at U7(4) on Channel A of the oscilloscope and the signal at U7(14) on Channel B. Compare to waveform F in *P/O Figure 5-22,* and note how the signal at U7(14) lags the signal at U7(4). Repeat this procedure, comparing the signals at U7 pin 3 (Channel A) and U7(14). Compare with waveform G in *P/O Figure 5-22.* These measurements should isolate failures of U7 or U10.

8. To check U3, display the signal at U3(3) on Channel A of the oscilloscope and the signal at U3(14) on Channel B. Set the LO to 300.1 MHz using Diagnostic 51. Compare to waveform H in *P/O Figure 5-22*. If the LO frequency is a multiple of 5 MHz, the signal at U3(14) will be a constant dc level (Modulus Control).

If the synthesizer output is not stable or is noisy, proceed as follows:

1. This type of problem could appear as spurs or sidebands clustered around the LO frequency which are not harmonically related to the LO frequency.

2. Spurs which are less than 100 kHz from the LO frequency typically indicate that the phase-lock loop is oscillating. Spurs which are greater than 100 kHz from the LO frequency typically indicate that either the VCO bias is incorrect, or one of the RF amplifiers (U6, Q7, or U9) is oscillating. If the spurs are exactly 100 kHz from the LO, the interference is probably caused by other parts of the A5 circuitry. A starting point for troubleshooting this problem would be to verify the components of the notch filter circuitry. In addition, the low pulses at U3(5) should typically be between 20 and 100 nanoseconds wide. Pulses greater than 100 ns may cause interference and may indicate a faulty U3. Be sure to use a 10 MΩ probe when measuring waveforms at U3(5).

5-37. A6 IF AMPLIFIER/DETECTOR ASSEMBLY TROUBLESHOOTING

Possible symptoms of a faulty A6 Assembly:

- HP 5361B fails to count, or counts improperly, a signal with an amplitude greater than the INPUT 1 sensitivity specification.

- INPUT 1 has poor sensitivity. Verify the LO and IF signals through the use of Extended Functions 2 and 4.

- HP 5361B fails to indicate a leveling or an overload condition (OVLD LED on the A6 Assembly does not turn ON).

Diagnostics that may indicate an A6 Assembly failure:

- Diagnostics 60 (IF Verification, 35 MHz, Disable INPUT 1 and IF) and 65 (IF Verification, 35 MHz, Disable INPUT 1).

- Diagnostics 2 (Display IF), 62 (Disable Hardware IF Detector Flag), 63 (Disable Hardware and Software IF Detector Flag), and 64 (Disable Software IF Detector Flag) — only displays measurement information rather than explicit PASS or FAIL indication.

- Diagnostic 61 (Check Level Detector) — displays whether or not a signal is above the maximum operating range of the A6 Assembly circuitry.

necessary to remove the A7 Assembly from the front sub-panel unless a component or the A9 Display/Driver Assembly must be replaced. If it is necessary to remove the A9 Assembly, use care when disconnecting and connecting the LCD ribbon cable connectors.

WARNING

IF THE W8 RIBBON CABLE FROM THE A7 KEYBOARD/DISPLAY LOGIC ASSEMBLY TO THE A8 MOTHERBOARD/POWER SUPPLY REGULATOR ASSEMBLY IS DISCONNECTED, THE POWER SUPPLY CIRCUITS WILL ALWAYS BE ON WHEN THE INSTRUMENT IS CONNECTED TO AC POWER.

Verify the following voltages:

SUPPLY NAME	A7 TEST POINT	ACCEPTABLE RANGE
+5V	TP1	+4.8 to +5.2 V
+15V	TP4	+14.75 to +15.25 V

If the HP 5361B fails to recognize keyboard entries, proceed as follows:

1. Remove ac power from the rear panel of the instrument, and disconnect the A11 ribbon cable (A11J2W1) from the motherboard.

2. Set the HP 5361B to Diagnostic 70 by performing the following key-press sequence: **Set/Enter, Extended Function, 7, 0, ENTER.**

3. Probe TP7 on the A7 Assembly and verify that the signal goes TTL high when a key is pressed and goes low when the key is released. This signal should remain high as long as the key is held down. An inverted version of this same signal should be present at U2(11).

4. Probe TP8 and verify that this signal pulses TTL high for each key closure, but goes low (that is, does not stay high if the key is held down).

5. Probe U5(13). Verify that the signal is normally TTL high. Check that the signal pulses low when a key is pressed. This is a reset signal (L_KB_READ) from the microprocessor, which allows the processor to read a key and reset the key interrupt. If this signal is not present as described, verify the connections between A4 Microprocessor and A8 Motherboard assemblies as well as the connection of cable W8.

If the above procedures do not isolate the key failure, verify that U4(12) pulses high when pressing a key in row 1 (refer to the A7 Assembly schematic diagram in *Figure 5-24*). Do the same for keys in rows 2, 3, and 4 at pins 11, 9, and 8, respectively. *Table 5-11* identifies the code that should be present for each key at the output pins of U4. Note that the **Reset/Local**

key sets all output lines to the low state. The appropriate code should remain on the data lines until another key is pressed. U3 is a three-state buffer to the bidirectional data bus shared with the LCD data. Since the data at the outputs of U3 depends on whether LCD data or key data is present on the lines, a fault in U3 is best determined by first eliminating U4 as a possible cause.

Table 5-11. Front Panel Keys and Corresponding A7U4 Output Codes

	A7U4 PIN NUMBER				
KEY	15	16	17	18	19
Frequency/Profile	0	0	0	0	1
P Width/Offtime	0	0	0	1	1
PRF/PRI (1/PRF)	0	0	0	1	0
Reset/Local	0	0	0	0	0
Offset	0	0	1	0	1
Smooth	0	0	1	1	0
Scale	0	0	1	1	1
Set/Enter	0	0	1	0	0
Sample Rate	0	1	0	0	0
Resolution	0	1	0	0	1
Extended Function	0	1	0	1	0
HP-IB Address	0	1	1	1	1
Trigger	0	1	1	0	0
Self Check/Cal	0	1	1	0	1
FM Rate/Track	0	1	1	1	0
Gate Mode	0	1	0	1	1
Manual	1	0	0	0	0
50Ω	1	0	0	0	1
Auto	1	0	0	1	0
1MΩ	1	0	0	1	1
Note: "1" = TTL high, "0" = TTL low					

If the Liquid Crystal Display is not operating properly, proceed as follows:

Verify the signals described below before attempting to replace the A9 Display/Driver Assembly. For backlighting failures, verify that +5V is present at the A9 Assembly by measuring at A9J1. If +5V is verified, the A9 Assembly must be replaced.

5-39. A9 DISPLAY/DRIVER ASSEMBLY TROUBLESHOOTING

The A9 Display/Driver Assembly is supported on a throw-away basis when it is determined to be bad. Perform the following checks to determine if the A9 Assembly is bad.

Possible symptoms of a faulty A9 Assembly:

- Power-Up Self Check Display Test fails.
- The Liquid Crystal Display (LCD) is missing segments during a display test or does not operate at all.

If the LCD is not operating properly, proceed as follows:

1. Verify that W8 (A8 Motherboard to A7 Keyboard) and W3 (A7 Keyboard to A9 Display/Driver) cables are not loose.
2. Verify that the +5V is present at the A9 Display/Driver Assembly by measuring at A9J1. If +5V is verified, replace the A9 Assembly as described in the disassembly and reassembly procedure in Section 5-49.

5-40. A11 HP-IB INTERFACE ASSEMBLY TROUBLESHOOTING

Possible symptoms of a faulty A11 HP-IB Interface Assembly:

- HP 5361B does not recognize the HP-IB during the Power-Up Self Test.
- HP 5361B will not respond to any of the HP-IB commands.

Diagnostic 80 (HP-IB Verification) can be used to determine if the HP-IB processor is able to respond to the main processor. This diagnostic cannot determine if all of the HP-IB Interface circuits are functioning properly.

If Diagnostic 80 fails and the counter passes all other diagnostics, verify that the ribbon cable, A11J2W1 is properly seated in its motherboard connector, A8J6.

Verify the following voltages on the A11 Assembly:

SIGNAL NAME	TEST POINT	RANGE
+5V	+5 (TP1)	+4.8 to +5.2 V
+5V CMC	U2(24)	+4.8 to +5.2 V

For problems involving a particular controller, it is recommended that an HP 59401A Bus Analyzer and a logic analyzer be used to determine the cause of the problem. As an initial test, verify that the interface responds properly to the HP-IB Verification program found in Section 1 (Performance Tests) for HP 9000 series 200 or 300 Desktop Computers. The HP-IB Verification program is available on floppy discs 05361-13502 (5 1/4-inch) or 05361-13501 (3 1/2-inch). Also verify that the controller interface is functioning properly.

Install the A11 assembly into the instrument and reset the A11S1 DIP switch to its original setting. Enter the following program into an HP Desktop Computer and connect the HP-IB interface to the HP 5361B. Note for line 10, the appropriate address for the counter should be entered if different than 714.

```
10 REMOTE 714
20 LOCAL 7
30 GO TO 10
40 END
```

Run this program and verify activity at A11U5(27). If there is no activity at this point, trace back through U4D, U4A, and U2 to locate the fault. Also verify activity on U5 pins 3, 4, 5, 6, 16, 17, and 18. If there is no activity on these lines, a problem may exist in the interface between the A4 Microprocessor Assembly and the A11 HP-IB Interface Assembly.

5-41. A12 MICROWAVE MODULE TROUBLESHOOTING (U1 SAMPLER)

Possible symptom of a faulty A12 Assembly:

- Counter portion of the HP 5361B will not measure an input of proper frequency and level at INPUT 1.

There are no diagnostics available which directly test the A12 Microwave Assembly or the U1 Sampler.

Verify that all the following tests and diagnostics return a "PASS" indication before attempting to troubleshoot the Microwave Module.

Points to consider when troubleshooting the A12 Microwave Module:

- The GaAs sampler (U1) is located in the A12 Microwave Module. This component is extremely sensitive to static electricity and care should be taken to observe proper ESD procedures when working with this component. It is strongly recommended that the circuitry around the sampler be verified before attempting to handle or replace it.

- Do not attempt to perform dc tests on the pins of the sampler. The abrupt application of current to the GaAs circuitry caused by using a standard voltmeter may damage an otherwise good component.

- The LO INPUT to the Module should be +14 dBm at the A12J1 input. Use proper attenuation on test equipment when measuring this signal. The LO INPUT must be at a proper level in order to generate an IF OUTPUT signal.

- If there is any IF OUTPUT at all from the A12 Assembly, the U1 sampler is probably good.

- The circuitry on this board should be tested using an active probe such as the HP 1124A (100 MHz active probe). A standard 1MΩ oscilloscope probe does not have the required 400 MHz bandwidth, resulting in inaccurate signal level measurements.

Refer to Section 5-46 for the Microwave Module disassembly procedures to remove the cover of the Module, and verify the following power supply voltages:

SUPPLY NAME	A12 TEST POINT	ACCEPTABLE RANGE
–5V	feedthrough pin with blue wire attached	–5.11 to –5.29 V
+5V SW	feedthrough pin with yellow wire attached	+4.93 to +5.07 V
+13V SW	feedthrough pin with red wire attached	+12.7 to +14.3 V

Verify the output of the A5 Synthesizer Assembly as follows:

1. Connect the SMB to BNC adapter to the A12 end of W2. Connect the BNC end of the adapter to a spectrum analyzer.

2. Set the spectrum analyzer for 30 dB input attenuation with a 20 dBm reference level.

3. Set the HP 5361B to Diagnostic 51 (LO Verification, User-Entered Frequency) and set the LO frequency to 325.0 MHz.

4. Center the output on the spectrum analyzer display with a frequency span of 10 MHz per division.

5. Set the counter to Diagnostic 52 (LO Sweep 275.0 > 375.0 MHz) and verify that the signal sweeps across the entire display (275 MHz to 375 MHz) and is level at +14 ±1 dBm (nominal). If this is not verified, refer to the A5 Assembly troubleshooting procedures. After verifying the LO signal, reconnect W2 (the cable supplied with the counter) to the LO INPUT at A12J2.

Verify the IF OUTPUT signal as follows:

1. Disconnect the IF OUTPUT A6W1 cable and connect the SMB to BNC adapter to the IF OUTPUT of the A12 Assembly.

2. Connect the BNC end to the spectrum analyzer and set the spectrum analyzer for 0 dB input attenuation and a –10 dBm reference level. Set the frequency span to 20 MHz per division.

3. Apply a 770 MHz signal at –20 dBm to INPUT 1 of the counter. Set the counter to Manual mode with a center frequency of 770 MHz.

4. Center the IF signal on the spectrum analyzer display. Vary the input frequency from 710 MHz to 875 MHz, verifying that the IF signal stays flat ±3 dB across the range of 10 MHz to 175 MHz at a level between –21 and –26 dBm.

If the IF signal is verified, the A12 Assembly is in proper working order. Refer to the A6 Assembly troubleshooting procedures, and begin troubleshooting the A6 circuitry at a point prior to where the AUX diagnostic test signal enters the main signal path.

If the IF signal is present, but not the correct amplitude or not flat across the sweep, then the U1 Sampler is not at fault. In this case, the suspect circuitry is Q1, U1, and U2. If the IF signal is not present, first check the LO matching and amplifier network.

To check the LO amplifier network, proceed as follows:

1. Check the bias voltage at the R8-R9 node. This voltage should be about 0.5V with no LO signal applied. The collector of Q2 should be at about +13V.

2. Set the counter to Diagnostic 52. Using the HP 1124A 100 MHz active probe with a 100:1 divider tip, compare the signal at the collector of Q2 with waveform A in *P/O Figure 5-26*. Check that the LO level does not drop below +20 dBm. (Remember that because the 100:1 divider tip was used, the spectrum analyzer measurement should have 40 dB added to it.) The heat sink on Q2 may have to be temporarily removed to make this measurement.

To check the IF preamplifier network, proceed as follows:

1. Verify that the base of Q1 is about –0.018V dc and the emitter is about –0.84V. The collector should be about +4.4V.

2. The input bias voltage to U1 and U2 should be about –0.84V, and the output bias voltage should be about +3.18V.

3. The dc voltages described above are typical and may vary due to the typical variations of each component. Generally however, a deviation of more than 0.1V from these values is an indication that a problem exists.

Set the counter to Manual mode with a 1 GHz center frequency. Apply a 1 GHz, 0 dBm signal to INPUT 1. Using the 1124A 100 MHz active probe with the standard tip, compare the outputs of Q1, U1, and U2 with waveforms B, C, and D in *P/O Figure 5-26*. Check for proper gain at each amplifier stage. Note that the noise seen in these measurements is due to the removal of the RF cover of the Microwave Module. During normal operation with the cover in place, this noise would not be present.

If the LO amplifier network is good, but there is no IF output from the U1 Sampler, then the sampler should be replaced. Refer to the disassembly procedures, Section 5-46.

5-42. A14 GATE BOARD ASSEMBLY TROUBLESHOOTING

Possible symptoms of a faulty A14 Gate Board Assembly:

- Instrument fails to make measurements at CW or pulsed frequencies.
- Instrument fails to make measurements at pulsed frequencies with the external gate input.
- No Scope View output.

Diagnostics that may indicate an A14 Assembly failure:

- Diagnostic 34: Display Gate Bias Error
- Diagnostic 54: Gate Bias Calibration

Points to consider when troubleshooting the A14 Assembly:

- There are four input lines from th A6 IF Assembly and three input lines from the A4 Microprocessor Assembly.
- There are three output lines from the A14 Gate Board Assembly that are inputs to the A3 Counter Assembly.
- Use the appropriate diagnostics to confirm proper operation of the A3, A4, and A6 assemblies.

To troubleshoot the A14 Assembly, perform the following procedures.

Verify the following power supplies:

SUPPLY NAME	A14 TEST POINT	ACCEPTABLE RANGE
+5V	L1(2)	+4.8 to +5.2 V
–5.2V	L2(2)	–5.10 to –5.29V

Verify the following inputs to the A14 Assembly when the instrument is in the **CW mode**:

1. Connect a 1 GHz, –10 dBm **sine-wave** signal to INPUT 1.
2. Set the instrument to Auto mode.
3. Verify the following waveforms:

SIGNAL NAME	A14TEST POINT	WAVEFORM (see *P/O Figure 5-28*)
–IF_NEW	U32(4)	A
+IF_NEW	U32(5)	B
L_HOLD_OFF	U28(2)	C

4. Verify the following outputs from the A14 Assembly when the instrument is in the **CW mode**:

SIGNAL NAME	A14 TEST POINT	WAVEFORM (see *P/O Figure 5-28*)
EVENTS	U33(2)	D

Verify the following inputs to the A14 Assembly when the instrument is in the **Pulse mode**:

1. Connect a 1 GHz, –10 dBm **pulsed signal** to INPUT 1 by performing the following steps:
   a. Connect the 50Ω OUTPUT signal of an HP 5359A Time Synthesizer to to the MODULATION INPUT PULSE input connector of an HP 8340B Synthesized Sweeper.
   b. Connect the RF OUTPUT of the HP 8340B Synthesized Sweeper to INPUT 1 of the HP 5361B.
   c. On the HP 5359A, set pulse WIDTH to 100.00 ns and PERIOD to 600.00 ns.

d. Set the HP 8340B's MODULATION to PULSE mode, and set the pulse signal to be 1 GHz at -10 dBm.

2. Set the HP 5361B to Auto mode.

3. Verify the following waveforms:

SIGNAL NAME	A14 TEST POINT	WAVEFORM (see *P/O Figure 5-28*)
-IF_NEW	U32(4)	E
+IF_NEW	U32(5)	F
H_ENV_IF	U31(4)	G
L_IF_INBAND	U11(1)	H
H_GATE	U28(1)	I
L_HOLD_OFF	U28(2)	J
L_INP_RST	U30(5)	K
H_MRC_READ	U3(22)	Positive pulses
L_MRC_STB	U3(23)	Negative pulses
MRC_REG0	U3(19)	L
MRC_REG1	U3(20)	M

4. Verify the following outputs from the A14 Assembly when the instrument is in the **Pulse mode:**

SIGNAL NAME	A14 TEST POINT	WAVEFORM (see *P/O Figure 5-28*)
ENVELOPE_OUT	U16(1)	N

If the above signals are incorrect, trace back through the circuitry to determine the cause. These signals must be correct.

If after performing the above procedure and the problem has not been discovered, the A14 Gate Board Assembly should be removed and replaced with another A14 Assembly. This can be arranged by contacting your nearest HP Sales and Support Office.

5-43. DISASSEMBLY AND REASSEMBLY

The following procedures are divided into four categories, as follows:

1. Cover removal (Section 5-44)
2. Front panel assembly removal (Section 5-45)
3. A12 Microwave Module disassembly (Section 5-46)
4. A9 Display/Driver Assembly removal and installation (Section 5-47)

The cover removal procedures describe how to open the instrument to gain access to all the serviceable assemblies within the counter. The front panel assembly removal procedure describes how to separate the front panel keyboard and display assembly from the mainframe and the Microwave Module to allow access for service, parts replacement, and option installation. The Microwave Module disassembly procedure describes the steps necessary for replacing the A12 Microwave Assembly or the U1 Sampler, without requiring removal of the front panel assembly. Since the Display Module in the front panel assembly is not repairable, the module must be removed as a unit, as described in the Display Module removal procedure, and a new module must be installed.

Reassembly procedures for all of the items mentioned above are essentially the reverse of the disassembly procedures. Where applicable, special reassembly instructions are given. Refer to Section VI, Replaceable Parts, for exploded views of all instrument assemblies discussed in the following procedures.

CAUTION

The electrical assemblies and components involved in the following steps are all static sensitive. To prevent electrostatic damage, all assemblies and components should be handled at a static-free work area, and in accordance with the procedures described in Section 5-8.

The following tools are required for this procedures:

1. Large (2 point) Pozidriv screwdriver.
2. Small (1 point Pozidriv screwdriver.
3. Needle-nose pliers.
4. 1/4 inch open-end wrench.
5. 3/4 inch knurled nut driver

6. 5/16 inch open-end wrench.

7. 5.5 mm hex nut driver.

8. Small flat-bladed screwdriver.

Before performing any disassembly or reassembly procedures, the following steps must be performed:

1. Set POWER switch to STBY position.

2. **Remove ac line power cord from rear panel power module.**

5-44. Cover Removal

WARNING

WHEN THE COVERS ARE REMOVED FROM THE HP 5361B, LINE VOLTAGES ARE EXPOSED WHICH ARE DANGEROUS AND MAY CAUSE SERIOUS INJURY IF TOUCHED. DISCONNECT POWER.

To remove the top cover, loosen the recessed Pozidriv screw at the rear of the top cover. The screw does not come out of the cover; slide the top cover to the rear 1/4 of an inch and lift off.

To remove the bottom cover, turn the instrument on its side and loosen the recessed Pozidriv screw at the rear of the bottom cover, in the same way as for the top cover. Slide the bottom cover to the rear until it can be lifted off.

5-45. Front Panel Assembly Removal

To remove the front panel assembly from the instrument, proceed as follows:

1. Remove the top cover, as described in Section 5-44.

2. Remove the top trim strip (MP10) from the top of the front frame (MP5) using a small flat-bladed screwdriver.

3. Remove 5 screws (H7) and 3 lockwashers (H22) from the top of the front frame. Next, remove the two front feet (MP9) from the instrument, and 5 screws (H7) and 3 lockwashers (H22) from the bottom of the front frame.

4. Disconnect the RF coaxial cable (A2W1) from the front panel INPUT 2 BNC connector, using a 1/4 inch wrench.

5. With a pair of needle-nose pliers, carefully remove the dc power to the Microwave Module (W5) from its motherboard connector (A8J11). Be sure to pull the cable connector straight up when removing it from the motherboard connector to avoid damage to the connector pins.

6. Disconnect the RF coaxial cables (W2, A6W2) connecting the A5 and A6 Assemblies to the Microwave Module RF connectors (A12J1, A12J2). Be sure to pull the cables straight down when removing them from the RF connectors. DO NOT TWIST OR BEND the SMB connections, as doing so may cause damage to the cable or Microwave Module connectors.

7. Pull the front panel assembly, with the attached Microwave Module, about 2 inches away from the instrument and disconnect the keyboard ribbon cable (W1) from its motherboard connector (A8J10).

8. If removing a HP 5361B front panel assembly, unscrew the knurled nut (H12) from the N-type INPUT 1 connector, using the 3/4 inch knurled nut driver. Separate the Microwave Module from the front panel assembly. This completes the front panel assembly removal for the HP 5361B.

5-46. A12 Microwave Module Disassembly

CAUTION

The components of the Microwave Module are extremely sensitive to electrostatic discharge, especially the U1 sampler. Use the precautions:

ENSURE that all disassembly and reassembly procedures are performed only at static safe work stations providing proper grounding for service personnel.

ENSURE that components and assemblies are stored in static shielding bags or containers.

DO NOT remove components or assemblies from static shielding containers until you are ready to install them.

AVOID touching component leads.

The following procedure describes how to disassemble the Microwave Module without removing the front panel assembly (see *Figure* 3-3). Proceed as follows:

1. Remove the top cover, as described in Section 5-44.

2. Remove right side cover (with attached strap handle) by removing two screws (H26) which hold the strap handle (MP14) and side cover (MP17) to the instrument.

3. Remove four screws (H9) on the top of the Microwave Module cover (MP27), and pull the cover away from the Module.

4. Remove the Microwave Module center section, and be careful not to damage the RFI round-strip conductive elastomer.

5. Remove the two screws (H6) which can be seen through holes in the A12 Microwave Assembly. DO NOT REMOVE the A12 assembly at this time.

6. Loosen the semi-rigid cable (INPUT 10 SMA) connection at the input to the U1 Sampler (U1J1) using a 5/16 inch wrench. (If Option 006 is installed for the HP 5361B, loosen the end of the AT1 Limiter connected to the U1J1 input.)

7. With a pair of needle-nose pliers, remove the Microwave Module dc power cable (W5) from its motherboard connector (A8J11). Be sure to pull the cable connector straight up when removing it from the motherboard connector to avoid damage to the connector pins.

8. Place your fingers around the bottom half of the Microwave Module cover (MP28) and gently pull up the bottom cover and attached A12 assembly just far enough to gain access to the coaxial cable SMB connections underneath the Module (A12J1, A12J2). Disconnect the RF coaxial cables (W2, A6W2) from the A12 SMB connectors. Be sure to pull the cables straight down; DO NOT TWIST OR BEND the SMB connections, as doing so may cause damage to the cable or Microwave Module Connectors.

9. Separate the A12 Assembly from the bottom cover by removing the two small hex nuts (H28) and lockwashers (H18) from the two SMB RF connectors, and the larger hex nut (H29) and lockwasher (H17) from the SMA sampler input connector.

10. Carefully push the A12 Assembly up out of the bottom cover by pressing on the SMB connectors, taking care not to bend the pins of the four feedthrough capacitors (C1-C4) which are plugged into pin sockets on the A12 board. BE CAREFUL not to lose the plastic spacer (MP36) which fits around the sampler SMA connector, between the A12 Assembly and the bottom cover.

CAUTION

Before performing the following steps, make sure that you are attached to a properly connected static grounding strap.

11. To remove the sampler from the A12 board, hold the sampler body while removing the two small screws (U1H1) which attach the sampler board. Pull the sampler straight up off the board, being careful not to bend the sampler leads as they are withdrawn from their pin sockets.

12. Immediately after removal, place the sampler in an anti-static bag of container; the U1 sampler is very static-sensitive, and can be damaged if handled without static protection. AVOID TOUCHING THE SAMPLER LEADS. This completes Microwave disassembly and sampler removal.

The reassembly of the sampler and the Microwave Module is simply the reverse order of the disassembly procedure described above, but the following precautions must be taken:

- When installing the U1 Sampler into the A12 board, be sure to hold the sampler by the body while installing the U1H1 screws. DO NOT TOUCH the sampler leads. Also, be sure to use the new U1H1 screws supplied with the replacement sampler. DO NOT reuse the old screws.

- When replacing the A12 Assembly, with the attached sampler, back into the bottom cover, be sure that the MP36 plastic spacer is placed onto the sampler's SMA connector between the sampler and the bottom cover. Also, be careful to line up the leads of the four feedthrough capacitors (C1-C4) with their sockets on the A12 board. BE CAREFUL not to bend the leads of the capacitors when installing the board.

- The two H18 lockwashers and one H17 lockwasher must be replaced when reinstalling the hex nuts onto the RF connectors. The lockwashers are essential for RFI suppression. Be sure to tighten the hex nuts snugly (about 8-10 inch pounds).

- Be sure that the W2 cable from the A5 Assembly, and the A6W2 cable from the A6 Assembly are correctly connected to the appropriate Microwave Module connector (A12J2 and A12J1, respectively). Refer to connection information described on the top of the Microwave Module's RF shielding scan.

- Be sure that the Microwave Module dc power cable (W5) is connected correctly to the four feedthrough capacitor leads between the two SMB connectors, as follows:

Blue	— –5/2V
Yellow	— +5V
Gray	— Ground
Red	— +13V

5-47. A9 Display/Driver Module Removal And Installation

CAUTION

The Display/Driver Assembly is extremely sensitive to electrostatic discharge. Use the following precautions:

ENSURE that all disassembly and reassembly procedures are performed only at static safe work stations providing proper grounding for service personnel.

ENSURE that the Display/Driver Assembly is stored in a static shielding bag or container.

DO NOT remove a replacement Display Module from its static shielding container until you are ready to install it.

AVOID touching circuit traces and component leads.

NOTE

The Display/Driver Assembly is not a repairable assembly. A replacement A9 Assembly (HP P/N 05350-60123) is available from the factory. Refer to Section 3 (Replaceable Parts) for ordering information.

To remove the A9 Display/Driver Assembly, proceed as follows (see *Figure* 3-2):

1. Remove cover as described in Section 5-44.
2. Remove the Front Panel Assembly from the instrument as described in Section 5-45.
3. Remove four nuts (H11) and lockwashers (H21) from the back of the A9 Assembly with a 5.5 mm nut driver.
4. Pull the A9 Assembly, up off of the rivet-on studs.

To install a replacement A9 Assembly into the front panel assembly, proceed as follows:

1. Check the display window (MP35) to be sure it is clean, and located properly in the MP21 sub-panel.
2. Slide the A9 Assembly and the attached shield down over the four studs on the sub-panel.

3. Install the four H11 nuts and H21 lockwashers onto the sub-panel studs, and tighten with the 5.5 mm nut driver. DO NOT OVERTIGHTEN THE NUTS.

4. This completes the Display Module installation. The Front Panel Assembly can now be installed back into the instrument.

5-48. A11 HP-IB Interface Assembly Removal and Installation

WARNING

WHEN THE COVERS ARE REMOVED FROM THE HP 5361B, LINE VOLTAGES ARE EXPOSED WHICH ARE DANGEROUS AND MAY CAUSE SERIOUS INJURY IF TOUCHED. DISCONNECT POWER.

1. Turn off HP 5361B, and remove all power connections.

2. Remove top cover as described in Section 5-44.

3. Disconnect the HP-IB Interface Assembly's cable from A1J6, located on A8 Motherboard Assembly.

4. Remove screw that goes through the HP-IB Assembly and into the standoff on the motherboard.

5. Remove the two black standoff studs and lockwashers that attached the HP-IB Assembly to rear panel.

6. Pull and remove HP-IB Interface Assembly.

7. Reverse steps to reinstall assembly.

5-49. THEORY OF OPERATION

The following pages describe the operation of the HP 5361B. The description begins with a discussion of the harmonic heterodyne down-conversion technique, followed by discussions of FM tolerance, sensitivity, and measurement time. Next, overall counter operation is described, showing the function and relationships of the major assemblies (a complementary overall block diagram of the HP 5361B is provided in *Figure 5-15*). (A component level description for each field repairable board assembly is provided, beginning at Section 5-133.)

5-50. HARMONIC HETERODYNE TECHNIQUE

The microwave frequency counter portion of the HP 5361B uses a harmonic heterodyne down-conversion technique to convert the microwave input frequency into the range of its internal low frequency counter. This technique combines the best performance characteristics of heterodyne converters and transfer oscillators to achieve high sensitivity, high FM tolerance, and automatic amplitude discrimination.

All microwave counters must down-convert the unknown microwave frequency to a low frequency signal which is within the counting range of an internal low frequency counter (about 100 MHz). Heterodyne converters down-convert the unknown signal, f_X, by mixing it with the Nth harmonic of an accurately known local oscillator frequency, f_{LO}, such that the difference frequency, f_{IF} (defined as $f_X - N \cdot f_{LO}$ if $f_X > N \cdot f_{LO}$, or as $N \cdot f_{LO} - f_X$ if $f_X < N \cdot f_{LO}$), is within the counting range of the low frequency counter. The counted frequency, f_{IF}, is then added to (or subtracted from, if $f_X < f_{LO}$) the Nth multiple of the local oscillator frequency to determine the input frequency.

Like heterodyne converters, transfer oscillators also mix the unknown signal with harmonics of an internally generated signal, f_{VCO}. When one of the harmonics of the VCO signal, $N \cdot f_{VCO}$, mixes with the unknown to produce zero beat, the VCO frequency is measured by the low frequency counter. After determining which harmonic produced zero beat, the measured VCO frequency is multiplied by N to determine the input frequency ($f_X = N \cdot f_{VCO}$).

Figure 5-4 is a simplified block diagram of the harmonic heterodyne technique. In this technique, all of the harmonics of an internal oscillator (a programmable frequency synthesizer locked to the counter's time base) are simultaneously mixed with the unknown signal by the sampler and sampler driver (samplers are like harmonic mixers — the sampling diodes in the HP 5361B sampler conduct only for a few picoseconds during each period of the sampling signal, generating a comb of frequencies which span the RF input bandwidth). The output of the sampler consists of sum and difference frequencies produced by each harmonic of the internal oscillator mixing with the unknown. The programmable frequency synthesizer is decremented in frequency until one of the outputs of the sampler is in the counting range of the low frequency counter. The IF detector detects when the IF is in the range of the low frequency counter and sends a signal which causes the microprocessor to stop decrementing the frequency of the frequency synthesizer. The IF is then counted by the low frequency counter.

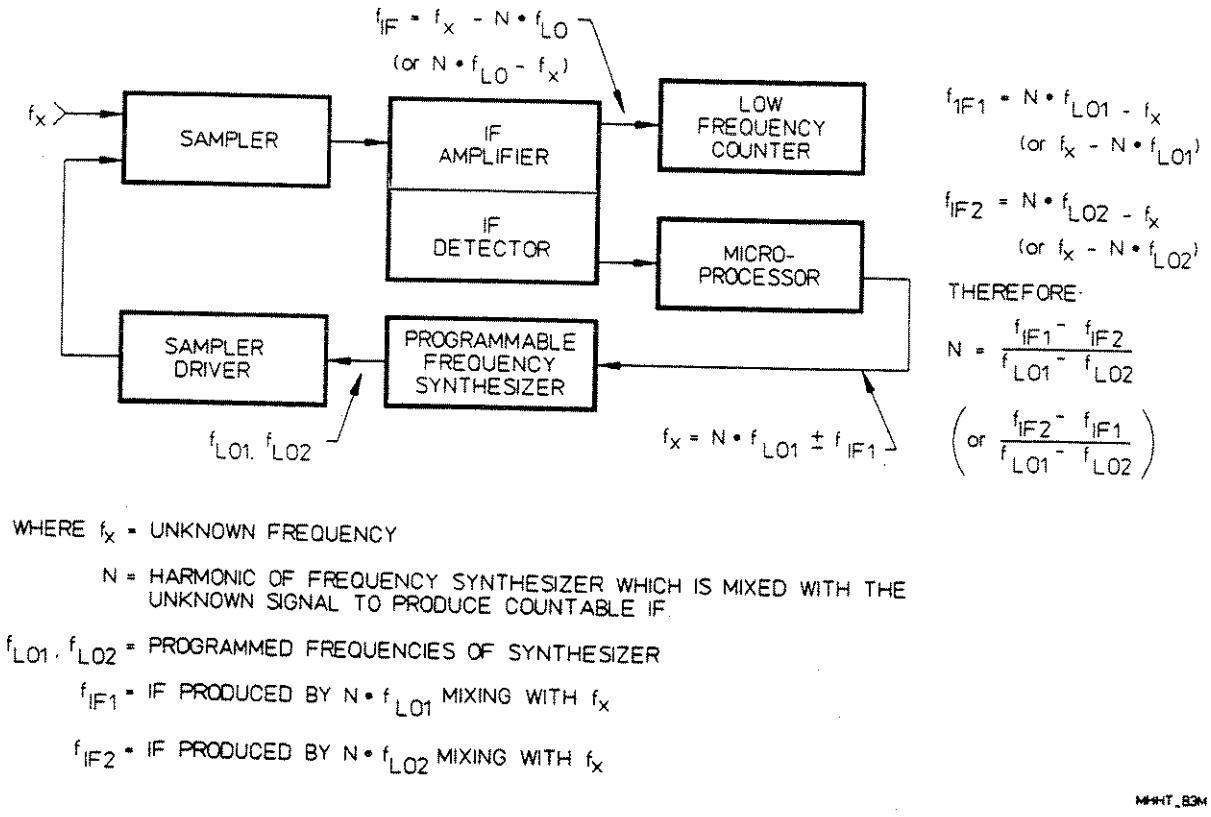


Figure 5-4. Harmonic Heterodyne Technique

The frequency, f_{LO1}, of the programmable synthesizer is known. The IF frequency, f_{IF1}, is known since it is counted by the low frequency counter. Still to be determined are the N number and the sign (±) of the IF (the sign of f_{IF1} will be (+) if $N \cdot f_{LO1}$ is less than f_x; the sign of f_{IF1} will be (–) if $N \cdot f_{LO1}$ is greater than f_x).

To determine N and the sign of f_{IF1}, one more measurement must be taken with the synthesizer frequency offset from its previous value by a known frequency to produce f_{LO2} ($f_{LO2} = f_{LO1} - \Delta f_{LO}$). This produces an IF, f_{IF2} (guaranteed by the software to be based on the same N number and sideband as f_{IF1}), which is counted by the low frequency counter. N is determined by the following:

$$f_{IF1} = N \cdot f_{LO1} - f_x \qquad (\text{if } N \cdot f_{LO1} > f_x)$$

$$f_{IF2} = N \cdot f_{LO2} - f_x \qquad (\text{if } N \cdot f_{LO2} > f_x)$$

$$\text{therefore } N = \frac{f_{IF1} - f_{IF2}}{f_{LO1} - f_{LO2}} \text{ (rounded the nearest integer)}$$

or, if f_x is greater than $N \cdot f_{LO1}$:

$$f_{IF1} = f_x - N \cdot f_{LO1} \qquad (\text{if } N \cdot f_{LO1} < f_x)$$

$$f_{IF2} = f_x - N \cdot f_{LO2} \qquad (\text{if } N \cdot f_{LO2} < f_x)$$

$$\text{therefore } N = \frac{f_{IF1} - f_{IF2}}{f_{LO1} - f_{LO2}} \text{ (rounded the nearest integer)}$$

Referring to *Figure 5-5*, it is seen that if f_x is greater than $N \cdot f_{LO1}$, then f_{IF1}, produced by mixing $N \cdot f_{LO1}$ with f_x, will be less than f_{IF2}, produced by mixing $N \cdot f_{LO2}$ with f_x, since f_{LO2} is less than f_{LO1}, by Δf. However, if f_x is less than $N \cdot f_{LO1}$, then f_{IF1} will be greater than f_{IF2}.

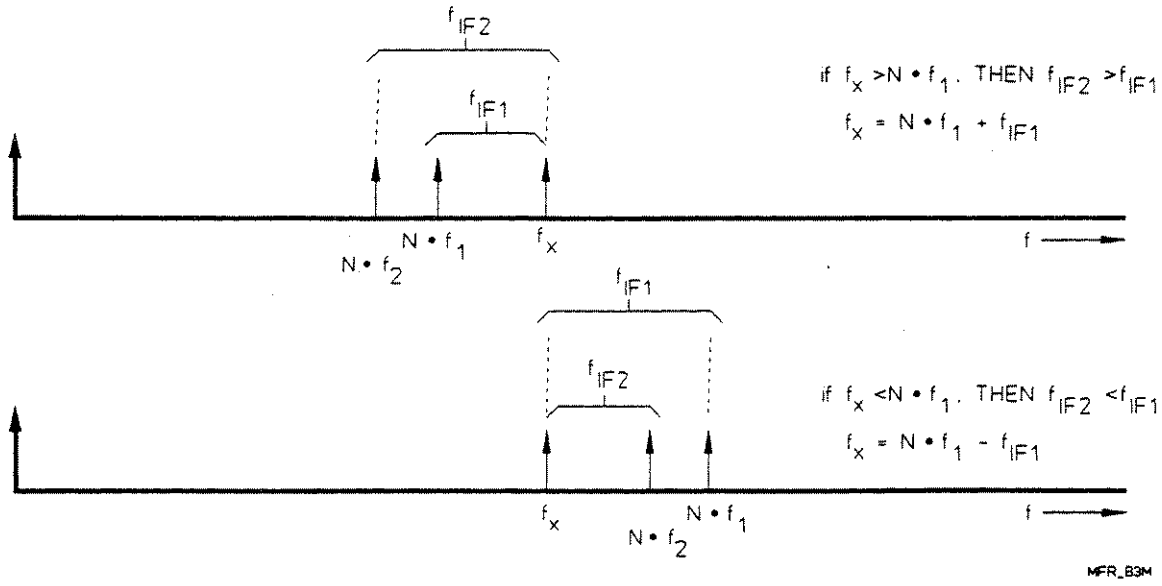


Figure 5-5.Frequency Relationships

The value of N is computed from:

$$N = \left| \frac{f_{IF1} - f_{IF2}}{f_{LO1} - f_{LO2}} \right|$$

The unknown frequency is then computed from the following:

$f_X = N \cdot f_{LO1} - f_{IF1}$ (if $f_{IF2} < f_{IF1}$)

$f_X = N \cdot f_{LO1} + f_{IF1}$ (if $f_{IF1} < f_{IF2}$)

Since the mean frequency of the synthesizer is known to the accuracy of the counter's timebase and the IF is measured to the accuracy of the counter's timebase, the accuracy of the microwave measurement is limited only by the timebase error and the residual stability of the synthesizer.

5-51. FM TOLERANCE

If all signals into the counter could be guaranteed to have little or no FM, the counter could operate quite simply as described previously. However, many signals in the microwave region, such as those originating from microwave radios, have significant amounts of frequency modulation. To prevent FM on the signal from causing an incorrect computation of N, the harmonic heterodyne technique is implemented as described in the following paragraphs. (See *Figure 5-6.*)

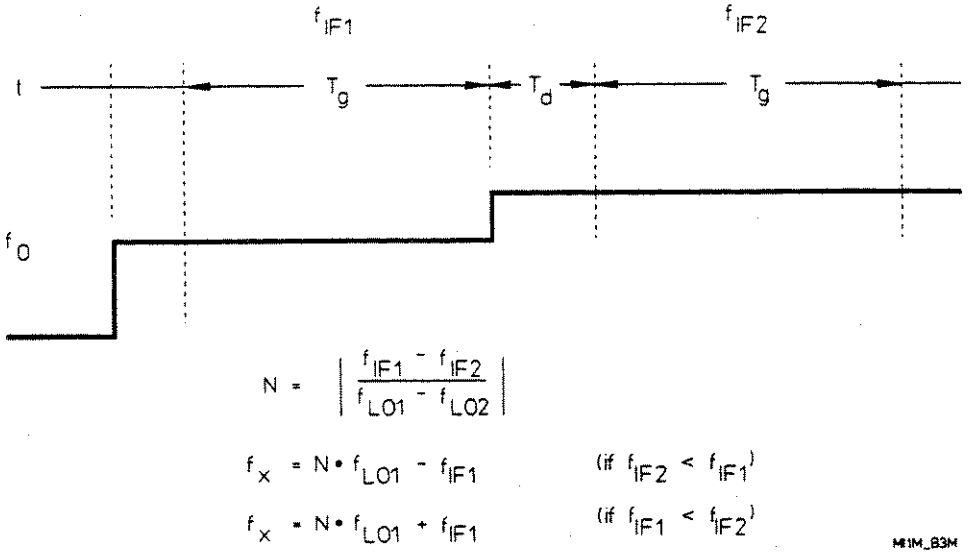


Figure 5-6. INPUT 1 Measurement Timing Diagram

The local oscillator (LO) is swept across the band until the input signal is found. At this point, there is a short delay for the LO to stabilize. Now the first measurement f_{IF1} is taken during gate time t_g. The LO frequency is now offset by Δf_{LO} during t_d. The dead time t_d must be long enough for the LO to stabilize. After this the second measurement f_{IF2} is taken during gate time t_g.

If the input signal has FM with peak deviation Δf_x at a rate f, we could have a maximum error in harmonic number ΔN given by:

$$\Delta N = \frac{\Delta f_x}{\Delta f_{LO}} \cdot 2 \sin \pi f(t_g + t_d) \cdot \left(\frac{\sin \pi f t_g}{\pi f t_g} \right)$$

where Δf_{LO} = LO frequency offset = $f_{LO1} - f_{LO2}$
Δf_x = peak frequency deviation of input signal
f = rate by which the input signal is frequency modulated
t_d = time interval between the two consecutive measurements
t_g = gate time

As long as ΔN is less than 0.5, the correct N can be computed. However, ΔN is selected to be less than 0.3. Using the formula above, the computed values for t_g, t_d, and f_{LO} tolerate a maximum peak deviation Δf_x of 10 MHz down to a minimum FM rate of 1 kHz or 45 Hz, which is selectable using the **FM Rate Tolerance** function of the HP 5361B. When measuring signals with an FM rate lower than 1 kHz, a longer gate time is used to permit the correct computation of N at the lower rate.

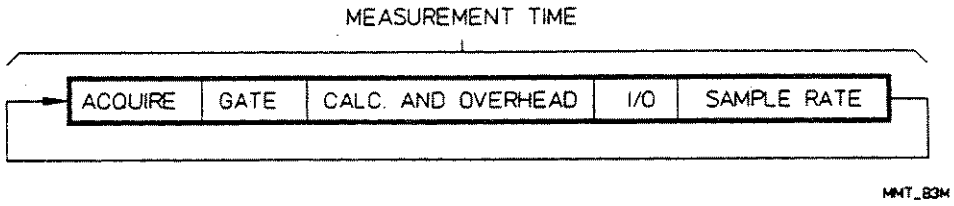
5-52. SENSITIVITY

The limiting factors in determining the sensitivity of the HP 5361B are the effective noise bandwidth of the IF, and the conversion efficiency of the sampler. The noise bandwidth of the IF determines the noise power, and the sampler conversion efficiency determines the IF signal power (for a fixed input power). The IF signal-to-noise ratio must be kept at a value which insures that there are no noise induced errors in counting the IF signal at the minimum signal input level.

The microprocessor detects two parameters: the first is the output from the IF detector, which is true if the IF signal is in the range of 35 MHz to 105 MHz and the counter input power level is greater than approximately –30 dBm; the other parameter is from the internal counter, which is true if the IF frequency is in the range of 45 MHz to 95 MHz. Both parameters have to be true for a measurement to be valid. Thus, information from the IF detector insures that the input signal is sufficiently large to produce an IF with an acceptable signal-to-noise ratio, and that the highest IF frequency is low enough to be correctly counted. The 45 MHz to 95 MHz IF information is used to center the IF in the range of 45 MHz to 95 MHz to achieve the specified FM tolerance.

5-53. MEASUREMENT TIME

The rate at which complete measurements can be made is called "measurement time." Measurement time consists of acquisition time, gate time, calculation and overhead time, I/O (display and HP-IB) time, and sample rate time, as shown below:



Measurement time tells how quickly results can be obtained from a counter. Acquisition time is the time necessary for a counter to configure its circuitry to measure a signal (that is, the time to determine the harmonic number). Gate time is the time in which the actual measurement takes place. Note that there is no acquisition time for INPUT 2 measurements as these go directly into the counting circuit.

In Auto mode, acquisition time is comprised of a local oscillator sweep to set the LO to its proper value, plus harmonic number and sideband determination. In Manual mode, acquisition time is calculation time for the LO frequency, harmonic number, and sideband, plus time to allow the LO to be programmed and to settle.

Gate time is a function of the resolution setting. A resolution of 1 Hz denotes a maximum gate time of 1 second. For 1MΩ (INPUT 2) measurements, the High Resolution function may be selected to give a resolution up to 0.001 Hz with a 1 second gate time.

Calculation and Overhead time, and I/O time are dead times during which the microprocessor formats and outputs the results of the latest measurement to the display and the HP-IB.

Sample rate time is a method for controlling the display update rate. Sample rates for the HP 5361B vary from Fast (allowing the counter to count as frequently as possible) to Hold (allowing the counter to retain the value of the last measurement until the next measurement is triggered). Intermediate sample rate values range from 0.5 seconds to 10 seconds.

Measurement times for local and remote measurements are the same. Harmonic number determination during a local or remote measurement is done once during each measurement.

5-54. HP 5361B BLOCK DIAGRAM DESCRIPTION

Figure 5-15 is a block diagram of the HP 5361B Pulse/CW Microwave Frequency Counter showing all the assemblies of the instrument. The seven major sections are: the low frequency input section, the microwave section, the synthesizer section, the IF amplifier/detector section, the gating section, the counter section, and the control section. Auxiliary sections include: the front panel keyboard/display section, the timebase/timebase buffer section, the power supply section, and the HP-IB interface section. Most of these sections are made up of single-board circuits, except the front panel keyboard/display section (A7 and A9 assemblies), the power supply section (A8 and part of A1 assemblies), and the timebase/timebase buffer section (A8 and part of A1 assemblies). Each section is briefly discussed in the following paragraphs. (A component level description of each board assembly is given in the Detailed Circuit Descriptions, beginning at Section 5-133.)

5-55. Low Frequency Input Section (A2 Assembly)

The A2 Low Frequency Input Assembly accepts signals below 525 MHz. The signals are preconditioned and then sent to the counter section. There are two input settings: a prescaled 50Ω input from 10 MHz to 525 MHz and a direct count 1 MΩ input from 10 Hz to 80 MHz. The input signal is applied through a fused BNC connector on the front panel and switched either to the 1 MΩ or the 50Ω path by pressing the appropriate front panel key next to the input connector. The low frequency output multiplexer on the A2 Assembly is controlled by the A4 Microprocessor Assembly. The low frequency signal is routed to the Channel C input of the MRC (Multiple Register Counter) on the A3 Counter Assembly.

During the time the main gate on the A3 Assembly is enabled from the A4 microprocessor, events pass through the main gate to Channel C of the MRC where they are totalized. At the conclusion of the gate time, the microprocessor reads the contents of the counter and computes the input frequency. A 35 MHz test signal is routed from the A5 Synthesizer Assembly to the A2 Low Frequency Input Assembly for diagnostic and self test purposes. When the test signal is in operation, the initial gain stages of the A2 Assembly are turned off by the A4 Assembly.

5-56. Microwave Section (A12 Assembly/U1 Sampler)

The basic function of the microwave section (Microwave Module, which includes the A12 Microwave Assembly and U1 Sampler) in the HP 5361B is to perform the down-conversion of microwave signals in the 500 MHz to 20 GHz (26.5 GHz for HP 5361B/Option 026; 40 GHz for HP 5361B/Option 040) region to the intermediate frequency (IF) region of the counter. (The resultant 35 to 105 MHz IF signal can then be detected and amplified by the A6 IF Amplifier/Detector Assembly, gated by the A14 Gate Board Assembly, and counted by the A3 Counter Assembly.) To perform its function, the Microwave Module requires a high power local oscillator (LO) signal from the A5 Synthesizer Assembly.

The Microwave Module can be divided into three sections: the sampler driver, sampler, and the IF preamplifier. The sampler driver is a medium power, class B power amplifier which accepts the +14 dBm LO signal from the A5 Assembly via a coaxial cable. The signal is amplified by +11 dB, and sent to the sampler.

The U1 Sampler is the heart of the down-conversion system. The sampler driver signal drives a step-recovery diode (SRD) in the sampler to produce a very narrow voltage pulse. This pulse is used to control the sampling of the microwave signal entering the sampler RF connector (via the front panel INPUT 1 connector). When a harmonic of the LO sampling frequency is close to the microwave input signal frequency, a signal within the IF bandwidth results, and is sent to the IF preamplifier. A high-pass filter in front of the sampler eliminates low frequency signals that may be present on the microwave signal. This high-pass filter is internal to U1.

The IF preamplifier performs several functions, including: IF signal amplification, controlling dc bias current for the U1 Sampler, impedance matching, and isolating the IF from the LO feedthrough signal and its harmonics. The IF signal passes through matching, filter, and frequency compensation networks, and is amplified +32 dB before it is sent to the A6 Assembly.

5-57. IF Amplifier/Detector Section (A6 Assembly)

The main functions of the IF Amplifier/Detector section are to amplify, filter, and detect specific information from the IF signal that arrives from the A12 Microwave Module. The resulting signal(s) are passed on to the gating section. The A6 assembly also generates several status/warning/support lines needed by the microprocessor, gating, and counter sections.

The IF section is essential to provide both the type of signals required by the gating section and their proper levels. Three important signals are output by the IF section to the gating section: IF event complementary (±), envelope, and IF inband. The first two signals relay the actual information of the microwave carrier and pulse envelope parameters, respectively. The third signal tells the gating section when the IF signal is between 35 - 105 MHz. This information is used to ensure that the gating and counter sections always make valid measurements.

Other signals output from the IF section to the microprocessor include: NO_IF_LCH, MODE_LCH, INBAND_LCH, PULSE_PRSNT_LCH, IF_PRESENT, and OVLD. The NEW_IF_MON signal is routed via A3 to the rear panel IF Out connector. Additional auxiliary/control inputs include: IF_TEST, AUXA, IF_OFF, LOW_PRF, and IF_BD_RST.

Three stages of amplification provide 43 dB of IF gain prior to the Schmitt trigger, peak detector inputs, and rear panel IF output. Correct passband is ensured through the use of the 7-pole 175 MHz and the 4-pole 200 MHz IF filters. Automatic gain control (AGC) is performed via the peak detector, sample and hold, AGC loop reference, integrator, and attenuator circuits. The Schmitt trigger, and envelope detector/comparator circuits convert the IF into signals useful for the gating and counter sections. An Inband 35-105 MHz detector circuit detects when the IF signal is between 35-105 MHz. Other circuits are present on the IF section that provide status and warning information to the microprocessor including: overload comparator, IF present comparator, and status latch.

5-58. Synthesizer Section (A5 Assembly)

The A5 Synthesizer Assembly provides the 294.5 to 350.0 MHz local oscillator (LO) signal to the A12 Microwave Module. The LO frequency is programmed by the A4 Microprocessor Assembly and is referenced to the 10 MHz timebase signal. The synthesizer circuit is based on a single phase-lock loop (PLL), which allows the high frequency wideband tuneable oscillator (VCO) in the synthesizer to have the same frequency accuracy and drift characteristics as the crystal oscillator timebase.

The 10 MHz signal from the timebase buffer is divided by 100 to obtain a 100 kHz reference for the phase-locked loop. A voltage controlled oscillator (VCO) frequency is divided by the programmable frequency dividers which are controlled by the A4 Microprocessor. The dividers output is compared to a 100 kHz reference in a phase detector. The phase detector output is integrated and filtered, and used to control the frequency of the VCO, forming a closed-loop negative feedback system. The feedback adjusts the VCO frequency such that the output of the programmable dividers is to equal the 100 kHz reference. Thus, the VCO frequency will always be a programmable multiple of 100 kHz.

The VCO output signal is amplified to +14 dBm (minimum) and sent to the Microwave Module via a coaxial cable. A 35 MHz auxiliary output signal from the frequency dividers is sent to the counter, IF amplifier/detector, and low frequency boards for diagnostic and self test procedures. This auxiliary output is turned off during normal operation of the instrument.

5-59. Gating Section (A14 Assembly)

The main function of the A14 Gate Board Assembly is to provide the A3 Counter Assembly with a gating or arming signal. This signal enables the counter section to correctly count the IF of a microwave pulse burst or continuous wave (CW) signal. All timing signals required for INPUT 1 measurements pass through the A14 Gate Board Assembly.

The gating section functions differently for pulse and CW measurements. During CW measurements, the A14 Gate Board Assembly (or gating section) divides the IF signal from the A6 IF Assembly by two before sending it it to the counter section. The A4 microprocessor generated gate signal also passes through the gating section to the counter section. During

pulse measurements, the gating section decides when and where the measurement is made within a pulse. It also determines how long the gate must remain open during a measurement. The gating section along with the counter section ensures that only valid measurements are made. These sections also function with each other to reduce the rate at which measurements occur so that the counter section and A4 microprocessor can correctly process the information gathered during the measurement.

The gating section has nine inputs and five outputs. The inputs include: +IF_NEW, -IF_NEW, ENVELOPE_DET, and L_IF_INBAND arriving from the from the A6 IF Assembly; DATA BUS, CONTROL, and H_GATE arriving from the A4 Microprocessor Assembly; EXT_GATE_ARM arriving via the front panel GATE/ARM IN connector; and L_HOLDOFF arriving from the A3 Counter Assembly. The outputs are: EVENTS, ARM_MRC (H_GATE), and ENVELOPE_CTR routed to A3 Counter Assembly; ENVELOPE_OUT routed to the rear panel PULSE OUT connector; and GATE+IF routed to the front panel SCOPE-VIEW connector.

The gating section consists of four main blocks: Microprocessor Interface, Gate/Event Generation, Event Counter/Width Generator, and Gating/Arming as shown on Sheet 1 of *Figure 5-15*.

The Microprocessor Interface block enables the A14 Gate Board Assembly to communicate with the A4 microprocessor. This interface allows the gating section to be programmed for the different measurement modes such as CW or pulse, envelope measurements, and internal or external gate.

The Gate/Event Generation block generates the gate synchronous with the incoming IF signal. The timing of these two signals is critical for the counter's measurement process. During internal gate mode, the gate generation block opens the gate synchronous with the second IF pulse and closes the gate when signalled by the event counting block. In external gate mode, it opens and closes the gate with the external gate signal synchronized to the IF pulses.

The Event Counter/Width Generator block performs two functions. During the External gate mode, the circuit counts the number of events while the gate is open. During Internal gate mode, it generates a signal to close the gate after counting a preprogrammed number of events. After closing the gate, these counters are preloaded for the next pulse.

The Gating and Arming block performs three functions. First, it prevents the gate generation logic from making a measurement until other conditions on the gating and counting sections are correctly synchronized. Second, it monitors the status of all gating section fault lines. And third, it controls the ENVELOPE signal routed to the counter section. The ENVELOPE signal is enabled only for OFFTIME, PRI, PRF, and PW measurements. For pulsed frequency measurements, the ENVELOPE signal is disabled.

5-60. Counter Section (A3 Assembly)

The Counter section contains an input switch circuit for the IF signals, a MRC (Multiple Register Counter), a phase shifter circuit, an interpolator circuit, and a counter circuit. The MRC is clocked by the 10 MHz signal coming from the timebase buffer circuit on the A1 Assembly. The MRC Channel A input counts either the envelope or events signal from the A14 Gate Board Assembly, Channel B counts the 35 MHz test signal from the A5 Synthesizer Assembly, and Channel C counts the low frequency signals. Channel selection and all other MRC setups, and the interpolator circuit are controlled by the A4 Microprocessor Assembly.

The general operation of the counter section centers on the interaction between the A14 Gate Board, the A4 microprocessor, and the Input Switch and MRC circuits of the A3 Counter. The MRC (Multiple Register Counter) is an LSI bipolar IC. It is a programmable universal counter-on-a-chip, containing four sets of registers: Events, Time, Status and Control. The E (Events) and T (Time) registers collect the raw input measurement data. The S (Status) register includes E and T register overflow flags and information on the state of the measurement. The C (Control) register, directed by the microprocessor, sets up the various measurement modes of the MRC, and resets the counters, synchronizers, and overflow flags.

For all CW measurements, the microprocessor uses the accumulated Events and Time data directly, calculating the measured frequency by dividing the contents of the Events register by the contents of the Time register. Pulse envelope measurements also use E and T MRC register data. For pulsed frequency measurements, IF frequency data is read from the T register while E register data arrives from the gating section. The measurement gate time is controlled by the gating section and microprocessor.

For increased measurement resolution, the interpolator circuit measures the uncertainty introduced by the time difference between the actual input events and the opening and closing of the counting gate. The MRC detects the slight error factor, and provides start and stop pulses to the interpolator circuit. The interpolator circuit measures the error factor and sends the data to the microprocessor, which then uses the interpolator data in the measurement calculations to compensate for the uncertainty.

5-61. Microprocessor Section (A4 Assembly)

The HP 5361B's CPU is designed around an MC6803 8-bit microprocessor, using a memory-mapped architecture. An 8-bit bidirectional data bus is used to control and monitor various circuits and assemblies within the instrument. The microprocessor controls the display, reads the keyboard, and receives a signal from a detector on the timebase buffer to indicate if an internal or external source is present and if an ovenized crystal oscillator has reached operating temperature.

The processor programs the gating section, controls the MRC's gate, sets the MRC control registers, and reads the data over the data bus. Overload, acquisition, and guardband signals come to the processor from the IF section, after which the dividers on the synthesizer are

programmed and implemented by a strobe signal. The processor also controls the signal path on the low frequency board. The A4 microprocessor interacts with the processor on the HP-IB interface board, which controls all communication over the HP-IB.

The A4 assembly contains one 8K byte RAM IC and one 64K byte ROM IC. When the counter is in the standby mode, a +5V standby RAM supply for the microprocessor will stay on, and the instrument's programmed front panel/HP-IB settings and HP-IB address will be retained in the processor's internal RAM as long as ac power is connected to the instrument.

Since the processor is the center of the instrument, any failure or inconsistency on its part would greatly influence the instrument's performance. The processor assembly has several levels of diagnostics available for testing and servicing.

5-62. Keyboard/Display Section (A7 and A9 Assemblies)

The keyboard/display section consists of the A7 Keyboard/Display Logic Assembly and the A9 Display/Driver Assembly. The A7 Assembly contains a 20-key keyboard matrix circuit, and encoding and interface circuitry for sending front panel entry data to the A4 microprocessor. The A7 Assembly also contains the display logic and interface circuitry for receiving and displaying data from the processor. All data flow to and from the A7 Assembly occurs over five data bus lines, and three control lines from the microprocessor. The A7 Assembly also contains the front panel POWER switch circuit; when the POWER switch is set to STBY, the instrument settings are saved and the optional oven oscillator timebase, if present, is kept warm.

The display consists of a 24-character Liquid Crystal Display, (LCD) backlit by LEDs within the A9 Assembly to provide increased contrast for improved viewing. The LCD displays all measurement information alphanumerically, and can be programmed via the HP-IB to display messages.

5-63. Timebase/Timebase Buffer Section (A8 and part of A1 Assemblies)

The instrument's standard oscillator is a Temperature Compensated Crystal Oscillator (TCXO). The counter may also be equipped with one of two types of optional timebases: an oven oscillator providing an improved aging rate over that of the standard TCXO, and a high stability oven oscillator providing a greatly improved aging rate allowing increased calibration periods of up to five years. Both the standard TCXO and optional oven oscillators provide a 10 MHz timebase reference frequency to the Timebase Buffer circuit (part of the A1 Timebase Buffer/Power Supply Control Assembly).

The Timebase Buffer on the A1 Assembly has four main output signals. The 10 MHz main signal goes to the A3 Counter and A5 Synthesizer Assemblies. Two rear panel outputs, 10 MHz and 1 MHz, are available for monitoring. When the instrument is in Standby, the 10 MHz and 1 MHz signals will still be available at the rear panel outputs, but not in the instrument.

The rear panel has an input for a 1, 2, 5, or 10 MHz external reference signal. A detection circuit on the A1 assembly will detect if an external reference source is being used for the timebase, and send a signal to the microprocessor, which will indicate through a display annunciator that an external source is being used. The instrument will automatically switch from the internal oscillator to the external reference. The display will also indicate when an ovenized oscillator (if present) is still cold.

The Timebase Buffer circuit also includes regulators for providing voltage supplies to both the standard and optional timebase oscillators, and a Standby voltage for the A4 microprocessor's internal RAM.

5-64. Power Supply Section (A8 and part of A1 Assemblies)

The power supply circuitry consists of the chassis-mounted power module and transformer, rectifying and series pass components on the A8 Motherboard/Power Supply Regulator Assembly, and current and voltage sense circuits on the Power Supply Control portion of the A1 Assembly. The A8 circuit produces regulated +15, +5, and –5.2 volt supplies for all instrument assemblies, as well as special purpose supplies for the HP-IB interface (+5V), Microwave Module (+5V,+13V), and the oven oscillator and synthesizer boards (–24V). Voltage and current sense lines go to the A1 circuitry, which in turn send voltage drive lines to the A8 circuitry to regulate the supplies. Unregulated +15 and +5 volts are also sent to the Timebase Buffer circuit for regulation.

5-65. HP-IB Interface Section (A11 Assembly)

The A11 Assembly controls all HP-IB interfacing between the HP 5361B and an external controller, allowing the counter to be remotely programmed to perform almost all functions normally available via the front panel keyboard. The interface partially decodes commands from the controller and sends them to the A4 microprocessor, and formats output data from the processor to send to the controller. The A11 Assembly contains a seven-position switch for manual selection of the HP 5361B HP-IB address; the address is also selectable via the front panel keyboard.

5-66. DESCRIPTION OF USER-CALLABLE DIAGNOSTICS/EXTENDED FUNCTIONS

5-67. Introduction

The HP 5361B is a microprocessor-based system with a total of 59 built-in diagnostics tests and extended functions. These diagnostics can be used as an aid in testing and troubleshooting the instrument by identifying faulty assemblies. All of the diagnostics are available via the front panel and, in most cases, over the HP-IB.

There are three types of diagnostics:

1. Power-Up Self Test: A sequence of tests **automatically executed** on power-up. These tests include subsets of the user-callable diagnostics. (Refer to Section 5-27.)

2. User-Callable Diagnostics: Individual tests which can be initiated manually or via the HP-IB. (Refer to list in *Table 5-12.*)

3. Self Check: A sequence of tests executed by pressing the **Self Check/Cal** key on the front panel. These tests are a subset of the user-callable diagnostics. (Refer to Section 5-28.)

   The diagnostic routines are designed to isolate faults in the HP 5361B to the assembly level. In any given failure mode, the assembly that is found faulty by appropriate use of the diagnostics is the most probable cause of the failure. It is still possible that the fault lies elsewhere in the instrument, but using the diagnostics can quickly provide an appropriate starting point for component level troubleshooting.

   The user-callable diagnostics consist of tests which can be called individually, while the Power-Up diagnostics execute a sequence of tests. Most of the diagnostics will display a message indicating whether the test passed or failed, and in remote operation the pass/fail result can be retrieved over the HP-IB. A few diagnostics may require an oscilloscope, spectrum analyzer or other equipment to obtain desired service information. The individual description for each diagnostic will list any required equipment. Refer to *Table B-1,* Recommended Test Equipment, in Appendix B for test equipment specifications.

   The following paragraphs provide descriptions of each diagnostic and extended function available in the HP 5361B. For complete information on how to use the diagnostic routines, refer to the paragraphs listed below:

a. Instructions for accessing the diagnostics via the front panel:

Section 5-70, Diagnostics Mode Entry (Keyboard versus HP-IB).
Section 5-71, Diagnostics Mode Exit and Special Conditions.
Section 5-72, Invalid Diagnostic Numbers.

b. Information for calling diagnostics over HP-IB:

Section 5-70, Diagnostic Mode Entry (Keyboard vesus HP-IB).
Section 4, Remote Operation Via HP-IB in the Operating and Programming Manual.

c. Troubleshooting procedures using diagnostics:

Section 5-19, Overall Troubleshooting.
Sections 5-29 through 5-41, Individual Assembly Troubleshooting.

5-68. User-Callable Diagnostics and Extended Functions

Table 5-12 is a complete list of the user-callable diagnostics (DIAG) and extended functions (EFUN) by number, and includes the DIAG or EFUN name, the assembly (or assemblies) being tested, and the section number where a description of the given DIAG or EFUN can be found. Each user-callable diagnostic or extended function can be executed as an individual test or function.

Table 5-12. User-Callable Diagnostics and Extended Functions

DIAG/EFUN NO.	NAME	ASSEMBLY TESTED	SECTION NO.
1	Self Test	A1, A2, A3, A4 ,A5, A6	5-73
2	Display IF	Extended Function	5-74
3	Display MRC E & T Register Contents	Extended Function	5-75
4	Display LO Frequency	Extended Function	5-76
5	Display N (integer) and Sideband	Extended Function	5-77
6	Display N (fraction) and Sideband	Extended Function	5-78
7	Display Interpolator Short Calibration	Extended Function	5-79
8	Display Interpolator Long Calibration	Extended Function	5-80
9	Display Interpolator Measurement	Extended Function	5-81
*10	Timebase Verification	A1 Timebase/Timebase Buffer Block	5-82
*11	Power Supply Verification	A1 Power Supply Block	5-84

* These Extended Functions are primarily diagnostic in nature.

Table 5-12. User-Callable Diagnostics and Extended Functions (Continued)

DIAG/EFUN NO.	NAME	ASSEMBLY TESTED	SECTION NO.
*20	Low Frequency 50 Ohm Verification: 35 MHz	A2 Low Frequency Input	5-84
*21	Low Frequency 1M Ohm Verification: 35 MHz	A2 Low Frequency Input	5-85
*30	MRC CH A Verification: 10 MHz Timebase	A3 Counter	5-86
*31	MRC CH B Verification: 35 MHz	A3 Counter	5-87
*32	Interpolator Check	A3 Counter	5-88
33	Display MRC E & T Register Contents for Pulse Measurements	Extended Functhon	5-89
34	Display Gate Bias Error	Extended Function	5-90
40	Display ROM Version Number	Extended Function	5-91
*41	RAM Test	A4 Microprocessor	5-92
*42	ROM Test	A4 Microprocessor	5-93
*43	Repeated Reset	A4 Microprocessor	5-94
*50	LO Verification 29.5 MHz, 35.0 MHz	A5 Synthesizer	5-95
51	LO Verification User-Entered Frequency	A5 Synthesizer	5-96
*52	LO Sweep 275.0 > 375.0 MHz	A5 Synthesizer	5-97
*53	LO Lower/Upper Frequency Bounds	A5 Synthesizer	5-98
54	Gate Bias Calibration	Extended Function	5-99
*60	IF Verification: 35 MHz; Disable INPUT 1 and IF	A6 IF Amplifier/Detector	5-100
*61	Check Level Detector	A6 IF Amplifier/Detector	5-101
62	Disable Hardware and Software IF Detector Flags: Display Measurement	Extended Function	5-102
63	Disable Hardware and Software IF Detector Flags; Display IF	Extended Function	5-103
64	Disable Software IF Detector Flag; Display IF	Extended Function	5-104
*65	IF Verification: 35 MHz; Disable INPUT 1	A6 IF Amplifier/Detector	5-105
66	Display IF Function Status Indicators	Extended Function	5-106
67	Display IF Detector: Display IF Function Status Indicators	Extended Function	5-107
68	Display Narrow Pulse Harmonic Numbers	Extended Function	5-108

* These Extended Functions are primarily diagnostic in nature.

Table 5-12. User-Callable Diagnostics and Extended Functions (Continued)

DIAG/EFUN NO.	NAME	ASSEMBLY TESTED	SECTION NO.
*70	Keyboard Test	Keyboard/Display Logic (Part of A1)	5-109
*71	Display Test (flash on/off)	Keyboard/Display Logic (Part of A1)	5-110
**72	Set Printer Option	Extended Function	5-111
73	Set PRT OPT	(non-operative function; reserved for future printer support)	5-112
*80	HP-IB Verification	A11 HP-IB Interface	5-113
**81	Set Start Time for Profiling	Extended Function	5-114
**82	Set Stop Time for Profilling	Extended Function	5-115
**83	Set Fine or Coarse Data for Profiling	Extended Function	5-116
**84	Set Profiling Output Printer Options	Extended Function	5-117
**85	Set Filter On/Off for Profiling Output	Extended Function	5-118
**86	Enter ID Prefix for Profiling Printer Output Plot	Extended Function	5-119
**87	Set Number of Data Points (Steps) or Frequency Profile	Extended Function	5-120
**88	Set Start IF Cycle for Frequency Profile	Extended Function	5-121
**89	Set Number of IF Cycles Per Step for Profile	Extended Function	5-122
90	Set Gate Width in Time	Extended Function	5-123
91	Set Number of Averages Frequency Measurement	Extended Function	5-124
92	Force Pulse or CW Measurement Mode	Extended Function	5-125
93	Enter <100 ns Pulse Mode	Extended Function	5-126
94	High Resolution (INPUT 1 PRF/INPUT 2, 1 MOHM)	Extended Function	5-127
95	Set Gate Width by Number of IF Events or Cycles	Extended Function	5-128
96	Enter Chirp Mode	Extended Function	5-129
97	Set IF for Manual Center Frequency	Extended Function	5-130
98	Keyboard Lockout	Extended Function	5-131
99	Display Lockout	Extended Function	5-132

* These Extended Functions are primarily diagnositc in nature.

** These Extended Functions are available only for the HP 5361B counter.

Diagnostic 1 is a test routine that runs the Power-Up Seft Test (refer to Section 5-27). DIAG 2 through DIAG 9 are Extended Functions which can be used to display various components of the input frequency measurement. DIAG 80 is actually an HP-IB verification of the A11 HP-IB Interface Assembly.

Extended Functions 98 and 99 are not tests, but they are instead special operating conditions of the HP 5361B.

While diagnostics may be individually called from the front panel, they are best used in particular combinations and sequences to obtain the maximum amount of testing and troubleshooting information.

The diagnostic descriptions in this section include examples of the PASS/FAIL messages which will appear on the display for a given test. In these message examples, a letter (x or y) is used to represent an unknown digit. Unknown digits may appear in the display when an erroneous frequency is being measured or an unpredictable value is being displayed. For example, if a test which is supposed to measure (and display) 10 MHz should fail, the displayed frequency will be represented in this manual by: xx xxx xxx.

5-69. Level (LVL) Display

NOTE

The terms "diagnostic" and "extended function" are the same when used for troubleshooting purposes; thus, the term diagnostic, which is more appropriate for troubleshooting, is used throughout this service section when feasible. Hence, the "F" or "FUNC" appearing in the display stands for diagnostic throughout this service section.

The "LVL" warning may appear in the diagnostic display during an overload (high input signal) conditon, or during the IF AGC settling time while the counter is in the diagnostic mode. For most diagnostics, the LVL will appear in the right-hand message side of the display, overriding the assembly number or the word "FUNC" in the display. For example, an overload during DIAG 41 (RAM Test) would cause the letters "LVL" to appear in place of the normal "A4 F" in the display, as shown below:

PASS RAM LVL 41

A few diagnostics display the LVL warning toward the left of the display, or give no overload indication. The diagnostic displays shown in the following paragraphs will include an example of an OVLD display just beneath the standard display for the given diagnostic. For example, the set of display examples for DIAG 41 is shown in this manual as follows:

```
PASS RAM    FUNC41
FAIL RAM    FUNC41
PASS RAM    LVL  41
```

A few diagnostics may display alternate formats for a given Pass or Fail message. Any alternate characters in a display will be shown in a manner similar to the overload example above. Note that the words "PASS" or "FAIL" will always appear in the same location in the display.

5-70. Diagnostic Mode Entry (Keyboard Versus HP-IB)

CALLING DIAGNOSTICS VIA KEYBOARD. The diagnostics mode may be entered by pressing the front panel **Extended Function** key once. After the key is pressed, the HP 5361B will carry out the current diagnostic routine. The current diagnostic will be that which was last entered by the user, or if the HP 5361B has just been turned on, the diagnostic will default to Diagnostic 1 (Self Test – Front Panel only).

The diagnostic mode may also be entered by using the parameter entry mode, which allows you to change the diagnostic number. A new diagnostic number (from 1 to 99) may be entered using the following key sequence:

Set/Enter,
Extended Function,
digit(s) (Function/Data keys),
Set/Enter

For example, to enter the diagnostic mode and set Diagnostic 32 (Interpolator Check, A3 Counter assembly), press the following key sequence:

Set/Enter
Extended Function
3
2
Set/Enter

The HP 5361B display contents will depend on the diagnostic in progress. Most of the diagnostic displays will show "FUNC XX" or "F XX" in the message portion on the right-hand side of the display (where XX represents a diagnostic number from 01 to 99). Most displays will also include the assembly number, preceded by the letter "A", just to the left of the diagnostic number. For example, the DIAG 60 display will show "A6" just to the left of "F 60".

Once the diagnostic mode is entered, the diagnostic number may be changed by using the key sequence described previously, or by pressing the **INC** (increment) or **DEC** (decrement) key to move through the list of diagnostics in numberical order (exceptions: DIAG 98 and 99 cannot be entered using **INC** or **DEC** keys; once entered, DIAG 70 cannot be exited using the **INC** or **DEC** keys). If the diagnostic mode is entered by pressing the **Extended Function** key without using the **Set/Enter** key sequence, the last test number entered will be the diagnostic executed. When the HP 5361B is first powered on, the diagnostic mode faults to the following settings: DIAG 1,OFF.

CALLING DIAGNOSTICS VIA HP-IB. Most of the User-Callable Diagnostics available from the front panel are also available over the HP-IB using the EFUN, EFUNPARM, and EFUN? commands. Diagnostics are initiated over the HP-IB using the DIAG command. For example, the command "EFUN32,ON" will cause the HP 5361B to cycle through the Interpolator Check until the command "EFUN,OFF" or another diagnostic number is sent. Diagnostic results can be obtained over the HP-IB by using the EFUN? command. The EFUNPARM command is used only with DIAG 51 to allow you to enter a frequency parameter for local oscillator verification. Refer to Section 4, Remote Operation via the HP-IB, for detailed information on use of the HP-IB. (Section 4 is in the Operating and Programming Manual.)

There are five diagnostics not available over the HP-IB, because they may erase needed memory or reset hardware. The diagnostics not available are as follows:

DIAG 1: Self Test
DIAG 41: RAM Test
DIAG 42: ROM Test
DIAG 43: Repeated Reset
DIAG 80: HP-IB Verification

5-71. Diagnostics Mode Exit and Special Conditions

For most diagnostics, the diagnostics mode can be exited by pressing **Extended Function** key a second time, or by pressing the **Reset/Local** key. There are some exceptions, however, in which the **Extended Function** key cannot be used to exit the mode because the key is used for otuer functions during the test. In these cases, pressing the **Reset/Local** key will exit the mode. Note that if the **Reset/Local** key is pressed to clear an "OUT OF RANGE 3 ERROR" (resulting from the entry of an invalid HP-IB address or Manual Center Frequency value), the error will be cleared and the diagnostic number will be exited at the same time.

There are also a few diagnostics which have special conditions attached to their use; for example, some diagnostics are not accessible via HP-IB as previously described in the paragraph titled "CALLING DIAGNOSTICS VIA HP-IB". *Table 5-5* lists these and other special conditions.

Pressing the increment or decrement keys will halt execution of the running diagnostic and move to the next one in sequence. Pressing the **Reset/Local** key halts execution of the current diagnostic, and returns to Diagnostic 1.

5-72. Invalid Diagnostic Numbers

If you attempt to enter an invalid diagnostic number, the HP 5361B will display the message: "NOT AVAILABLE FUNC XX", where XX represents the invalid number. The only exception is if 00 is entered as the diagnostic number, in which case the HP 5361B will automatically default to DIAG 1. If the **INC** or **DEC** key is being used to move through the list of diagnostics, the HP 5361B will display "NOT AVAILABLE" message until the next valid diagnostic in the sequence is reached.

NOTE

The terms "diagnostic" and "extended function" are the same when used for troubleshooting purposes; thus, the term diagnostic, which is more appropriate for troubleshooting, is used instead throughout this service section. Hence, the "F" or "FUNC" appearing in the diagnostic display stands for diagnostic throughout this service section.

5-73. Diagnostic 1: Self Test

Effect: Enables a particular sequence of diagnostic extended functions to test the measurement circuits of the counter. This function performs the same sequence of tests as the front panel Self Check function, but stays in a loop, repeating the test sequence until the extended function mode is exited or another function called. The tests are arranged so that each routine involves only one untested assembly. The test routines and the order in which they occur are listed in *Table 5-13*.

Table 5-13. DIAG 1 Self Test Sequence

DIAG NUMBER	TEST	ASSEMBLY TESTED
DIAG 11	Power Supply Verification	A1/A8
DIAG 10	Timebase Verification	A1
DIAG 30	MRC CH A Verification: 10 MHz Timebase	A3
DIAG 50	LO Verification: 29.5 MHz, 35.0 MHz	A5
DIAG 31	MRC CH B Verification: 35 MHz	A3
DIAG 60	IF Verification: 35 MHz, Disable INPUT 1 and IF	A6
DIAG 32	Interpolator Check	A3
DIAG 20	Low Frequency 50Ω Verification: 35 MHz	A2
DIAG 21	Low Frequency 1MΩ Verification: 35 MHz	A2
DIAG 54	Gate Bias Calibration	A14

NOTE

Diagnostic 1 (EFUN 1) is not available over the HP-IB.

If the counter passes DIAG 1, the messages are:

```
PASS  35   000    0**     F      01
PASS  35   000    0**     LVL    01
```

If a failure should occur, the counter displays the number of the failed diagnostic, and the assembly involved. For example, if the DIAG 21 Direct Count test failed during DIAG 1, the display would be:

```
FAIL   nn   nnn   nnn   A2    F   01
```

The failure display formats for DIAG 11, 10, or 32 are exceptions to the format shown above. The possible messages are:

```
FAIL  POWER      A1   F 11
FAIL  TIMEBASE   A1   F 10
FAIL  INTERPOL   A3   F 32
```

If you exit the extended function or diagnostic mode during DIAG 1, the diagnostic number remains at 1, regardless of whether the function passed or failed. For example, if the counter failed DIAG 31 during DIAG 1 and you exited the extended function mode, the test number stored will be 1. The next time the **Extended Function** key is pressed (to re-enter the extended function mode), the counter returns to DIAG 1, which (in this example) would again fail at DIAG 31.

5-74. Diagnostic 2: Display IF

Effect: The counter displays the value of the IF, showing one digit greater than the chosen resolution (two digits for 1 Hz). The chosen resolution and sample rate affect the display, and also the Smooth function, if enabled. The IF is displayed only when the counter is set to INPUT 1; when set to INPUT 2, the counter displays the low frequency measurement. The IF display will be in the format shown below (assuming an IF of 75 MHz, and a chosen resolution of 1 Hz):

```
IF     75  000  000  .nn  F 02
LVL    75  000  000  .nn  F 02
```

5-75. Diagnostic 3: Display MRC E and T Register Contents

Effect: The counter displays the contents of the MRC Events (E) and Time (T) registers, including overflow. The chosen resolution affects the contents of the Time register (gate time), but the selected sample rate does not affect register contents. Math functions, if enabled, also have no effect. The gate time equals the T register value multiplied by 100 ns. The T register portion of the display includes the fraction (in decimal form) calculated from the interpolator data. For CW measurements, the E register contains the number of IF cycles (INPUT 1) or total zero crossings (INPUT 2). The T register contains the gate time during which the E events were counted. For pulse frequency measurements, the E register contains the number of averages set by the user or default while the T register contains the total gate time of all averaged measurements. The messages are:

```
E    10019713  T  2003937   .28
E    10019713  T  2003      LVL
```

5-76. Diagnostic 4: Display LO (Synthesizer) Frequency

Effect: Displays the current value of the LO frequency. In Auto mode, the LO value is displayed only when a measurement is in progress, not during signal acquisition or LO sweep. In Manual mode, the display of the LO value is stable. If the counter is switched to INPUT 2, the LO value will be 0.0. The messages are:

```
LO   350.0 MHZ  FUNC  04
LO   350.0 MHZ  LVL   04
```

5-77. Diagnostic 5: Display Harmonic Number (Integer) and Sideband

Effect: Displays the value of the harmonic number (N), along with the sideband location of the input frequency (USB=upper sideband, LSB=lower sideband) with respect to N • LO. If the instrument is in Auto or Manual mode, the display only changes when a new harmonic number has been determined. When INPUT 2 is active, the harmonic number is 0, "USB" is displayed. The message display format is:

```
HARM  3  LSB  FUNC  05
HARM  3  LSB  LVL   05
```

5-78. Diagnostic 6: Harmonic Number (Fraction) and Sideband

Effect: Displays the value of the harmonic number (N) to .01 accuracy, along with the sideband information (refer to DIAG 5 description). When the counter is in Manual mode, the fractional value of N is the same as the integer value. This auxiliary function can be used to see if FM on the input signal is affecting the measurement. The message display format is:

```
HARM   2.99  LSB   FUNC  06
HARM   2.99  LSB   LVL   06
```

5-79. Diagnostic 7: Display Interpolator Short Calibration

Effect: The Interpolator Start and Stop counts are displayed for the short MRC calibration mode. The Start and Stop values should be within ±20 counts of each other, with a typical calibration count falling in the approximate range of 100-130. The Short calibration values should always be less than the values displayed by DIAG 8 (Interpolator Long Calibration). The message display format is:

```
SH   CAL   126  125  FUNC   07
SH   CAL   126  125  LVL    07
```

5-80. Diagnostic 8: Display Interpolator Long Calibration

Effect: The interpolator Start and Stop counts are displayed for the long MRC calibration mode. The Start and Stop values should be within ±20 counts of each other, with a typical calibration count falling in the approximate range of 290-310. The long calibration values should always be greater than the values displayed by DIAG 7 (Interpolator Short Calibration). The message display format is:

```
LONG  CAL  308  307  FUNC   08
LONG  CAL  308  307  LVL    08
```

5-81. Diagnostic 9: Display Interpolator Measurement

Effect: The Interpolator Start and Stop counts are displayed for the current measurement. The Start value (the three digits to the left) should fall within the range of the Start values displayed by the Short Calibration (DIAG 7) and Long Calibration (DIAG 8) functions described above. Similarly, the Stop value (the three digits to the right) should fall within the range of the Stop values displayed by DIAG 7 and DIAG 8. The message display format is:

```
MEAS   245   218   FUNC   09
MEAS   245   218   LVL    09
```

5-82. Diagnostic 10: Timebase Verification

Effect: Confirms the presence of either an external or internal time base reference frequency. A signal (L 10MHZ OK) from the Timebase Buffer circuit (on the A1 Timebase Buffer/Power Supply Control Assembly is sampled by the A4 microprocessor to determine if the timebase is operational. The display messages are:

```
PASS  TIMEBASE     A1  F  10
FAIL  TIMEBASE     A1  F  10
PASS  TIMEBASE     LVL    10
```

5-83. Diagnostic 11: Power Supply Verification

Effect: Verifies operation of the power supply circuits on A1. The Power Supply circuit (on the A1 Timebase Buffer/Power Supply Control Assembly) sends a signal (H PWRSP OK) to the A4 microprocessor to indicate that most of the power supplies are functioning. All supply voltages in the instrument (except +5V, and the +3V on the A3 Assembly) are checked only for their presence or absence, but are not checked for specified voltage levels. The messages are:

```
PASS  POWER    A1  F  11
FAIL  POWER    A1  F  11
PASS  POWER    LVL    11
```

5-84. Diagnostic 20: Low Frequency 50Ω Verfication: 35 MHz

Effect: Verifies the low frequency 50Ω measurement function. A 35 MHz test signal (AUX A/B) is provided by the A5 Synthesizer Assembly, derived by dividing the LO frequency (350 MHz) by 10. The A4 microprocessor switches this signal to the 50Ω input (INPUT 2) and the MRC counts the signal, verifying the frequency to ±100 Hz. This measurement is taken using a 100 ms gate time (with no interpolation). The messages are:

```
PASS   35   000   0**   A2  F  20
FAIL   nn   nnn   nnn   A2  F  20
PASS   35   000   0**   LVL    20
```

5-85. Diagnostic 21: Low Frequency 1 MΩ Verification: 35 MHz

Effect: Verifies the low frequency 1 MΩ measurement function. A 35 MHz test signal (AUX A/B) is provided by the A5 Synthesizer Assembly, derived by dividing the LO frequency (350 MHz) by 10. The A4 microprocessor switches this signal to the 1MΩ input (INPUT 2) and the MRC counts the signal, verifying the frequency to ±100 Hz. This measurement is taken using a 100 ms gate time (with no interpolation). The messages are:

PASS	35	000	0**	A2	F	21
FAIL	nn	nnn	nnn	A2	F	21
PASS	35	000	0**	LVL		21

5-86. Diagnostic 30: MRC Channel A Verification: 10 MHz Timebase

Effect: Verifies MRC Channel A. The microprocessor programs the MRC to count its own 10 MHz time base in both registers. The result is checked to ±100 Hz accuracy using a 100 ms gate time (with no interpolation). The messages are:

PASS	10	000	0**	A3	F	30
FAIL	nn	nnn	nnn	A3	F	30
PASS	10	000	0**	LVL		30

5-87. Diagnostic 31: MRC Channel B Verification: 35 MHz

Effect: Verifies MRC Channel B. The 35 MHz test signal (AUX A/B) available from the A5 Synthesizer Assembly is used to test Input B of the MRC. The result is checked to ±100 Hz using a 100 ms gate time (with no interpolation). The messages are:

PASS	35	000	0**	A3	F	31
FAIL	nn	nnn	nnn	A3	F	31
PASS	35	000	0**	LVL		31

5-88. Diagnostic 32: Interpolator Check

Effect: Tests the interpolator circuitry by first comparing the Start and Stop measurements for the Short calibration. The difference must be less than 20 counts to pass the test. If the Short calibration values pass, the Long calibration is tested. The messages are:

PASS	INTERPOL	A3	F	32
FAIL	INTERPOL	A3	F	32
PASS	INTERPOL	LVL		32

5-89. Diagnostic 33: Display MRC E and T Register Contents for Pulse Measurements

Effect: The counter displays the contents of the MRC Events (E) and Time (T) registers for pulse measurements. Level is indicated if it occurs. The chosen resolution affects the contents of both registers, but the selected sample rate does not affect register contents. Math functions, if enabled, also have no effect. The T register portion of the display includes the fraction (in decimal form) calculated from the interpolator data. The contents of the E register is the number of events counted during the time value contained in the T register. The messages are:

```
E  10019713  T  2003937  .28
E  10019713  T  2003     LVL
```

5-90. Diagnostic 34: Display Gate Bias Error

Effect: Displays the gate bias calibration error in picoseconds. The displayed value is the result of the gate bias calibration performed by DIAG 54. The counter uses this number to adjust the gate times internally. The message format is:

```
GATE BIAS ERROR  104  PS
```

5-91. Diagnostic 40: Display ROM Version Number

Effect: Displays the ROM software version number currently in use in the instrument. The message display format is:

```
ROM VERSION  3847  A4  F  40
ROM VERSION  3847  LVL     40
```

5-92. Diagnostic 41: RAM Test

Effect: Performs a test algorithm on the microprocessor external RAM. The standby RAM inside the microprocessor is assumed to be functional, and is in use when performing the test. This test erases whatever is stored in the external RAM; critical values required to restore instrument operation after the test are saved in standby RAM. The messages are:

```
PASS  RAM  A4  F  41
FAIL  RAM  A4  F  41
PASS  RAM  LVL    41
```

5-93. Diagnostic 42: ROM Test

Effect: Performs a checksum routine on the ROM. If the ROM which contains the execution code for this function is faulty, it is possible that the test may never be completed, causing an unpredictable display instead of a FAIL message. This depends entirely on the degree of the ROM failure. If the test passes or if the message display is not affected by a ROM failure, the possible messages are:

PASS	ROM	A4	F	42
FAIL	ROM U14	A4	F	42
FAIL	ROM U17	A4	F	42
FAIL	ROM BOTH	A4	F	42
PASS	ROM	LVL		42

5-94. Diagnostic 43: Repeated Reset

Effect: Performs a test sequence similar to the power-up self check. The sequence of tests for DIAG 43 is as follows:

1. Display Test — All segments lit, all annunciators lit.
2. DIAG 42 — ROM Test.
3. DIAG 1 — Self Check.
    a. DIAG 11 — Power Supply Verification
    b. DIAG 10 — Timebase Verification
    c. DIAG 30 — MRC Channel A Verification: 10 MHz Timebase
    d. DIAG 50 — LO Verification: 29.5 MHz, 35.0 MHz
    e. DIAG 31 — MRC Channel B Verification: 35 MHz
    f. DIAG 60 — IF Verification: 35 MHz; Disable INPUT 1 and IF
    g. DIAG 32 — Interpolator Check
    h. DIAG 20 — Low Frequency 50Ω Verification: 35 MHz
    i. DIAG 21 — Low Frequency 1 MΩ Verification: 35 MHz
    j. DIAG 54 — Gate Bias Calibration
4. Restore front panel annunciators based on instrument status.
5. HP-IB verification and address display.
6. Check for external reference; update annunciators.
7. Test for HOLD mode; If so, display message.

8. Test for lockouts in effect; if so, display message.

9. Set current DIAG number to 43.

The DIAG 43 routine continuously cycles through the above tests until the diagnostic or function is exited by the operator. When exited, DIAG 43, like the power-up self check, restores the status of the instrument that existed before the function was called. If the tests pass, the display alternates between showing all segments lit, FUNCTION 54 CALIBRATING, and the HP-IB address in the format shown below:

(All 24 LCD segments lit for 2 to 3 seconds)

```
FUNCTION 54  CALIBRATING
             nn       HP-IB
```

— where nn is a number from 0 to 31.

If DIAG 43 failure occurs, the messages displayed depend on which functions are failing. Refer to the descriptions of the individual diagnostic extended functions for general information about possible failures which may occur during DIAG 43.

5-95. Diagnostic 50: LO Synthesizer Verification: 29.5 MHz and 35 MHz

Effect: Sets the A5 LO frequency to 295 MHz, and sends the AUX B (LO/10 = 29.5 MHz) signal to Input B of the MRC to be counted. This test uses the same measurement procedure as Diagnostics 20, 21, 30, 31, and 60. If the 295 MHz test passes, the test is repeated at 350 MHz. If the test fails at either frequency, the "FAIL" message displays the measured AUX B frequency. If the test passes both frequencies, the second AUX B measurement (LO/10 = 350/10) is displayed. The messages are:

```
PASS   35   000   0**   A5   F   50
FAIL   nn   nnn   nnn   A5   F   50
PASS   35   000   0**   LVL      50
```

5-96. Diagnostic 51: LO Synthesizer Verification: User Entered Frequency

Effect: Lets you use the instrument as a down converter by selecting the sampler LO frequency. You are allowed to enter (via the front panel keys, or over the HP-IB) any frequency between 300 – 350 MHz. The LO will be set to the frequency entered. You can enter a new LO frequency any time. The down converted IF is available at the rear panel "IF OUT" connector.

You'll first need to determine where the LO must be set in order to generate the desired IF. The formula shown here lets you pick an IF output between 50 MHz – 100 MHz by setting the LO somewhere between 300 MHz – 350 MHz. Because the LO is quantized, some desired

IF frequencies might not be obtained. The value of N (divisor) in the formula must be an integer between 1 and 67.

$$\frac{F_{in} - IF}{N} = LO$$, where: F_{in} = Frequency of signal at INPUT 1

IF = 50 MHz – 100 MHz
LO = 300 MHz – 350 MHz
N = Integer between 1 and 67

To illustrate the use of this formula, suppose we want to down-convert an input signal of 18.08 GHz to an IF of 80 MHz. First we subtract 0.08 from 18.08 GHz which leaves 18 GHz. We must now find the values of N (upper and lower within the permitted range of 1 – 67) that can provide an approximate 80 MHz IF with a LO between 300 – 350 MHz.

By dividing 18 GHz by the lower and upper LO frequencies, we can get an upper and lower harmonic N of 60 and 51, respectively. At this point, a trial and error process of selection can be used starting with the mid-point of the range to find the exact value that best approaches 80 MHz. The exact IF is computed by the following formula:

$$F_{in} - (LO \times N) = IF$$

For a harmonic N of 55, the equation becomes, 18.08 – (327.3 MHz)(55)=78.5 MHz. Although this is close to the desired IF, we can try another number in the range, for instance 60. For a harmonic N of 60, the equation is now, 18.08 – (300 MHz)(60)= 80.0 MHz. This gives us exactly 80 MHz.

When entering a value via the front panel keyboard, a four digit number (without the decimal point) must be entered, using the **Set/Enter** key. For example, if the desired LO frequency is 310.5 MHz, enter **3, 1, 0, 5, Set/Enter.** The decimal point is displayed after the **Set/Enter** key has been pressed.

To exit DIAG 51, press the **Reset/Local** key, or use the **DEC** or **INC** key (arrow keys). The **Extended Function** key cannot be used to exit DIAG 51 (the key is interpreted as a "1"). On entry to this function, the LO is automatically set to the last value used during the measurement cycle.

Indication of success or failure is shown on the display with an asterisk. The asterisk does NOT appear if the frequency is set and measured to be within the allowable margin defined by the upper and lower bounds of the synthesizer range. If the frequency is out of the synthesizer range, the asterisk appears on the display beside the requested frequency value. For example, if the LO is set to 295.9 MHz (within the allowable range), the messages would be:

```
ENTER LO  295.9  A5  F  51
ENTER LO  295.9  LVL    51
```

If you enter 4955 MHz (which is out of range), the message will be:

```
ENTER LO 4955 *  A5  F  51
```

The asterisk also appears if the instrument fails to measure the requested LO frequency.

5-97. Diagnostic 52: LO Synthesiser Sweep

Effect: Sweeps the synthesizer from 275.0 MHz up to 375.0 MHz, in 100 kHz steps. DIAG 52 does not show a pass or fail message on the display, but instead gives a message indicating that a test is in progress. The complete sweep requires about four seconds. The results of this test may be seen by connecting a spectrum analyzer to the W2 output cable of the A5 Synthesizer Assembly. The messages are:

```
275-375 LO SWEEP A5  F  52
275-375 LO SWEEP LVL    52
```

5-98. Diagnostic 53: LO Synthesizer Lower, Upper Frequency Bounds

Effect: Determines the upper and lower bounds of the LO frequency. The A4 microprocessor attempts to program the synthesizer well below its known lower bound range. The measured frequency is a very good approximation to the lower bound. A similar procedure determines the upper bound. These upper and lower values are displayed for visual verification by the operator (the A4 microprocessor does not make a pass/fail decision). The messages are:

```
LO nnnn  HI A5  F  53
LO nnnn  HI LVL    53
```

— where nnnn represents some Local Oscillator frequency in the format nnn.n MHz (the decimal point is implied). For example, if "LO 2505 HI 3985" is displayed, the lower bound is 250.5 MHz, and the upper bound is 398.5 MHz.

The lower bound of the LO frequency should be less than 275 MHz (a typical value would be 245 MHz). The upper bound should be greater than 375 MHz (a typical value would be 405 MHz).

5-99. Diagnostic 54: Gate Bias Calibration

Effect: Performs Gate Bias Calibration. This function is always performed at power-up and can also be used to check the A14 Gate Board Assembly circuits. The results of this function can be displayed via DIAG 34. The displayed message is:

```
FUNCTION 54 CALIBRATING
```

5-100. Diagnostic 60: IF Verification: 35 MHz; Disable INPUT 1 and IF

Effect: Verifies A6 IF function. The 35 MHz test signal (AUX A/B) provided by the A5 Synthesizer Assembly is switched to the A6 IF Amplifier/Detector Assembly which in turn sends the signal to Channel A of the MRC to be counted. The signal is counted to ±100 Hz accuracy using a 100 ms gate time (with no interpolation). To ensure proper diagnostic results, the microprocessor disables the INPUT 1 circuit by turning off dc power to the A12 Microwave Module, and disables the normal IF path by turning off the first two gain stages of the A6 Assembly. The messages are:

```
PASS   35   000   0**   A6  F   60
FAIL   nn   nnn   nnn   A6  F   60
PASS   35   000   0**   LVL     60
```

5-101. Diagnostic 61: Check Level Detector

Effect: Indicates whether the level detector has triggered and been detected by the A4 microprocessor during the time since the last reset of the level flag. (A red LED at the top of the A6 IF Amplifier/Detector Assembly indicates the circuit level status.) There are two possible ways that the level flag can be reset: pressing the **Reset/Local** key to exit this function, or switching the instrument power off (STBY). If this test is exited using the **Extended Function** key, the flag is NOT reset. The messages are:

```
NO  LVL   OCCURRED   A6  F   61
    LVL   OCCURRED   A6  F   61
```

5-102. Diagnostic 62: Disable Hardware and Software IF Detector Flags: Display Measurement

Effect: Disables the IF inband detector, and assumes that the IF is always "good" (i.e. the proper IF range). After disabling the flag, the instrument returns to the normal measurement cycle for either frequency or envelope parameters and ignores the results of the IF 35 MHz – 105 MHz inband test and also the software 45 MHz – 95 MHz check. The frequency is displayed as for a regular measurement, as shown:

```
nn   nnn nnn nnn    FUNC   62
nn   nnn nnn nnn    LVL    62
```

If you call any other diagnostic (except for DIAG 63), or leave the diagnostic mode (by pressing **Reset/Local** or toggling the **Extended Function** key), the IF flags are once again enabled, and measurements proceed normally.

5-103. Diagnostic 63: Disable Hardware and Software IF Detector Flags: Display IF

Effect: Identical to DIAG 62, except that the instrument displays the IF, using the same format as DIAG 2 (Display IF). The messages are:

```
IF    nn   nnn nnn .nn    F   63
LVL   nn   nnn nnn .nn    F   63
```

5-104. Diagnostic 64: Disable Software IF Detector Flag: Display IF

Effect: Similar to DIAG 62, but instead of disabling the IF inband detector, the software flag set by the IF frequency measurement (software check) is ignored; the IF is assumed to be always within the required range. The instrument returns to the normal measurement cycle and the current IF measurement is displayed as follows:

```
IF    nn   nnn nnn .nn    F   64
LVL   nn   nnn nnn .nn    F   64
```

5-105. Diagnostic 65: IF Verification: 35 MHz: Disable INPUT 1

Effect: Similar to DIAG 60. The AUX A/B 35 MHz test signal from the A5 Synthesizer Assembly is switched by the A4 microprocessor to the A6 IF Amplifier/Detector Assembly, which in turn sends the signal to Channel A of the MRC to be counted. The signal is counted to ±100 Hz accuracy using a 100 ms gate time (with no interpolation). To perform this test, the microprocessor disables the INPUT 1 circuit by turning off dc power to the A12 Microwave Module, in the same way as DIAG 60; however, the normal IF path is NOT disabled. The messages are:

```
PASS   35   000   0**   A6   F   65
FAIL   nn   nnn   nnn   A6   F   65
PASS   35   000   0**   LVL       65
```

5-106. Diagnostic 66: Display IF Function Status Indicators

Effect: Displays the status of the four IF function LED indicators on the A6 IF Assembly. An asterisk (*) on the display indicates that a corresponding A6 LED is lit. The display is the same as the order of A6 LEDs from left to right: LEVEL (OVLD), IF PRESENT, PULSE MODE, and INBAND. The message display format is:

```
IF   STATUS   ****   A6   F   66
```

5-107. Diagnostic 67: Disable IF Detector: Display IF Function Status Indicators

Effect: Disables the IF Detector and displays the IF function status indicators in the same way as DIAG 66 above. The message display format is:

```
IF  STATUS  ****  A6  F  67
```

5-108. Diagnostic 68: Display Narrow Pulse Harmonic Numbers

Effect: Displays the harmonic numbers generated during measurement calculations for a 100 to 256 ns pulse. The harmonic numbers displayed are first, the initial estimate, followed by the actual number used for final measurement. This extended function also disables a tolerance check between the estimate and the actual number. This condition remains until some other diagnostic is called or **Set/Enter, Reset** key sequence is pressed. The message display format is "n.nn" or "nn.nn" (decimal point implied):

```
HARM  000  U  000  U  F  68
```

5-109. Diagnostic 70: Keyboard Test

Effect: Allows the front panel keyboard to be tested. Any key, when pressed, causes the name of the key function to be displayed. The displayed key names are:

FREQ	OFFSET	RESOL	SELF CK	50 OHM
PW/OFFT	SCALE	GATE MD	HP-IB	1 MOHM
PRF/PRI	SMOOTH	FUNC	FM RATE	AUTO
RESET	SET	SAMP RT	TRIGGER	MANUAL

Before a key is pressed, the messages are:

```
KEY  TEST  A7   F  70
KEY  TEST  LVL     05
```

When a key is pressed, the display changes to show the function name of the pressed key. For example, if the user presses the MANUAL key, the message will be:

```
KEY  MANUAL  A7   F  70
```

To exit this routine, you must press the **Reset/Local** key. The word RESET appears on the display for approximately 1 second, and then the instrument returns to the normal measurement mode. Pressing the **Extended Function** key will NOT exit this test, as it is interpreted as a key to be tested, and only displays the test message associated with that key. (Note that the INC and DEC functions are also not usable, as pressing either one is interpreted as a test of the SCALE and SMOOTH function keys.)

5-110. Diagnostic 71: Display Test

Effect: Causes the display to alternate between fully lit (all segments and annunciators) and fully blank (no segments and no annunciators lit). A visual verification is required. A level indication will NOT be shown in this display.

5-111. Diagnostic 72: Set Printer Option

Effect: Lets you select which printer is to be used for the hardcopy profiling measurement output. When DIAG 72 is enabled, the following menu is displayed:

```
ENTER   0*TJET/QJET   1-PJET
```

The "*" indicate the currently active option. To select ThinkJect or QuietJet, enter "0" (default) then press **Set/Enter**. This selection is confirmed by the following message:

```
THINKJET OR QUIETJET
```

To select PaintJet, enter "1" then press **Set/Enter**. This selection is confirmed by the following message:

```
PAINTJET ONLY
```

The default state occurs at power-up after the HP-IB "INIT" command is used, or after the **Set/Enter, Reset/Local** key sequence is pressed.

5-112. Diagnostic 73: Set PRT OPT

Effect: Has no effect at present and is reserved for future printer support. When called, the following message is displayed:

```
PRT  OPT   0   F   73
```

5-113. Diagnostic 80: HP-IB Verification

Effect: Causes the A11 HP-IB Interface Assembly to execute its start-up tests, resetting the HP-IB processor and initializing its memory. The messages are:

```
PASS   HP-IB          A11  F  80
FAIL   HP-IB          A11  F  80
PASS   HP-IB  000  0**  LVL     80
```

NOTE

DIAG 80 is not available over the HP-IB.

5-114. Diagnostic 81: Set Start Time for Profiling

Effect: Sets the start time for profiling from 0 to 9.999999 ms. When selected DIAG 87, DIAG 88, and DIAG 89 are turned off, and the following prompt and message are displayed:

```
0.000   T   START
```

To set a start time of 13 ns, press the following keys: **1, 3, ns, Set/Enter.** This extented function operates together with DIAG 82 and DIAG 83 to specify how the profiling is to be done. The default value of 0 is loaded during power-up (full power-up or power-up from standby), after the INIT command, or after the **Set/Enter, Reset/Local** key sequence.

5-115. Diagnostic 82: Set Stop Time for Profiling

Effect: Sets the stop time for profiling from 0 to 9.999999 ms. When selected, DIAG 87, DIAG 88, and DIAG 89 are turned off and the following prompt and message are displayed:

```
0.000   T   FINAL
```

To set a start time of 33 ms, press the following keys: **3, 3, ms, Set/Enter.** The default value of 0 is loaded during power-up (full power-up or power-up from standby), after the INIT command, or after the **Set/Enter, Reset/Local** key sequence.

The default value of 0 uses the pulse width or the external gate width to determine the stop time, as long as ESTART, EDELTA and DATAPTS are not being used to control the profile.

5-116. Diagnostic 83: Set Fine or Coarse Data for Profiling

Effect: Selects fine or coarse data for profiling. When selected, the following prompt and message are displayed:

```
FINE DATA or COARSE DATA
```

If FINE DATA is selected, 50 data points are used for profiling instead of 10 (coarse data). If COARSE DATA is selected 10 data points are used instead of 50 (fine data). This extented function operates together with DIAG 81 and DIAG 82 to specify how the profiling is to be done.

The default value of FINE,ON is loaded during full power-up, after the INIT command or after the **Set/Enter, Reset/Local** key sequence. The fine or coarse profiling mode is stored in the standby RAM before power-down.

5-117. Diagnostic 84: Set Profiling Output Printer Options

Effect: Sets the profiling output printer options for tabular, graphic, or both. When selected, the following prompt and message are displayed:

```
ENTER   0*BOTH   1-PLT   2-TBL
```

The "*" indicates the currently active option. To select table only, enter "2", then press the **Set/Enter** key. The following message appears after the selection:

```
TABLE ONLY
```

To select plot only, enter "1", then press the **Set/Enter** key. The following message appears after the selection:

```
PLOT ONLY
```

To select both plot and table, enter "0", then press the **Set/Enter** key. The following message appears after the selection:

```
BOTH PLOT AND TABLE ON
```

The default value, plot on, is loaded during full power-up, after the INIT command or after the **Set/Enter, Reset/Local** key sequence. The selection is stored in the standby RAM before power-off. Entering numbers other than 0, 1, and 2 will not change the current active mode.

When profiling, the message "PROFILING- - - -" is displayed. After the profiling is completed, the display changes to "PRINTING PLOT- - - -" during graphic output to the printer. The display changes to "PRINTING TABLE- - - -" during tablular output to the printer. When all the output to the printer is completed, the average frequency is displayed.

During Math overflow, the "MATH OVERFLOW" message is displayed at the end of profiling. The same message is also printed out on the text portion of the plot. These can be found alongside the rows for "Top of freq axis =", "Bottom of freq axis =" and "Average frequency =". The table output also has the same message printed out if there is a Math overflow error.

If you choose to manually control the profiling set-up parameters and then enter invalid values or parameter combinations, a plot error will occur. The counter will be unable to generate a plot and the message "PLOT ERROR" is printed out alongside the text legend of the plot. When this happens, the following parameters are set to 0 to indicate the error condition. In addition, the counter will display all 0's.

Time per division = 0 ns
Freq per division = 0 Hz
Start of time axis = 0 ns
Stop of time axis = 0 ns
Top of freq axis = 0 Hz
Average frequency = 0 Hz
Average step width = 0 ns

To obtain the printed output, ensure the counter's HP-IB address is set to 31 (TALK ONLY mode) and the printer is set to LISTEN ALWAYS mode. There must not be any other equipment connected to the HP-IB bus besides the printer and the counter (otherwise, the bus will hang). If the printer is not connected to the counter or set for the correct configuration, exit the profiling mode by cycling power to the counter.

During front panel operation, if you don't want to output data to the printer, then set the HP-IB address to values other than 31. At the conclusion of the profiling process, the average frequency is displayed.

5-118. Diagnostic 85: Set Filter On/Off for Profiling Output

Effect: Toggles between filter on and filter off when selected. The following message is displayed when selected:

FILTER ON (or) FILTER OFF

The default value, filter on, is loaded during full power-up, after the INIT command or after the **Set/Enter, Reset/Local** key sequence. The filter state (on/off) is stored in the standby RAM before power-off.

5-119. Diagnostic 86: Enter ID Prefix for Profiling Printer Output Plot

Effect: Permits entry of an identifying prefix no larger than six decimal digits for a specific printer output plot. When selected, the following prompt and message are displayed:

```
ID   PRFIX  0   F   86
```

When this function is selected, the suffix for the ID is initialized to 0001. Input of leading zeros is not displayed but will be output to the printer. For example, to input Feb 8, 1990, press these keys: **0,2,0,8,9,0, Set/Enter**. The display shows 20890, but the output on the plot or the table will be 020890.0001 for the first hardcopy.

The default value of 000000 (the full ID default is 000000.0001) is loaded during power-up (full power-up or power-up from standby), after the INIT command or after the **Set/Enter, Reset/Local** key sequence.

5-120. Diagnostic 87: Set Number of Data Points (Steps) for Frequency Profile

Effect: Sets the number of steps during profiling. When selected, DIAG 81 and DIAG 82 are turned off and the following message and prompt is displayed:

```
DATA PTS  0   F   87
```

To set the number of steps to 35, press these keys: **3, 5, Set/Enter**. A maximum of 2 digits is allowed (the maximum number of steps is 99). This extended function operates together with DIAG 88 and DIAG 89 to specify how the profiling is to be done. The default value of 0 is loaded during power-up, after the INIT command, or after the **Set/Enter, Reset/Local** key sequence.

5-121. Diagnostic 88: Set Start IF Cycle for Frequency Profile

Effect: sets the start event for profiling between 0 and 999999. When selected, DIAG 81 and DIAG 82 are turned off and the following message and prompt is displayed:

```
E  START  0   F   88
```

To set the start event to 213, press the following keys: **2, 1, 3, Set/Enter.** This extented function operates together with DIAG 87 and DIAG 89 to specify how the profiling is to be done. The default value of 0 is loaded during power-up, after the INIT command, or after the **Set/Enter, Reset/Local** key sequence.

5-122. Diagnostic 89: Set Number of IF Cycles Per Step for Profile

Effect: sets the delta events for profiling between 0 and 999999. When selected, DIAG 81 and DIAG 82 are turned off and the following message and prompt is displayed:

```
E DELTA   0   F   89
```

To set the delta events to 34, press the following keys: **3, 4, Set/Enter.** This extented function operates together with DIAG 87 and DIAG 88 to specify how the profiling is to be done. The default value of 0 is loaded during power-up, after the INIT command, or after the **Set/Enter, Reset/Local** key sequence.

5-123. Diagnostic 90: Set Gate Width In Time

Effect: Lets you specify the gate width in time from 0 through 9.999999 msec. If the programmed gate width is longer than the measured pulse, then the counter will read 0 (actual width may vary due to presence of FM or chirp on pulse). When selected, the following prompt and message is displayed:

```
ENTER   GW   0   A9   F   90
```

Enter the desired gate time and press **Set/Enter.** The counter resumes measurement using the new gate time and displays the resulting measurement. Entering 0 causes the counter to automatically determine the gate width. (See pages D-5 thru D-7 in the Operating and Programming Manual for more details on gating.)

5-124. Diagnostic 91: Set Number of Averages for Frequency Measurement

Effect: Lets you specify how many separate frequency measurements are averaged to yield a displayed value. The range of selectable values is 0 through 9,999. Selecting a value of 0 disables this extended function and causes the counter to automatically determine the number of averages necessary for a desired resolution. If the total accumulated gate time for a measurement exceeds 20 seconds, the counter may read a zero value. The total gate time equals the Programmed Gate Width X the Number of Averages. When selected, the following prompt and message are displayed:

```
ENTER   AV   0   A9   F   91
```

Enter the desired average number and press **Set/Enter.** The counter resumes measurement using the new average value and displays the resulting measurement. The **Resolution** key now only controls the number of displayed digits.

5-125. Diagnostic 92: Force Pulse or CW Measurement Mode

Effect: Lets you override the counter's ability to automatically distinguish between pulse or CW signals. Refer to the "Note", in Section 2 of the Operating and Programming Manual, under the sub-section titled "CHECK SAMPLE RATE" for information about DIAG or EFUN 92 use during HOLD. When enabled, the following menu is displayed with the asterisk indicating the currently active mode:

ENTER 0-AUTO 1-CW 2*PLS

If you want the counter to measure only pulsed signals, enter "2", then **Set/Enter**. The following message appears and the counter resumes measurement:

PULSE MEASUREMENTS ONLY

If you want the counter to measure only CW signals, enter "1", then **Set/Enter**. The following message appears and the counter resumes measurement:

CW MEASUREMENTS ONLY

If you want to return to the automatic recognition of either pulse or CW signals, enter "0", then **Set/Enter**. The following message appears and the counter resumes measurement:

PULSE AND CW MEASURE

5-126. Diagnostic 93: Enter <100 NS Pulse Mode

Effect: Enables <100 nanosecond pulse mode after entering MANUAL mode. This extended function is necessary when you're measuring pulse bursts that are less than 100 nanoseconds wide. When first selected, this mode is turned ON and the following message is displayed momentarily:

LESS THAN 100 NS MODE ON

When selected a second time, this mode is turned OFF and the following message is displayed momentarily:

LESS THAN 100 NS MODE OFF

Any further selection of this function continues to toggle it on or off.

5-127. Diagnostic 94: High Resolution (INPUT 1, PRF/INPUT 2, 1 MΩ)

Effect: Turns High Resolution ON. This extended function is useful when your measurements require resolution greater than 1 Hz. The function applies only to INPUT 1 pulse repetition frequency and INPUT 2, 1 MΩ frequency measurements. The higher resolution obtained using this function depends on the input frequency. Refer to *Table 2-4* of the Operating and Programming Manual for detailed limits.

When first selected, this mode is turned ON and the following message is displayed momentarily:

```
HIGH RESOL ON
```

When selected a second time, this mode is turned OFF and the following message is displayed momentarily:

```
HIGH RESOL OFF
```

Any further selection of this function continues to toggle it on or off.

5-128. Diagnostic 95: Set Gate Width by Events

Effect: Lets you set the gate width by IF events or cycles from 0 through 999999. If the programmed gate width is longer than the measured pulse, then the counter will read 0. To allow the counter to determine the gate width automatically enter 0. When selected, the following prompt and message is displayed:

```
0  ENTER GW
```

Enter the desired gate width by events and press **Set/Enter.** The counter resumes measurement using the new gate width and displays the resulting measurement.

5-129. Diagnostic 96: Enter Chirp Mode

Effect: Causes the instrument to accommodate frequency chirp on the pulse by reducing the gate width. When first selected, this mode is turned ON and the following message is displayed momentarily:

```
CHIRP MODE ON
```

When selected a second time, this mode is turned OFF and the following message is displayed momentarily:

CHIRP MODE OFF

Any further selection of this function continues to toggle it on or off.

5-130. Diagnostic 97: Set IF for Manual Center Frequency

Effect: allows you to specify the IF (in MHz) when setting a manual center frequency. When selected, the following prompt and message is displayed:

ENTER IF 0 A9 F 97

To set the IF to 56 MHz, press these keys: **5, 6, Set/Enter.** No more than 2 digits are allowed with a maximum IF of 99 MHz.

5-131. Diagnostic 98: Keyboard Lockout

Effect: Causes the instrument to ignore all front panel keyboard entry, except for a special key sequence that exits the mode. The display continues to function normally. When the user enters this mode, a lockout message is shown for approximately 1 second; the counter then returns to its normal measurement display. The message is:

KEY BOARD LOCK OUT

NOTE

A level condition will NOT be indicated in the display.

This function can only be entered using the standard diagnostic or extended function keyboard entry sequence (**Set/Enter, Extended Function, 9, 8, Set/Enter**). The **INC** key advances to a maximum number of 96, and cannot be used to enter DIAG or EFUN 98.

If a key is pressed at any time after the lockout is enabled, the lockout message appears briefly to indicate that the key has been ignored. The counter then returns to counting. If the instrument is powered-up from Standby with DIAG 98 active, the lockout message reappears for approximately 2 seconds. The counter then returns to counting. When the Keyboard Lockout is enabled and counting resumes, the extended function number defaults to 1.

The only way to exit DIAG 98 is to remove and then reconnect the ac power cord, send "INIT" over HP-IB, or to enter the following special key sequence: **7, 4, 0, RESET/LOCAL**. Pressing this key sequence restores normal front panel control of the counter.

5-132. Diagnostic 99: Display Lockout

Effect: Locks out all messages from the display. All the annunciators are blank and the display shows the following constant message:

DISPLAY LOCK OUT

NOTE

A level condition will NOT be indicated in the display.

This function can only be entered using the standard diagnostic or extended function keyboard entry sequence (**Set/Enter, Extended Function, 9, 9, Set/Enter**). The **INC** key advances to a maximum number of 96, and cannot be used to enter DIAG or EFUN 99. If the instrument is powered-up from Standby with DIAG 99 active, the counter goes into normal measurement mode and displays the lockout message. When the Display Lockout is enabled and counting resumes, the diagnostic number defaults to 1. The only way to exit DIAG 99 is to remove and then reconnect the ac power cord, send "INIT" over HP-IB, or to enter the same key sequence used for exiting DIAG 98: **7, 4, 0, RESET/LOCAL**. Pressing this key sequence causes the counter to return to normal message display.

5-133. DETAILED CIRCUIT DESCRIPTIONS

The following paragraphs describe the theory of operation of each of the assemblies (pc boards) in the instrument. An overall block diagram (*Figure 5-15*), and schematic diagrams (*Figures 5-17* through *5-28*) are provided at the end of Section 5. The descriptions are arranged in numerical order by assembly reference designation, with the exception of the A8 Motherboard/A1 Power Supply Regulator/Power Supply Control/Timebase Assemblies.

5-134. Power Supply Block (A8 Motherboard/A1 Assemblies)

The power supply for the HP 5361B, shown on Sheet 2 of *Figure 5-15* (the overall block diagram), consists of the Power Supply Regulator circuit on the A8 Motherboard Assembly, the Power Supply Control circuit on the A1 Power Supply Control/Timebase Buffer Assembly, and several chassis-mounted components. The A8 Motherboard Assembly contains the majority of the power supply components. The voltage regulators for the timebase oscillator and buffer circuits are located on the timebase buffer half of the A1 Assembly, and these regulators are described in a separate circuit description, beginning at Section 5-135.

In the following circuit description, the chassis-mounted components are described first. Then, each of the functional stages of the +5, +15, and –5.2 volt supplies are described, first in general, and then specifically for each individual supply, as necessary. Finally, the +12V, –24V, and fan voltage are described. The board assembly being described will be identified at the beginning of each functional description, and all reference designations in the description are in reference to the named assembly, unless otherwise indicated.

CHASSIS-MOUNTED COMPONENTS. Chassis-mounted power supply components consist of the ac power module (A13), and the power transformer (T1). (Refer to *Figure 5-27. A13 Power Input Module and Transformer Assembly Schematic Diagram*). The ac power module in the instrument's rear panel contains a connector for the power cord, a fuse (in the hot line), a filter, and a four position line voltage selector card. The position of the voltage selector card determines the connections to the primary windings on the power transformer.

The power transformer converts the ac line voltage to several lower voltages and isolates the ac line from the instrument circuitry. Both the primary and secondary sides of the transformer have cable connectors to allow easy disassembly and reassembly of the instrument.

For the following paragraphs, refer to one of the appropriate schematic diagrams:

- *Figure 5-17. A8 Motherboard/Power Supply Regulator Assembly*
- *Figure 5-18. A1 Timebase Buffer/ Power Supply Control Assembly (Sheets 1 and 3)*

RECTIFIERS (A8). The lowest-voltage transformer secondary is center-tapped: CR15 is a full-wave, center-tap rectifier for the unregulated +5V, and CR11 and CR12 form a full-wave, center-tap for the unregulated –5.2V. The other two transformer secondaries are rectified by

full-wave bridge rectifier CR13 for the unregulated +15V and +12V, and by CR14 for the unregulated –24V and fan voltage. The rectified unregulated voltages are present whenever ac power is connected to the instrument.

Fuse F2 is in series with the secondary which supplies the unregulated +15V because this secondary winding has enough series resistance to prevent a secondary short circuit from blowing the primary fuse.

ENERGY STORAGE CAPACITORS (A8). C3, C4, C18, and C19 store energy to supply the dc power to the regulators between peaks of the ac line half-cycles. Resistors R20A through R20E, and R14C slowly drain the charge out of the energy storage capacitors after the instrument is unplugged.

SERIES PASS TRANSISTORS (A8). Q7, Q9, and Q10 are series pass transistors for the +15V, –5.2V, and +5V regulators. Q8 supplies the base current for Q10 from the unregulated +15V. CR10 prevents the large reverse currents through Q8 in case the unregulated +15V is off for any reason. The Power Supply Control part of the A1 Assembly supplies the base current drive for Q7, Q8, and Q9. R14A,B,D, and R18 keep Q7, Q8, Q9, and Q10 turned off when there is no base drive, such as in Standby mode or when the A1 Assembly is not plugged into the instrument.

CURRENT SAMPLING RESISTORS (A8). The load currents from the +5V, +15V, and –5.2V supplies flow through R8, R10, and R11, causing small voltage drops which are monitored by the Power Supply Control portion or the A1 Assembly. The output voltages of these three supplies are sensed at the load side of the current sampling resistors. The voltage sense (V SENSE) voltages are referenced to ground, and current sense (I SENSE) voltages are referenced to the V SENSE lines.

R9, R5, and R4 provide a minimum load current to keep the voltage regulators on if there is no other load. CR5, CR7, and CR6 help protect the loads in case a regulator fails to regulate the voltage, or in case a supply is shorted to some other supply. C8 slows the fall time of the +5V supply when the instrument is switched to Standby mode, giving the microprocessor time to store the instrument state into the Standby RAM before the supply drops below the level required for proper operation.

ERROR VOLTAGE AMPLIFIERS (A1). Operational amplifiers U14D, A, and B amplify the difference between the voltage sense lines of the +5V, +15V, and –5.2V supplies, and a stable voltage reference. Since the reference voltage is +5.0V, the +5V V SENSE is used directly, but the V SENSE lines for the +15V and -5.2V supplies are scaled.

The +15V SENSE is scaled by R42, R43, and R44 down to +5V so that it can be compared to the +5.0V reference at the input of U14A. The -5.2V V SENSE is scaled by R41, R52, and R53, which sum the –5.2V V SENSE and the +5.0V reference to obtain 0V at U14B(5) where it is compared to the 0V from R45D. Schottky diode CR26 prevents U14B's input from being pulled negative enough to cause malfunction, CR27 reduces the current injected into the –5.2V supply through the –5.2V V SENSE line when in Standby mode.

ERROR AMPLIFIER SUPPORT CIRCUITRY (A1). Support circuitry for the error amplifiers includes Analog OR Gates, and level shifting and buffering circuits. The Analog OR Gates allow the power supply output voltages to be controlled by the error voltage amplifiers, the current sense amplifiers, or the L_STBY control line (or several other things in the case of the +5V regulator). Level shifting circuitry is required for the +15V and -5.2V regulators because the error voltage amplifiers and the Analog OR Gates use a +12V supply (to be described later). The buffer circuits provide the proper drive current to the series pass transistors on the A8 Assembly.

Standby. The front panel ON/STBY (POWER) switch electronically turns off the main regulators in Standby mode via the L_STBY line. As mentioned above, when the L_STBY line is asserted LOW it takes control of the voltage regulators through the Analog OR Gates and turns off their outputs. R29E pulls up the L_STBY line to +12V when negated (instrument ON). R38A and CR7 supply current from the +5V UNREG supply to the STBY LED on the instrument's front panel.

+5V Analog OR Gate. In normal +5V regulator operation, CR12 is forward biased and error-voltage amplifier U14D is controlling the +5V output. If the regulator is current limited due to some fault condition in the load, CR22 will be forward biased. If the +5V UNREG voltage drops too low for proper regulation CR13, CR14, and CR15 will be forward biased. If the L_STBY line is held LOW, CR6 will be forward biased. If some serious failure occurs in the regulator circuit, CR25 clamps the analog OR voltage. Only one of these conditions may control the regulator at any particular time. In any mode other than the normal (voltage regulated) mode, CR12 will be far reversed biased because the output of amplifier U14D will be saturated near the +12V supply. R45C biases the diodes in the Analog OR Gate.

+5V Buffer. The buffering stage in the +5V regulator consists of emitter-follower Q20, CR21, and CR23. The Q20 collector current is supplied from the +15V UNREG line through CR23. CR21 limits the reverse emitter-base voltage of Q20 when the base voltage is pulled down suddenly (such as when going into Standby mode). The output of the buffer stage is the +5V DRIVE line, which drives the +5V pass transistors on the A8 Assembly.

+15V Analog OR Gate. In normal +15V regulator operation, CR11 is forward biased and error-voltage amplifier U14A controls the +15V output. CR9 is forward biased when the L_STBY line is held LOW. If the regulator is current limiting (load fault), the +15V current sense amplifier (Q12,13) will turn on and pull down the Analog OR Gate voltage. R29F supplies bias current for the Analog OR Gate. When the regulator is not in the normal (voltage regulated) mode CR11 will be far reverse biased because the output of U14A will be saturated near its +12V supply.

+15V Level Shifter and Buffer. Level shifting and buffering in the +15V regulator is performed by common-emitter Q10 and associated components CR10 and associated components CR10, CR4, R30A, and R31. CR10 and CR4 raise the Analog OR Gate voltage high enough above ground to work properly. R30A keeps Q10 cut off when the instrument is in Standby mode. R31 limits the current in Q10 if the +15V UNREG voltage drops too low

to allow voltage regulation. The output of the level shifter and buffer is the +15V DRIVE line, which drives the +15V series pass transistor on the A8 Assembly.

–5.2V Analog OR Gate. In normal -5.2V regulator operation, CR29 is forward biased and error-voltage amplifier U14B controls the -5.2V output. CR8 will be forward biased when the L_STBY line is held LOW. If the regulator is current limiting (load fault), the -5.2V current sense amplifier (Q19) will turn on and pull down the Analog OR Gate voltage. R29G provides bias current for the analog OR gate. When the regulator is not in the normal (voltage regulated) mode, CR29 will be far reverse biased because the output voltage of U14B will be saturated near its +12V supply.

–5.2V Level Shifter. The level shifter for the –5.2V regulator consists of Q15 and associated components CR28, CR18, and R30D. Q15 operates in the common-base mode. CR28 and CR18 raise the Analog OR Gate voltage high enough above ground to work properly. R30D keeps Q15 turned off when the instrument is in Standby mode.

–5.2V Buffer. The buffer for the -5.2V regulator consists of emitter-follower Q16 and associated components R38D and R45A. R45A keeps Q16 turned off when the instrument is in Standby mode. R38D limits the current in Q16 if the –5.2V UNREG voltage drops too low to allow regulation. The output of the buffer is the –5.2V DRIVE line, which drives the –5.2V series pass transistor on the A8 Assembly.

CURRENT SENSE AMPLIFIERS (A1). The Current Sense Amplifiers monitor the voltage difference between the I SENSE and V SENSE inputs to the A1 Assembly, which are the two sides of the current sampling resistors on the A8 Assembly. When this voltage (load current) exceeds a certain value, the Current Sense Amplifier takes control of the voltage regulator through the Analog OR Gate and reduces the output voltage. In the +15V and –5.2V regulators, the current limit is approximately constant, but the +5V regulator has foldback current limiting (that is, the current limit decreases as the regulator output voltage decreases to reduce the power dissipation in the series pass transistor).

+5V Current Sense. In the +5V regulator, the current sense amplifier consists of operational amplifier U14C and resistors R47C, R47D, R46C, R46D, and R37C. These components form a differential amplifier with a voltage gain of about 5, and with its output voltage referenced to the Analog OR Gate voltage. As the load current increases, the output voltage of U14C decreases. When U14C's output voltage becomes one diode drop lower that the Analog OR Gate voltage, CR22 becomes forward biased, CR12 becomes reverse biased, and the current sense amplifier takes control of the voltage regulator. R37C generates an offset in the differential amplifier which tends to reverse bias CR22. Since this offset depends on the voltage across R37C, the current limit decreases as the +5V output voltage decreases (foldback current limiting). The short-circuit output current is approximately one-half of the maximum output current.

+15V Current Sense. In the +15V regulator, the current sense amplifier consists of Q12, Q13, CR3, R30B, and R30C. When the +15V load current becomes large enough to forward bias the Q12 base-emitter junction and CR3, Q12 supplies base current to Q13, Q13's collector

current pulls down the Analog OR Gate voltage (CR11 becomes reverse biased), and the current sense amplifier takes control of the voltage regulator. R30B and R30C keep Q12 and Q13 turned off during normal (voltage regulated) operation. CR3's voltage drop allows the Current Sense Amplifier to work when the +15V output is shorted to ground.

–5.2V Current Sense. Q19 is the current sense amplifier in the –5.2V regulator. When the –5.2V load current pulls down the Analog OR Gate voltage (CR29 becomes reversed biased) and the Current Sense Amplifier takes control of the voltage regulator.

COMPARATORS (A1). The comparator section of the Power Supply Control circuit on A1 Assembly generates Reset and NMI (Non-Maskable Interrupt) signals to the instrument's microprocessor (the HP-IB microprocessor also uses the Reset signal) based on the condition of the +5V regulator, generates another logic signal to the microprocessor which indicates the condition of the other voltage regulators, and lights and LED on the A1 Assembly when the power supply is in standby or when any of the voltage regulator outputs is incorrect.

L_μP_NMI. Comparator U8C generates the L_μP_NMI signal by monitoring the voltage on CR12, a diode in the +5V Analog OR Gate. When the +5V regulator is regulating properly, CR12 will be forward biased and L_μP_NMI will be negated (HIGH); otherwise, CR12 will be reversed biased and L_μP_NMI will be asserted (LOW). The L_μP_NMI signal is used to give the microprocessor immediate warning that the +5V supply is going down (such as when going into Standby) so that state variables can be stored into the Standby RAM before +5V drops below the operating limit for digital circuits.

L_μP_RST. The L_μP_RST signal is generated by U8D, U7D, R15, R13, C8, R29C, R14, and C24. U8D monitors the voltage on CR12 exactly like U8C does; therefore, the output of U8D is LOW when the L_μP_NMI signal from U8C is LOW. The voltage divider consisting of R29C and R14 provides an approximate +6V reference for comparator U7D. C8, R13, and R15 form a dual time constant circuit; R13 slowly charges C8 and R15 quickly discharges C8.

When the +5V supply is turned on, U8D holds C8 discharged until CR12 becomes forward biased (indicating proper voltage regulation). C8 then slowly charges to +12V through R13. U7D compares the voltage on C8 to the approximate +6V reference, so L_μP_RST (output of U7D) will be asserted (LOW) when the +5V supply is not regulated and for a fraction of a second after it becomes regulated. The L_μP_RST line is pulled up on the A4 Microprocessor Assembly.

R15 and C8 provide a short delay between the assertion of L_μP_NMI and the assertion of L_μP_RST. This delay is long enough to allow the microprocessor to store variables in the Standby RAM, but short enough to ensure that the microprocessor is held in Reset when the +5V supply is lower that the limit for digital circuits. R15 also limits the peak current when U8D discharges C8.

H_PWRSP_OK. The H_PWRSP_OK signal indicates to the A4 microprocessor that the voltage regulators (other than the +5V regulator) have the proper output voltage. The signal is derived from the wire-ORed outputs of comparators U8A, U8B, U7A, U7B, and U7C. U8B

checks the +15V regulator by monitoring the voltage on CR11 in the Analog OR Gate; when the +15V output is properly regulated, CR11 is forwarded biased, otherwise CR11 is reverse biased. Similarly, U8A checks the –5.2V supply by monitoring the voltage on CR29. U7A compares the average of +5V μP V SENSE and +5V OSC V SENSE (standby +5V regulators on the timebase buffer half of A1) to 4.5V. R28B and R28C form a voltage divider which takes the average of the two V SENSE lines. R36B and R37A form a voltage divider which derives approximately 4.5V from the 5.0V reference. U7C compares the +12 OSC V SENSE (standby +12V regulator on the timebase buffer half of A1), divided by two by voltage divider R28D and R36A, to the +5.0V reference. U7B compares the –24V V SENSE (standby –24V regulator on A8), scaled and shifted by R54 and R29D, to the +5.0V reference. R35A, B, D, and R36C provide a small amount of positive feedback (hysteresis) for comparators U7A, C, and B to prevent oscillation with voltages exactly at the switching thresholds. R45B pulls up the H_PWRSP_OK line to the +5V V SENSE.

Standby/Power Fail LED. The DS1 LED provides an indication that some regulator is not properly regulating its output voltage. The LED is ON in Standby, when a regulator is current limited, when an unregulated voltage falls too low for adequate regulation, or when a regulator fails. Since the L_μP_NMI line, when asserted, indicates lack of regulation of some other supply, Q6 and Q7 are ORed to provide the LED drive. R38B limits the current in DS1, although the current will vary with the +5V UNREG voltage. CR2 clamps the voltage on the anode of DS1 to ensure that the LED will not light when both digital lines are HIGH. R37B ensures that Q6 will not turn ON from the leakage current when the A4 Microprocessor Assembly (with pull-up resistor) is not plugged in.

VOLTAGE REFERENCE (A1). U1 generates the +5.0V reference voltage used by the +5V, +15V, and –5.2V regulators and the comparator section. R36D isolates the REF +5.0V line which goes to the Power Supply Test (PST) connector on A8 so that the line, if accidentally shorted to ground, will not affect the power supply.

+12V REGULATOR (A1). Voltage regulator U2 supplies +12V to the other integrated circuits in the Power Supply Control portion of A12. L7 prevents high frequency noise and interference on the +15V UNREG line (which supplies U2) from being injected into the ground of the Power Supply Control circuit through bypass capacitor C14. R29B isolates the V/+12 PS line which goes to the PST connector on the A8 Motherboard Assembly so that the V/+12 PS line, if accidentally shorted to ground, will not affect the power supply.

Note that the +12V regulator described above is a different circuit than the +12V OSC regulator in the Timebase Buffer portion of A1, which supplies the 10 MHz oscillator.

–24V REGULATOR (A8/A1). The -24V regulator primarily supplies the oven circuit of the optional timebase oscillator, but is also used by the A5 LO Synthesizer. The main part of the -24V regulator is on the A8 Motherboard Assembly, but the circuit that switches between normal and warm-up modes for the oven oscillator is on the A1 Assembly.

MAIN –24V REGULATOR (A8). On A8, the -24V regulator consists of U1, CR2, CR3, CR4, and associated components. CR2 and CR3 help protect U1 from reverse currents in case of

accidental grounding of the V_{in} or V_{out} terminals. CR4 prevents the –24V supply from becoming positive under any possible fault condition. The OVEN DRIVE line from A1 is either grounded (normal) or opened (warm-up). During the oven warm-up, the –24V supply is –28V typical (–30V maximum). During normal operation, R7 is in parallel with R19, causing the output of the regulator to drop to –24V. The oven draws a large amount of current during warm-up after which the current drawn decreases suddenly to a relatively low level.

NORMAL/WARM-UP CONTROL (A1). In the Power Supply Control portion of A1, Q21, CR24, R47B, and R46A switch the –24V regulator (on A8) between normal and warm-up modes. L_OVN_COLD is a +5V logic signal from the Timebase Buffer portion of A1 which is LOW when the oven is cold, and HIGH when the oven is warm. Q21 is a common-base stage which is either turned off (cold) or saturated (warm); its output is the OVEN DRIVE line to the A8 Motherboard Assembly. R47B limits the current in Q21. CR24 increases the noise immunity when L_OVN_COLD is LOW. R46A holds Q21 turned off when L_OVN_COLD is LOW.

When the TCXO standard timebase oscillator is used, the –24V will be in its normal (warm) mode because the TXCO assembly simulates the Oven Monitor output of the oven oscillator.

FAN CURRENT REGULATOR (A1/A8). The instrument is cooled by a dc fan, B1. The fan is driven by a constant-current regulator consisting of two parts: a circuit in the Power Supply Control portion of A1 that generates a small constant current when the instrument is ON (not in Standby), and a current mirror/amplifier on A8 that boosts the current by a factor of about 200.

CONSTANT CURRENT SOURCE (A1). In the Power Supply Control portion of A1, the circuit consisting of Q22, CR5, CR16, R29A, R47A, and R37D generates a small constant current. Q22 is a common-base stage that is either in the linear range or turned off; its output is the FAN DRIVE line, which goes to the A8 Motherboard Assembly. R29A and R47A set the current in Q22. CR5 turns off the current through Q22 when the L_STBY line is asserted (LOW); when the instrument is ON, CR5 is reversed biased. R37D holds Q22 cut off, and CR16 increases the noise margin when in Standby mode.

CURRENT MIRROR/AMPLIFIER (A8). On A8, a current mirror/amplifier composed of Q2, Q6, CR9, R12, R13, R17, and C10 boosts the current of the FAN DRIVE line (from A1) by a factor of about 200 to generate the fan current. The small constant current from A1 flows through CR9 and R12, causing a voltage drop that is applied across the base-emitter junction of Q2 and R17 in series (and filtered by C10). CR9 compensates for the temperature variations of Q2's base-emitter voltage. Q2, Q6, and R13 form a feedback circuit with high current capability and very high current gain. The current through R17 flows through Q6, F1, and the fan; the positive side of the fan motor is grounded. Since the voltage across R17 is approximately equal to the voltage across R12, the current through the fan is equal to the FAN DRIVE current from A1 Assembly times the ratio of R12 to R17. Fuse F1 protects the fan in case of a failure in the fan current regulator.

POWER SUPPLY TEST CONNECTOR (A8). Connector J7 on A8 Motherboard Assembly can be used as a central point for probing the power supply voltages. All of the signals in the connector (except ground) are protected with series resistors, or are otherwise current limited to prevent damage to the instrument should the pins be accidentally shorted together or shorted to ground. R1A through R1E and R2A through R2E protect the V SENSE and I SENSE lines; protection resistors for other signals are on the plug-in assemblies, which generates the signals.

In addition to the main power supply voltages (+5V, +15V, –5.2V, –24V), the test connector has pins for monitoring the +12V and +5.0V Reference (from the Power Supply Control portion of A1), the +5V OSC and +12V OSC oscillator supplies (from the Timebase Buffer portion of A1), the microprocessor standby +5V μP (also form the Timebase portion of A1), the MRC's +3V (from the A3 Counter Assembly), the fan voltage, and the load current in the main +5V, +15V, and –5.2V supplies. In addition, the instrument may be put into Standby mode by grounding the L_STBY pin, available at the test connector.

MISCELLANEOUS CIRCUITS (A8). The following paragraphs describe additional circuits on the A8 Motherboard Assembly that are not part of the power supply.

Microprocessor RAM Backup Diode. The Standby RAM on A4 Microprocessor Assembly is supplied by the +5V μP voltage regulator on the Timebase portion of A1 whenever the instrument is plugged in. CR1 (on A8) is a Schottky rectifier diode between the +5V μP and the main +5V, so that the main +5V can supply the microprocessor RAM in case of failure in the Timebase Buffer, thus allowing the A4 Microprocessor Assembly to continue to operate in case of a Timebase Buffer +5V μP regulator failure.

Microwave Module Turn-Off. To reduce certain forms of the electromagnetic interference at particular times, a microwave turn-off circuit on A8 Motherboard Assembly allows the A4 microprocessor to turn off the Microwave Module circuitry. The microwave turn-off circuit operates by interrupting two of the power supply connections to the A12 Microwave Assembly. The circuit defaults to the ON state if the A4 Microprocessor Assembly is not installed.

The microwave turn-off circuit is controlled by the L_μW_OFF line from the A4 microprocessor. Q4, Q5, R15, R16A and R16B gate the +5V to the IF preamplifier portion of A12 Assembly. Q1, Q3, CR8, and R16C, D, and E gate the +15V to the sampler driver portion of the A12 Assembly. In normal operation, Q1 and CR8 drop the +15V supply to about +13.5V (typical) for proper operation of the sampler driver.

HP-IB Common Mode Choke Filter. This filter keeps signals from the HP-IB circuit out of the +5V supply. A Common Mode Choke (CMC) filter is used on the +5V and ground lines which supply the bus drivers and terminations of the A11 HP-IB Interface Assembly. The CMC filter consists of L1, C1, and C2.

Configuration Jumpers. JMP1 through 7 and pull-up resistors R3A through R3I are factory set connectors that indicate to the A4 microprocessor the instrument configuration and options.

IF MON RTN Ground Jumpers. The IF_MON signal to the rear panel has a separate return path (IF_MON_RTN) to A3's digital ground to isolate the IF_MON signal from the A8 motherboard ground plane (used by the analog signals for ground reference and return paths). Jumper wires W1 and W2, near the rear panel IF OUT connector (J4), provide the required ground connections. W2 ties the return path to the body of J4, and W1 ties the body of J4 to the motherboard ground plane.

5-135. Timebase Buffer Block (Part of A1 Assembly)

The Timebase Buffer block, shown on Sheet 2 of *Figure 5-15*, on the A1 Assembly conditions an internal or external timebase reference signal so that it can operate the instrument's synthesizer, its MRC Counter, and provide a reference signal from which other instruments may be operated. The internal timebase reference source can be either a 10 MHz Temperature Compensated Crystal Oscillator (TCXO), or a 10 MHz ovenized crystal oscillator (A10 Option 001 or 010 Oven Oscillator). An external reference source must provide a sine or square wave at 1, 2, 5, or 10 MHz, 0.7V p-p minimum into 1 kΩ shunted by 30 pF.

When an external reference is applied to the rear panel External Reference In connector, the signal appears on the EXT REF IN line at P1A(1,26). (Refer to Sheet 3 of *Figure 5-18. A1 Timebase Buffer/Power Supply Control Schematic Diagram.*) The external reference is preamplified by transistor Q17, and sent to one-shot U3. CR20 and CR30 provide input protection, CR19 temperature stabilizes the bias point of Q17, and CR31 prevents Q17 from saturating due to high level external reference inputs. U3 produces periodic 50 ns pulses, resulting in a comb of frequencies that are harmonics of the of the external reference frequency. Bandpass amplifiers Q3 and Q4, and their associated tank circuits consisting of L8, C20, C21, L1, C2, L2, and C3 filter out all frequency components except for the desired 10 MHz. CR17 insures unidirectional current flow at the output of U3.

NAND gate U4A acts as a sine wave-to-TTL converter. When an external timebase reference is used, TTL level, 50 ns pulses appear at U4A(3). U4D ensures that the input to U10A(1) is always HIGH in the absence of an external timebase reference.

U5A is a retriggerable one-shot serving as a detector for external reference 10 MHz pulses. The values of R27 and C27 correspond to a triggered pulse width of 1.2 μs. Any periodic retrigger pulse with an interval less than 1.2 μs will keep the output of U5A (L_EXT_REF) LOW, indicating the presence of an external timebase reference.

An external timebase reference will always disable the internal reference in two ways. First, because the L_EXT_REF line will disable gate U10B. Also, the L_EXT_REF line will shut

down the dc power to the optional ovenized oscillator by means of transistor switches Q1 and Q8, or the standard TCXO by means of switches Q2 and Q9.

Gate U10A transmits either the internal or external pulse train. Two pulse trains cannot appear at the input of U10A(1). U10A will always transmit whichever of the two pulse trains is present since the nonpulsed input will always be HIGH.

The 10 MHz detector U5B works in a similar manner to the external reference detector U5A. L_10MHz_OK is LOW whenever a 10 MHz reference exists at the output gate U10A.

The 10 MHz reference is distributed to the A5 Synthesizer Assembly, the MRC on the A3 Counter Assembly, and to the rear panel BNC connector A8J2 (10MHz Out) via 50-ohm line drivers U9A, U9B, and U9C. R51 and C36 form a 100 MHz low-pass filter that minimizes transmission of frequency components in the synthesizer's tuning range. The line drivers to the synthesizer and the MRC, U9A and U9B, are disabled in Standby when the +5V supply at the inputs of U10D drops to 0V.

A 1 MHz output is derived from the 10 MHz output of U10A through decade divider U6 and line driver U9D, and provided at the rear panel via BNC connector A8J3 (1MHz Out). R61 and C45 form a 50 MHz low-pass filter to reduce 10 MHz spikes on the 1 MHz output.

Operation is straightforward when only an internal timebase reference source is used. When there is no external reference, both the sine wave-to-TTL converter U4 and external reference detector U5A outputs are HIGH. Consequently, the internal 10 MHz reference signal passes through gates U10B and U10A to the output line drivers.

OVEN TEMPERATURE MONITOR. The oven temperature monitor circuit consists of Q5, CR1, and associated components. This circuit translates the oven temperature monitor voltage from the optional ovenized oscillator to a TTL signal (L_OVN_COLD) indicating oven status to the A4 microprocessor.

The OVN_TEMP input at P1A(44) is -1.5V when the oven is cold. This voltage is insufficient to break down 14V zener diode CR1; thus, Q5 is turned OFF and the L_OVN_COLD line is LOW. After the oven warms up, the OVN_TEMP line changes to -20.5V, causing conduction through CR1. Q5 is turned ON, and L_OVN_COLD is now HIGH.

VOLTAGE REGULATOR. The +5V UNREG and +15V UNREG supplies appear whenever the instrument is connected to the power mains (these voltages are not controlled by the

COUNTER/TIMER. The Counter/Timer circuit digitizes the length of the comparator's output pulse at U10(7) by counting the 40 MHz crystal oscillator output from U1(14). This circuit is essentially comprised of three counters.

The first counter, which includes both halves of U9, functions as a dual JK flip-flop, which least significant bits (LSB) control the module-ten synchronous counter (U15) of the Pseudo Random Phase Shifter circuit. Its J and K inputs are connected to the output of the interpolator (pin 7 of U10), and counting is enabled when U10(7) output is HIGH during the interpolator ramp discharge and charge.

The second counter, the upper half of U9 (i.e., U9 pins 1 thru 5), is a ripple counter with the J and K inputs set HIGH and the clock input connected to the first stage output. The output of the second stage is counted by one of the 16-bit counters in Timer U8. During averaging, the counters are not reset between each averaged measurement, the count in the LSB carries over into further measurements and is accumulated in the MSB.

The third 16-bit counter in Timer U8 is used as a timer to generate a holdoff signal (L_HOLD_OFF) for A14 Gate Board Assembly. Essentially, it functions as digitally programmable one shot. It is triggered off the start of the Stop Interpolator pulse (SPI) from U3(7), the stop pulse comparator. The L_HOLD_OFF signal goes to the A14 Gating Board Assembly to prevent the gate from opening before the interpolators and/or the A4 microprocessor is ready under high PRF conditions.

POWER SUPPLY REGULATOR. U7 provides a +3 volt supply (derived from the +5 volt line) to the MRC, the IF Input Switch circuit, and the Interpolator comparator reference. A test line (+3V TEST) goes to the Power Supply Test connector, A8J7(13), on the A8 Motherboard Assembly. Potentiometer R1 is used to adjust the +3V supply.

5-138. A4 Microprocessor Assembly

The A4 Microprocessor Assembly controls the overall operation of the instrument. This assembly receives instructions via the front panel keyboard or the HP-IB interface, and sends instructions and data to the front panel display, HP-IB interface, synthesizer, and counter circuitry to control the measurement.

As shown on Sheet 1 of *Figure 5-15*, the A4 Assembly consists of the following circuits:

- Microprocessor Unit (U1)
- 64K Byte Read-Only Memory (ROM), U8
- 8K Byte Random-Access Memory (RAM), U10
- Input Buffers (U18, U19, U20)
- Output Buffers (U11, U13, U14, U15, U16)
- Address Buffer (U7)
- Data Buffer (U6)
- Read/Write Decoder (U2, U4, U12)
- MATE Counter (U9)

MICROPROCESSOR UNIT. U1 is an NMOS 6803 microprocessor. All control functions of the A4 Microprocessor Assembly are performed by U1. The main tasks that U1 executes are as follows:

- Read from ROM
- Read from and Write to RAM
- Write to Output Buffers
- Read from Input Buffers
- Transfer data over the two on-board bidirectional data buses

Microprocessor U1 contains an 8-bit CPU, 64 bytes of power-down RAM, 64 bytes of nonpower-down RAM, three 8-bit I/O ports, one 5-bit I/O port, clock generating circuitry, a programmable timer, and interrupt logic.

U1 performs all I/O transfers by reading and writing to memory (memory-mapped I/O). Four latched Static Output Ports (SOPRT1, SOPRT2, SOPRT3, SOPRT4) are used for controlling other assembly boards, and three Static Input Ports (SIPRT1, SIPRT2, SIPRT3) are used to sample circuit conditions in the instrument. Microprocessor U1 performs bidirectional data transfer between other assemblies via its 8-bit Data Port 1 (pins 13 – 20) and 5-bit Data Port 2 (pins 8 – 12).

Microprocessor U1 activity begins with the Reset sequence, after the +5V supply is first turned on. On the rise of the +5V supply, processor activity is held back by a logic LOW on the L_μP_RST, U1(6). The L_μP_RST line, which comes from the Power Supply Control circuit on the A1 Assembly, goes logic HIGH after a minimum delay of 100 ms, and then processor execution begins. The 100 ms delay enables the clock circuits in the microprocessor to stabilize.

At power-up, the microprocessor is latched into its proper operating mode by the setup conditions at U1(8-10). The latching of the operating mode is explained in more detail in the paragraph titled "Latching the Operating Mode", but for now it is only necessary to know that once the operating mode is set, the processor reads from a preset ROM address (0FFFE;0FFFF). The addressed memory location contains the starting address of the operating program.

In the following paragraphs, the basic tasks which the processor performs are described in detail, followed by a description of the various auxiliary circuits on the A4 Assembly. Refer to *Figure 5-21. A4 Microprocessor Assembly Schematic Diagram.*

ADDRESSING AND DATA TRANSFER. Microprocessor U1 uses an 8-bit multiplexed address/data port (A/D 0 to A/D 7). This port is demultiplexed by latch U7 to provide the lower 8 bits of the on-board address bus (A0-A7). The upper 8 bits of the address bus (A8-A15) come directly from U1(pins 22 – 29). The required address lines are applied directly to ROM U8 and RAM U10 (lines A0-A15 for ROM, lines A0-A11 for RAM). The lower 8 bits of the address are latched by Address Bus Buffer U7 on the falling edge of the Address Strobe (AS) pulse from U1(39), causing the address to be applied to the ROM and RAM for the rest of the memory access cycle.

The multiplexed address/data (A/D0 – A/D7) lines are buffered by Data Bus Buffer U6, which is a bidirectional transceiver, to provide the on-board 8-bit data bus (D0 – D7). The level at the EN1 input at U6(1) determines the direction of the data transfer. U6 outputs are enabled by the rising edge of a delayed and inverted EPLUS10 delay signal (INV_EPLUS10), so that the U6 outputs are three-stated during the address portion of the multiplexed bus cycle.

READ FROM ROM. ROM U8 is an NMOS 64K byte device. U8 has two enable lines, 16 address lines, and 8 three-state data lines. U8 is enabled when both the L_ROM_EN (enable) input at U8(22) and ~CE input at U8(20) are logic LOW. (Since U8(20) is tied LOW, U8(22) L_ROM_EN is the line that actually enables ROM U8.)

When the L_ROM_EN signal at U8(22) is active LOW, the data at the addressed location of U8 appears at the data lines. The data is held until U8(22) goes HIGH. The microprocessor reads the data on the bus on the falling edge of the system clock. After U8(22) goes HIGH and the data lines are three-stated, the ROM goes into its standby low power dissipation state.

READ FROM AND WRITE TO RAM. U10 is an 2K byte CMOS static RAM device. U10 has four enable lines, 12 address lines, and 8 bidirectional data lines. The CS1 (Chip Select 1) input at U10(20) is tied to ground. The EPLUS30 delay signal from the Delay Line, U2(10), connects to to the ~CS2 (Chip Select 2) input at U10(26) to ensure the proper timing of when the data is read from or written to RAM U10. The L_RAM_RD signal from PAL U14(14), which connects to the ~OE (Output Enable) input at U10(22), is always HIGH during a write. The ~WE (Write Enable) signal at U10(27) is an active LOW during a write. The ~WE (L_RAM_WR) signal comes from NAND gate U3D, which inputs are the H_RAM_WR signal (active HIGH during the write) and the system clock (ECLK). Once RAM U15 is enabled, data on the I/O lines at U15(11-13, 15-19) are stored into memory on the rising edge of the ~WE signal. This completes the write cycle to RAM.

The read from RAM cycle is identical to the read from ROM cycle, except the L_RAM_RD signal to U10(27) via PAL U4(14) enables the RAM to output data during the read operation.

The read/write (H_RD_L_RD) signal from U1 is used to indicate to PAL U4(14) to make an active LOW signal during the read cycle; whenever this signal (L_RAM_RD) at at U10(22) is LOW, the H_RAM_WR signal at U4(15) is also LOW. The LOW at U4(15) causes U3D(11) to go HIGH to ensure that RAM U10 is not enabled during the address portion of the multiplexed bus cycle.

READ FROM INPUT PORT. Status condition signals from other circuits are received at the SIPRT1, SIPRT2, and SIPRT3 input ports, using 8-bit latches (U18, U19, U20) with three-state outputs, as input buffers. Reading from an input port is similar to reading from ROM, but only one enable is needed for each input buffer, at U18(1), U19(1), and U20(1). Read and Write Decoder U12 outputs (L_PRT1_RD, L_PRT2_RD, and L_PRT3_RD) enable the corresponding input buffer based on the address range (A2 to A3) of U12's input (pins 1 and 2); the address range comes from Address Bus Buffer U7 (pins 17 and 16). When the enable signal at pin 1 of an input buffer is LOW, the data at the corresponding input buffer is transferred onto the on-board data bus (D0 – D7). The microprocessor reads this data, via Data Bus Buffer U6, on the falling edge of the system clock (ECLK), and decoder U12 disables the input buffers before the next bus cycle begins.

WRITE TO OUTPUT PORT. Control signals (the outputs from the Input Buffers) for the other circuits or assemblies in the instrument are sent through buffer U17 and transferred to the four Output Buffers (U16, U13, U14, and U15). Writing to an output port is similar to writing to RAM. The output lines L_PRT1_WR, L_PRT2_WR, L_PRT3_WR, and L_PRT4_WR from Read/Write Decoder U12 connect to the enable inputs (pin 1) of Output Buffers U13, U14, U15, and U16, respectively. These four L_PRTn_WR outputs are used to latch the data on the output lines (SOBUS0-SOBUS7) of Output Data Latch U17 to the inputs of the Output Buffers. Data transfer through each output buffer is enabled only when the corresponding enable signal from Decoder U12 (pin 15, 14, 13, or 12) is active LOW. The outputs of U16, U13, U14, and U15 are totem outputs, and thus are always active.

READ FROM AND WRITE TO DATA PORT. Microprocessor U1 uses two of its ports as static data buses for data transfer to and from other assemblies. Data Port 1 (pins 13 through 20) is an 8-bit bidirectional port which is used for all data transfers directly to and from the processor via the DBUS 0-DBUS 7 lines. Three lines of the 5-bit Data Port 2 (pins 8 through 12) are used for handshaking with the HP-IB processor on the A11 HP-IB Interface Assembly. These three handshake lines (IB DVAL, IB DREC, IB DDIR) provide synchronization between the two asynchronous processors. The fourth Data Port 2 line (L KB IRQ) is used to detect an interrupt caused by a front panel key being pressed. The fifth of Data Port 2 line is not used.

The pins of the Data Port 1 (DPRT1) and Data Port 2 (DPRT2) are individually programmable to be either inputs or outputs; at any one time, some pins may be inputs, and others may be outputs. A +5V pull-up via resistors R10 and R11, and resistor network R7, makes the DPRT1 and DPRT2 lines high level when configured as inputs. When configured as outputs, DPRT1 and DPRT2 lines are totem pole outputs. A read to, or write from, these ports is controlled entirely within Microprocessor U1.

READ AND WRITE DECODING. This circuitry is comprise of Delay Line integrated circuit U2, PAL U4, and Decoder U12. Its purpose is to ensure proper timing of all read and write functions of the A4 Microprocessor Assembly by controlling the read and write enable lines of the RAM, and the enable lines for all the input and output buffers.

Microprocessor U1 provides a single system clock output ECLK at U1(40). A number of delayed and/or inverted clock signals are derived from the ECLK by 50-Nanosecond Delay Line IC U2, inverter U3C, and PAL U4. The ECLK system clock at U1(40) is a 2 MHz square wave which is active HIGH for data valid, and active LOW for address valid. Individual devices on the A4 Assembly are enabled based on two things: the Read/Write Decoder U12 and PAL U4, and a precisely timed edge of the system clock (ECLK). The decoding outputs of U12 and U4 have many propagation delays, and are used only for device selection, not device deselection.

The delayed ECLK signals (EPLUS30, EPLUS20, EPLUS10) generated by the 50-nanosecond Delay Line IC guarantee the correct timing of the read and write functions on the A4 Assembly.

The 30 nanoseconds (EPLUS30) version of the ECLK signal from U2(10) is used to provide required data setup and hold times for RAM U10.

The L_RAM_RD signal, U4(14), is used to read from RAM U10 while H_RAM_WR is LOW; hence, the L_RAM_WR signal, U3(11), is used to write to RAM.

The L_IO_EN, U4(12), is used to enable Decoder U12. Decoder U12 outputs are used to enable the read and write of data from the Input Buffers (U18 – U20) and Output Buffers (U13 – U16).

The output signals from Decoder U12 (pins 15, 14, 13, and 12) are used to write to the Output Buffers (U16, U13, U14, and U15).

WRITE TO SYNTHESIZER ASSEMBLY. The A5 Synthesizer Assembly is programmed via a separate 8-bit latch, U11, in order to isolate the A5 Assembly from microprocessor noise. A write to the synthesizer is similar to writing to one of the SOPRT outputs, except the latching signal (SYN LCH) comes from output buffer U13(16) via the A8 Motherboard Assembly. The U11 output latch is always enabled by a ground connection at U11(1).

This completes the explanations of the basic tasks performed by A4 Microprocessor Assembly. The following paragraphs describe auxiliary circuits of A4 Assembly; such as, the MATE Timer, the 6803 Microprocessor operating mode latching, the interrupts, and the power supply decoupling circuitry.

MATE TIMER. Mate Timer U9 is designed for use with the 6803 Microprocessor (U1) and is installed to meet timing requirements for Option 700 CIIL Interface (MATE). The timer has internal logic to decode the ECLK and H_RD_L_WR lines, and has two enable inputs. One enable (CS1) is tied HIGH through R13. The second enable (CS0) is the L_MATE_EN line, which comes from PAL U4. The output of the timer counter 3 at U9(6) is routed to the input of counter 2 (U9 pin 4), and the output of counter 2 at U9(3) is routed to the input of counter 1 (U9 pin 28). The data to and from the Timer U9 is enabled identically to reading and writing from RAM.

CRYSTAL CLOCK. Microprocessor U1 has an internal clock generating circuit which requires only an external 8 MHz clock and the proper load capacitance (C1, C2). The 8 MHz crystal frequency is divided by four to give a system clock (ECLK) of 2 MHz.

INTERRUPTS. Two interrupt inputs to the processor are available in addition to the L_μP_RST input: the L_KB_IRQ and the IB_DDIR inputs.

The IRQ1 input at U1(5) is an active LOW maskable interrupt enabled by either HP-IB communication, or the front panel keyboard when the operator presses a key. Both interrupts are logically NANDed together by U3A, and the output (L_IRQ) at U3B(6) is applied to the single IRQ1 input at U1(5). When the processor is interrupted, it scans the DPRT2 lines to determine whether the L_KB_IRQ line at U1(8), or the IB_DDIR line at U1(12) has gone LOW, and executes the appropriate program based on which interrupt occurred.

LATCHING THE OPERATING MODE. The 6803 (Microprocessor U1) is basically a 6801 single-chip microcomputer operating in Mode 2. U1 operating mode is established on the rising edge of the L_μP_RST signal from the A1 Assembly. Resistor R9 and capacitor C13 produce a ramp input at U1(6). Diodes CR2 and CR3 are held LOW by the L_μP_RST line (the logic low level here is 1.5V dc maximum), and the Microprocessor U1 reads DPRT2 at U1(8,9,10) for the operating mode. The levels read by U1 are 010 (binary 2), which is operating mode 2. After the L_μP_RST line goes HIGH, CR2 and CR3 have no effect and DPRT2 operates as a bidirectional data port.

output at U7(4) and clocked by the Q3 output at U7(3). The flip-flop's Q0 and Q0 outputs at U7(15,14) have the same frequency as the Q3 and Q3 outputs, but with a 40/60% duty cycle and a phase allowing the maximum time for U3 to compute the modulus control for the next %50 or %51 cycle.

Low Frequency Programmable Divider (÷N). The F_{in} input (CMOS) at U3(3), which is ac coupled from the Q0 output at U7(14), is biased at about +2.4V by R37 and R38. The F_{in} frequency is 5.9 to 7.0 MHz for LO frequencies in the 295 to 350 MHz range, being approximately the LO frequency divided by 50. The % N counter inside U3 divides the F_{in} frequency down to 100 kHz (when phaselocked). N is an integer between 59 and 70 for LO frequencies in the 295 to 350 MHz range.

Modulus Control (A/MC). The F_{in} input also clocks the A counter inside U3, which generates the Modulus Control (MC) signal for the ECL divider. The MC output is a signal to U7 and U10 to divide by 50 (MC high) or 51 (MC low). The MC signal is low for A cycles of F_{in}, then high for N – A cycles of F_{in} (A is always programmed to a value less than 50 and N is at least 59, so N – A is always positive). Thus the total divide number $Nt = (A \cdot 51) + [(N - A) \cdot 50] = (N \cdot 50) + A$.

When phaselocked, the LO frequency will be Nt •100 kHz, that is, $f_{LO} = [(N \cdot 50) + A] \cdot 100\ kHz = (N \cdot 5\ MHz) + (A \cdot 100\ kHz)$. The value of N acts as a coarse frequency control with 5 MHz steps, and the value of A acts as a fine frequency control with 100 kHz steps.

Switching back and forth between the two prescaling numbers (50 and 51) results in an average prescaling number which is a fractional value between 50 and 51. The switching between prescaling numbers is done at a 100 kHz rate. The total divide number, Nt, is always a whole number.

CMOS-to-ECL Converter. CR2, CR3, CR4, C10, C14, R9, R10, and R11 form a CMOS-to-ECL converter which changes the slow CMOS Modulus Control logic signal into a relatively fast ECL level signal. R9, R10, and R11 form a voltage divider which generates a +3.7V reference (ECL switching threshold, Vbb). CR2 and CR3 clamp the converter circuit output to one diode drop above or below this Vbb reference (approximately ECL logic levels).

C14 shifts the input switching thresholds of the converter circuit to levels near the beginning of U3's high-to- low and low-to-high transitions. Therefore, the converter circuit's input switching threshold is about +4.3V for high-to- low transitions and about +0.6V for low-to-high transitions.

PHASE DETECTOR. The phase detector inside U3 compares the 100 kHz signal from the reference divider, FR, with the signal from the internal %N divider, FV (100 kHz when phaselocked). The phase detector output (PD) is normally high impedance, but it pulses high or low at a 100kHz rate. In the high impedance state the PD voltage will be about +2.4V, determined by the integrator circuit (discussed later) which follows the phase detector. The PD pulses are low if FV leads FR and high if FV lags FR, and the pulse width is proportional to the phase difference between FV and FR. The phase-lock loop would normally drive the

phase difference to zero, however, the loop is biased for a slight phase lead in order to maintain circuit stability.

If the phase-lock loop is not phaselocked (FV not 100 kHz), the phase detector (PD) output of U3 will be pulsing high if the LO frequency is too low (FV < 100 kHz) or pulsing low if the LO frequency is too high (FV > 100 kHz). The pulse width will be much greater than in the locked state, and the pulse width will be time varying. The average of the PD output will have an ac component and a dc component. The frequency of the ac component is the difference between FV and FR. The dc component will tend to drive the phase-lock loop toward the locked state.

PHASELOCK INDICATOR. A red LED indicator at the top of the A5 Assembly lights when the synthesizer is not phaselocked. The LED flashes at a rapid rate (it may appear to be just dimly lit) during the signal acquisition sweep in Auto mode. The lock indicator is derived from the phase detector.

The Lock Detect (LD) output at U3(13) is normally high, and pulses low whenever the phase detector (PD) pulses low or high. CR8, R8C, R16, and C13 form a dual time constant circuit. When the synthesizer is phaselocked, the LD pulses are narrow and allow C13 to charge to nearly a +5V level; when the synthesizer is not phaselocked, the LD pulses are wide and discharge the C13 voltage to a relatively low level (about 1V). Comparator U2 compares the voltage on C13 to about +3V from R9-R11. The U2 output and transistor Q3 drive the DS1 LED. DS1 lights when the synthesizer is not phaselocked. The Q3 collector also goes to the test connector as the L UNLOCKED signal.

INTEGRATOR. The integrator circuit following the phase detector, consisting of U1 and associated components, performs many functions: biasing the phase detector, generating a low impedance to change the VCO, providing large loop gain at low frequencies for phase noise reduction, setting the step response of the loop, and helping to filter out ripple from phase detector pulses.

R7, C8, and R6 convert the phase detector voltage pulses into current pulses, and remove the high frequency components which are beyond the frequency range of the integrator. Operational amplifier U1 and feedback components C1, R1, and C3 integrate the phase detector current pulses. C1 is the integrating capacitor, and R1 helps to keep the closed loop response stable.

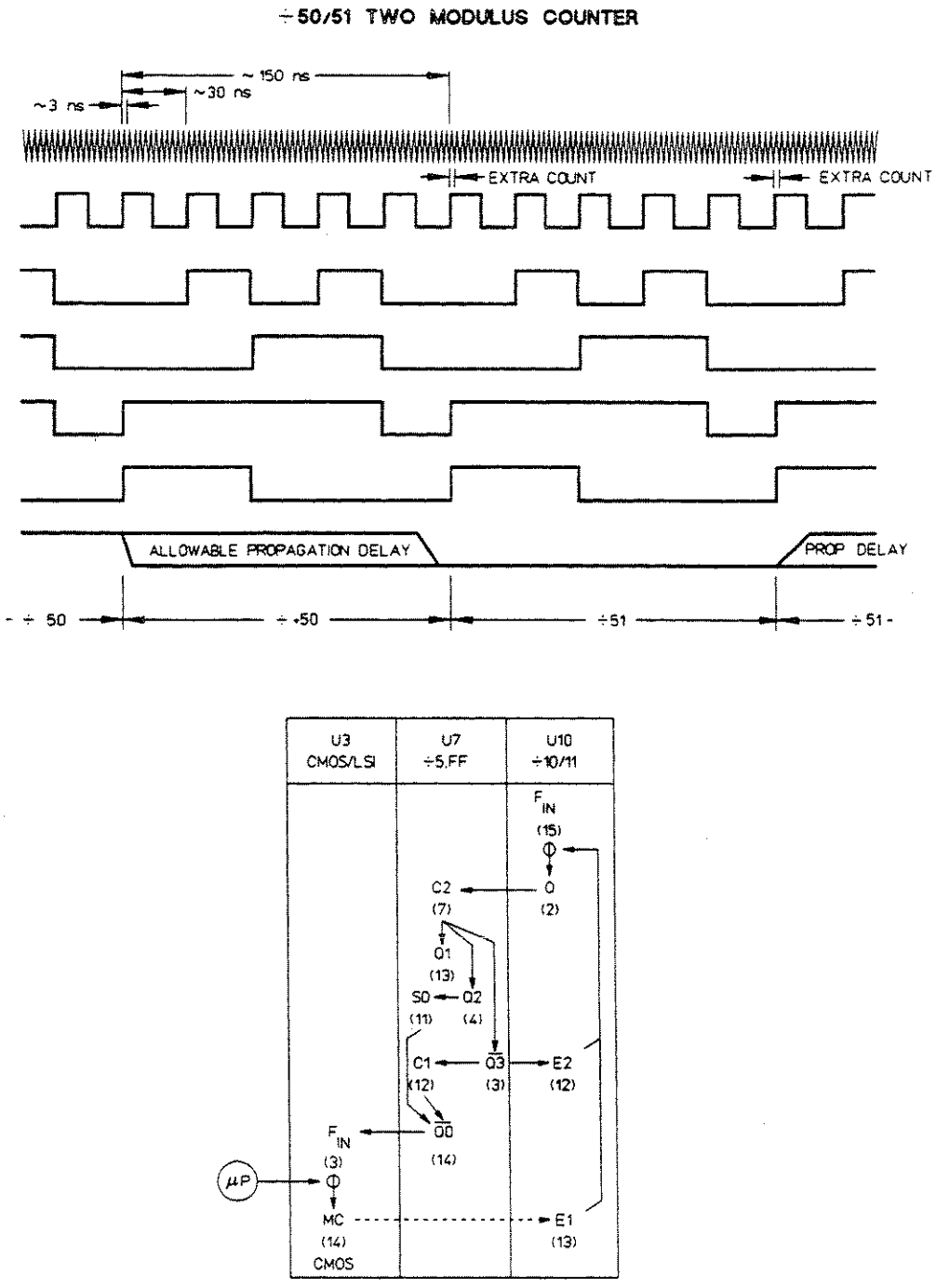


Figure 5-8. Two-Modulus Counter (divide-by 50/divide-by 51) Timing Diagram

The noninverting input at U1(3) is biased at about +2.35V dc by R8B, R4, and R8A. When the synthesizer is phaselocked, the inverting input is at the same voltage as the noninverting input. The voltage across R5 is the same as the voltage across R4 (about 0.3V dc). The current through R5 biases the phase detector so that, when phaselocked, the PD output of U3 will have narrow low pulses (20-100 ns).

When the synthesizer is not phaselocked, U1 will probably be saturated. Since U1 has no voltage gain in this condition, it cannot function as an integrator, and the inverting input will not be at the same voltage as the noninverting input.

LOOP GAIN COMPENSATION. The phase-lock loop gain tends to vary with LO frequency because of changing VCO tuning sensitivity and changing divide number in the programmable frequency dividers. In the 300 to 370 MHz range the two effects mostly cancel, giving an almost constant loop gain. Below 300 MHz the loop gain increases, requiring compensation to keep the phase-lock loop stable.

The loop gain increase below 300 MHz is compensated by detecting the integrator output voltage (VCO tuning voltage), and connecting resistance in parallel with R1. P-channel JFETs Q1 and Q2 are used to connect R3, or R3 and R2, in parallel with R1, as determined by the integrator output. When the U1 output voltage is more negative than about –4V, both Q1 and Q2 are off, and R1 determines the phase-lock loop gain. When the U1 output is between about –3.5V and –1V, Q1 is on (Q2 remains off), and R3 is in parallel with R1. When the U1 output is more positive than about –0.5V, both Q1 and Q2 are on, so R3 and R2 are in parallel with R1.

CLAMP AND LOW PASS/NOTCH FILTER. CR1 prevents the integrator output of U1 from being more positive than +0.7V (U1 current limits at 15 to 20 mA). After passing through series resistor R14, the tuning voltage is limited to lower than about +0.2V by Schottky rectifier CR6 to prevent forward biasing the varactor diode (CR13) in the VCO.

Both ends of series resistor R14 are accessible at the test connector through R17A and B as the PLL OUT and PLL IN lines. C22 and C23 low pass filter the signals to the test connector and help prevent interference pickup from the connector. The phase-lock loop can be monitored or influenced through the PLL OUT and PLL IN connector pins.

R14, L2, L3, and C39 form a low-pass filter with a cut- off frequency of about 10 kHz. C28 and C29 in parallel with the series combination of L2 and L3 form a notch in the filter response at 100 kHz to block any remaining ripple caused by phase detector pulses. C19 (with R14) provides additional filtering above 100 kHz. C20 shunts to ground any RF signal which may have leaked back through the filter from the VCO. C35 helps maintain C39's low impedance in the 10-100 MHz range.

VOLTAGE CONTROLLED OSCILLATOR (VCO). The VCO is a grounded collector, varactor-tuned Hartley oscillator covering approximately 250 to 410 MHz. Only the 295 to 350 MHz range is used in the synthesizer. The VCO can be turned off by removing the bias current via firmware control.

The VCO tuned circuit (resonator) consists of varactor diode CR13, C45, L10, C51, and stray series inductance and shunt capacitance. The capacitance of CR13 varies from about 2 pF at 20V reverse bias to about 20 pF at 0V bias. The negative tuning voltage is applied to the anode of CR13 through RF choke L9; the dc side of L9 is bypassed by C38. C45 isolates the tuning voltage from the voltage on the emitter of the VCO transistor,Q6, and limits the tuning range at the low frequency end.

The resonator current flowing through the inductance of a short PC line between C44 and Q6 emitter produces an RF voltage which is ac coupled by C44 to the base of Q6. This RF voltage across the base and emitter junction of Q6 produces an RF collector-emitter current which sustains the oscillation in the resonator. The nonlinearity of Q6 limits the VCO amplitude by making the collector-emitter current more impulsive (instead of sinusoidal) as the base-emitter signal voltage increases.

The output of the VCO is the RF voltage drop of the resonator current flowing through the inductance of a short PC trace between C51 and the grounded cathode of CR13. C51 isolates the dc voltage on the emitter of Q6 from this grounded output inductance.

DC bias for the VCO circuit is provided by R28, R17D, and R20. R28 and R17D form a voltage divider which biases the base of Q6 at about -10V. L8 and C37 present a high impedance to the base of Q6 at the oscillation frequency, while R27 prevents lower frequency oscillation by greatly reducing the Q of L8. The emitter current in Q6 is set by the voltage across R20.

Q5, CR11, R23, R22, and R21 allow the microprocessor or the service technician to turn off the VCO by removing Q6's emitter current. When the base of Q5 is pulled low, either by the L TEST 4 line from the A4 microprocessor (through CR12) or by the L LO OFF line from the test connector, the collector current from Q5 substitutes for the emitter current of Q6 in R20, reverse biasing CR11 and turning off the VCO.

RF AMPLIFIERS. The RF amplifiers amplify the 295-350 MHz signal from the VCO, limit the amplitude to give constant output level, split the signal into a main LO output and a PLL feedback path, and isolate the VCO from interference.

U6 is a monolithic differential pair of transistors (and 3 resistors). The emitter bias current in U6 is set by a resistor inside U6 in series with R30A. Since U6 is driven into hard limiting, its gain will depend on its input amplitude. The output signal at each collector is about a 20 mA peak-to-peak near-square wave of current. The small inductance of jumper W2 in series with the output to the main LO power amplifier improves the bandwidth.

Isolation Amplifier. The amplifier composed of common- base transistor Q7 and associated components isolates the digital dividers in the PLL feedback loop from the VCO and other RF amplifiers. Q7 also transforms the near-square wave of current from one output of limiter/isolation amplifier U6 into a near- sine wave of voltage at the clock (Fin) input of digital divider U10. The signal at the collector of Q7 is ac coupled to the clock (Fin) input of divider U10 and to R36. R36 is the main load on the isolation amplifier and also biases the

F_{in} input at U10(15) from the Vbb output at U10(14). The fundamental frequency voltage amplitude at U10(15) is typically about 1 Vp-p.

Power Amplifier. The RF power amplifier consisting of U9 and associated components amplifies the signal from one output of limiter/ isolation amplifier U6 to +14.5 dBm typical at the main LO output, which drives the A12 Microwave Assembly. U9 is a common-emitter feedback amplifier with +14 dB gain.

AUX A/B MULTIPLEXER. The synthesizer generates an auxiliary output used for automatic synthesizer and instrument diagnostics and self-test. The AUX multiplexer circuit allows the microprocessor to select one of four signals from various points in the PLL frequency dividers to send out via the AUX A and AUX B balanced output. This output goes to the MRC on the A3 Counter Assembly, the third stage of the IF amplifier chain on the A6 Amplifier/Detector Assembly, and to the middle stages of both the 1MΩ and 50Ω low frequency input channels on the A2 Low Frequency Input Assembly. During normal instrument operation none of the four signals is selected, so the AUX output is inactive. The multiplexer circuit is controlled by four dedicated lines from the microprocessor board, which are separate from the lines used to program the synthesizer frequency. One of the multiplexer control lines (L TEST 4) is also used to turn off the VCO for certain diagnostics.

The AUX multiplexer circuit consists of U8, resistor network R32, and power supply bypass capacitors C48 and C49. U8 is an ECL IC which has four 3-input OR gates whose outputs feed an internal 4-input NAND gate. Each of the four 3-input OR gates has inputs from a signal line and an active LOW control line (unused inputs are grounded). During normal instrument operation all four control lines are high, and the AUX output is inactive. In the test/diagnostic mode, one of the control lines goes LOW to pass the selected signal to the U8 output. Pull-up resistor network R32 allows the TTL control lines to drive the ECL inputs of U8. Pull-down resistors for the U8 outputs are mounted on the receiving boards.

The four control lines select the following signals for the AUX output:

L TEST 1: LO/10 (29.5-35.0 MHz specified, 25-41 MHz typical)
L TEST 2: LO/50 (5.9-7.0 MHz specified, 5-8 MHz typical)
L TEST 3: MC, Modulus Control (100 kHz, programmable duty cycle)
L TEST 4: 10MHz/R (usually set to 100 kHz, but programmable: $3 < R < 4096$);
(Note: L TEST 4 also turns off the VCO)

POWER SUPPLY. The +5V supplies for digital and analog circuitry are kept separate on the A5 Synthesizer Assembly (+5VD, +5VA). Although the two supplies come from the same voltage regulator on the A8 motherboard, they enter the A5 board at separate pins on the P1 connector and are provided with separate filtering components to prevent digital interference in the analog circuitry. The +15V supply is available at the P1 connector, but is not used.

The voltage regulator consisting of U5 and associated components regulates the –24V supply down to –20V to supply the VCO and integrator. The –20V regulator is turned off when the counter is in Standby mode.

U5 is a three-terminal adjustable voltage regulator that maintains a –1.25V difference between its output (Vout) and adjust (ADJ) terminals. Voltage divider R24 and R13D multiply this reference voltage so that U5's output terminal is at about –20V. CR9 and CR10 protect U5 from excessive reverse current surges in case either the –24V or –20V side is shorted to ground.

Q4, R13, and R18 turn off the –20V output of the voltage regulator in Standby mode (whenever the +5VA supply is not on). When the instrument is on, voltage divider R13 and R18 between +5VA and -24V holds the base of Q4 at about +2.3V; Q4 is therefore cut off and has no effect on the voltage regulator. When the instrument is in Standby, +5VA is off (0V), the –24V remains on, Q4 saturates and pulls up the adjust terminal of U5, and the output of U5 is reduced to about –1.35 volts, which is not enough to turn on the VCO or the U1 integrator. The –20V supply can be monitored on the test connector –20 OUT pin. R17C limits short circuit current and prevents interference pick-up.

5-140. A6 IF Amplifier/Detector Assembly

The main function of the A6 IF Amplifier/Detector Assembly is to amplify, filter, and level the incoming IF signal from the A12 Microwave Module and output the appropriate signal to be measured. To perform this, the A6 Assembly consists of the following seven major blocks (see Sheet 1 of *Figure 5-15*):

- AGC (Automatic Gain Control) Loop
- Schmitt Trigger
- Envelope
- Inband Detector
- Status
- Test/Diagnostics
- Miscellaneous Circuits (Inband Driver, Monitor Driver, and Sample/Hold Buffer)

Each of the above blocks are described in the following paragraphs. Refer to *Figure 5-23. A6 IF Amplifier/Detector Assembly Schematic Diagram.*

AGC LOOP. The AGC Loop block consists of several circuits as shown on Sheet 1 of the overall block diagram in *Figure 5-15*. These circuits are the Variable Attenuator, Amp 1, Low Pass Filter 1, Amp 2, Low Pass Filter 2, Amp 3, Buffer Amps, Envelope/AGC Detectors, Sample/Hold, Integrator, and the AGC Loop Reference. The AGC Loop block performs several tasks as listed below:

1. Amplifies the input signal.

2. Filters out undesired signals that come out of A12 Microwave Module.

3. Levels (by attenuation) the input signal to a desired level.

The IF signal from A12 Microwave Module enters A6 Assembly via cable W2 and immediately goes into U16 which is a 50-ohm variable attenuator. U16 controls the amplitude of the AGC Loop block. After U16, the signal enters RF amplifier AMP 1 (U15). U15 has a gain of approximately 19 dB. U15 drives the Low Pass Filter 1 which is a 50 ohm 7-pole elipitical filter. The cut off frequency is 175MHz. The filter is adjusted to have a zero (notch) at 200 MHz by tuning C56. The Low Pass Filter 1 is very important since it provides the greatest amount of attenuation of unwanted signals.

The signal then enters Amp 2 (U10) which amplifies the signal by approximately another 19 dB. U10 drives the Low Pass Filter 2 (LPF 2) which is a 4-pole Chebyshev 200 MHz, 68-ohm filter.

After the LPF 2 the signal is amplified by Amp 3 and buffered by the Buffer Amps. The active components in the Amp 3 and Buffer Amps circuits are the transistors in transistor array U5. AMP 3 is a differential amplifier with differential outputs U5E(11) and U5C(6). This amplifier provides approximately 5 dB of gain. The overall flatness is controlled by Amp 3. The Buffer Amps are emitter followers and are the RF output of the AGC Loop block.

The peak amplitude of the signal is detected by the AGC Detector, which consists of transistors U6D and U6E (of the five-transistor array U6), resistor R21, and capacitor C26. The DC signal is then sampled and held by U8 of the Sample/Hold circuit. The control of the sample sample is discussed in the Envelope Circuitry section.

The output of the Sample/Hold circuit goes into a summation node formed by resistors R60A and R60B of the Integrator circuit, which consists of U13C and it associated components. The level of the IF is compared at the R60A(2) and R60B(3) node to the AGC Loop Ref circuit output at U13B(7). This drives the Integrator circuit in the correct direction to level the loop. The Integrator circuit has two different time constants for the two different pulse-repetition frequency (PRF) ranges.

The AGC Loop Ref circuit generates the dc voltage or reference level that the IF level is compared. The dc signal is derived from the voltage reference regulator U14 and diode CR6. CR6 is used to eliminate any temperature dependencies in the AGC level.

SCHMITT TRIGGER. The Schmitt Trigger block which consists of U1, U2, and their associated components converts the analog IF signal from the AGC Loop block into a ECL level representation of the analog IF signal. To ensure that the frequency of the signal is not altered by the Schmitt Trigger block, the positive going hysteresis point (compare point) is set to zero volts. In other words, for positive going signal swings, the Schmitt Trigger block triggers at zero volts, making the Schmitt Trigger less sensitive to anomalies in the signal that could cause frequency errors.

U1 is a dual high-speed comparator, U2 is a RS flip-flop (or latch). The 68 ohms resistors R7A, R7B, R7C, and R7D terminate the output of the Buffer Amps circuit.

Both the IF signal from the emitter of U5B and the 180 degree out of phase or inverted version of the IF signal from the emitter of U5D drive the Schmitt Trigger circuitry. U5B drives the positive input of U1(8) where it is compared against the zero volts at the negative input, U1(7). Similarly, U5D drives the other comparator's positive input at U1(9) where it is compared against the negative input at U1(10), which has a dc voltage level of approximately 120 mv. This voltage at U1(10) sets the hysteresis level of the Schmitt Trigger block.

When the sine-wave input signal at pin 8 of comparator U1 is above zero volts, the output at U1(1) is an ECL high (~-0.9V) and U1(2) is an ECL low (~-1.75V). When it is below zero volts, the output of comparator U1(1) becomes an ECL low and U1(2) is an ECL high. The other half of comparator U1 operates the same, except the trigger point is 120 millivolts instead of zero volts.

The clock input at U2(9) is driven by the H_ENVELOPE signal of the Envelope Comparator circuit. When a H_ENVELOPE pulse is present U2 is enabled; that is, the outputs at U2 pin 15 (+IF_NEW) and U2 pin 14 (-IF_NEW) follow the set and reset pulses of the U5B and U5D, respectively. During the off time of the pulse, U2 is latch LOW, eliminating any possibility of an event occurring when a H_ENVELOPE pulse is not present. For CW latch U2 is always enabled.

ENVELOPE. The Envelope block consists of the Envelope Detector, Envelope Comparator, ECL-to-TTL Converter Logic, and Sample/Hold Control circuits. The main function of the Envelope block is to generate a envelope signal that can be used both on and off the A6 Assembly, and to generate a control signal for the Sample/Hold circuit.

The Envelope Detector circuit (U6B, U6C, C27, C40, L3, and R29) detects the envelope of the IF signal at the output of transistors U5B and U5D, which are the output of the Buffer Amps circuit of the AGC Loop block.

The Envelope Comparator circuit (U7, R30, R23, and C39) compares the outputs of the Envelope Detector and the Sample/Hold Buffer circuits to generate an envelope pulse (H_ENVELOPE) to the A14 Gate Board Assembly, and a signal (via the ECL-to-TTL Converter Logic circuit) to the Status block circuitry and the Sample/Hold Control circuit. The Sample Hold Buffer output, U13A(1), is fed through resistors R30 and R23, and drives

pin 10 of U7 (the minus input); this output becomes the reference input for the comparator U7. R30 and R23 set the trigger points and hysteresis for U7. The Envelope Detector output (the L3(2), C40, and R29 node) drives pin 9 of U7 (the plus input).

If the output of the Envelope Detector is higher than the reference level or voltage (generated by the Sample/Hold Buffer) at U7(10), U7(16) outputs an ECL high pulse (H_ENVELOPE) to the A14 Gate Board Assembly and to U9B where it is converted to TTL high. The ECL high pulse from U7(16) also disables U2 of the Schmitt Trigger block. The TTL output from U9B(13) drives RS Latch U19 of the Status block, and the two timers (U17A, U17B) of the Sample/Hold Control circuit. U17A is used to stretch the envelope signals that are less than 2μ seconds wide. The stretching is needed to allow the sample and hold to settle. U17B is used to detect missing pulses.

If the output of the Envelope Detector is lower than the referecnce level at U7(10), U7(16) goes to an ECL low; thus there is no envelope pulse sent to the A14 Gate Board Assembly. Simultaneusly, U7(15) goes to an ECL high. This ECL high is converted to a TTL high by U9B. This TTL high out at U9B(13) causes the output (pin 4) of Latch U19 of the Status block to indicate no pulse is present.

For pulse operation, the missing pulse detector U17B is repeatedly triggered, causing its output at U17B(10) to be HIGH. This allows the Sample/Hold circuit to be sampled for a input pulse and then held between pulses. During the negative cycle of the pulse-repetition frequency (PRF), U17B changes states. Thus, U17B(10) goes LOW, forcing the sample/hold signal at U8(5) of the Sample/Hold circuit to go HIGH. This HIGH signal enables the AGC Loop block to sample. This signal also triggers the mode latch, U19(4), of the Status block.

For CW operation, the missing pulse detector output at U17B(10) is LOW except for when the input signal is first applied. This puts the Sample/Hold circuit into a sample or track mode. U17B(10) will be HIGH until it has timed out.

Q4 and capacitor C77 are used to change the timing of the U17B. When the gate of Q4 is LOW, Q4 is OFF and C77 is not in the circuit. This mode is what is normally used; thus, in this mode U17B timing is set by capacitor C71 and resistor R64. When the gate of Q4 is HIGH, C77 is parallel with C71. This configuration is for the less than 50 Hz PRF mode.

INBAND DETECTOR. The Inband Detector block determines if the IF signal is between approximately 35 to 105 MHz. The Inband Detector block consists of five circuits. These circuits are the low-pass filter, the high-pass filter, the level comparator, the envelope detector, and the envelope comparator.

The two filters are both 5-pole, 0.1 dB ripple Chebyshev filters. The low-pass filter consists of C7, L20, C8, L21, and C17. The high-pass filter consists of C19, L22, C20, L23, and C82. The low-pass filter is in a "PI" configuration, and the high-pass filter is in a "T" configuration. Thus, for a total of ten poles of filtering only four inductors are used.

The level comparator consists of one half of comparator U4 (9,10,12,13,16,15), resistors R9 and R10, and capacitor C79. R9 and R10 set a reference level which the input is compared against. For signals above this level, comparator U4 toggles at the input frequency, turning ON the INBAND LED via the enevelope detector (CR5), envelope comparator (U4A), ECL-to-TTL Converter (U9A), Status latch U19(7), and finally the Status buffer U11D. For signals below the reference level set by R9 and R10, U4 does not toggle, turning OFF the INBAND LED.

The envelope detector is formed by CR5, C68, C80, R69, and C81. The envelope detector is a negative peak detector. C80, R69, and C81 form a 2-pole filter. The diode CR5 is temperature compensated by the base-to-emitter junction of the output transistor inside of comparator U4(15).

The envelope comparator is formed by the other half or U4 (1, 2, 4, 5, 7, 8), R5, and R6. R5 and R6 set the compare level and hysteresis. The compare level is about –0.7 volts, and the hysteresis is about 100 mV.

STATUS. The Status block consists of the Status latch U19, IF Present Detector U9D, and the Overload Detector U9C. From these outputs the A4 microprocessor can determine the status of the A6 Assembly; that is, the microprocessor can detect whether a signal is present or not present. The aforementioned circuits are described in the following paragraphs.

The Status latch U19 is a quad RS latch. The R (reset) pins of U19 are the driven input and the S (set) pins are used as the clear. The four latches are reset by the A4 microprocessor with the L_IF_BD_RST line.

The IF Present Detector consists of U9D, R38A, R38C, R39, and R48. This detector indicates whether or not there is enough IF signal for the A6 Assembly to function properly. The output at U9D(11), the L_IF_PRSNT line, is fed to the A4 microprocessor. When this line is HIGH, there is no IF present; as a result, all the other status lines have no meaning.

The IF Present Detector is driven from the Sample/Hold Buffer circuit. As the IF signal level is increased the Sample/Hold Buffer output at U13D(14) goes from a "large" positive voltage to a slightly negative voltage. When this output gets to +400 mV (600 mV minus input of –200 mV hysteresis) the IF Present Detector will indicate that an IF signal is present. This occurs around –40 dBm for an input signal at 770 MHz.

The Overload Detector consists of U9C, R38B, R38D, R40, R54 and U18C. This detector indicates when the IF is in an overload condition for CW signals, and if the IF signal is leveling from a positive step in input power.

The Overload Detector is also driven from the Sample/Hold Buffer circuit. As the IF signal goes beyond where the AGC Loop normally levels (this occurs at approximately 2 dB above the normal leveling point), the detector U9C(5) goes LOW. This LOW (L_OVLD_LCH) line is fed to the buffer U11A of the Status block to turn on the OVERLOAD LED, and to the A4 Microprocessor. U18C inverts the L_OVLD_LCH signal, resulting in a H_OVLD signal to the

Integrator circuit. The H_OVLD signal drives the resistor R59 in an overload condition. This causes the Integrator to ramp down and increase the attenuation of the Variable Attenuator circuit. This overload detection and compensation function keeps the AGC Loop from getting "stuck" in an overload state when suddenly driven with a large IF input signal.

TEST/DIAGNOSTICS. The Test/Diagnostics block consist of U12, U11E, Q1, and the other associated components. This circuitry is used to test, diagnose, and calibrate the A6 Assembly. U12 is a three-pin voltage regulator which supplies the voltage for AMP 1 and AMP 2 circuits. U12 output voltages is set to +6V by resistors R50 and R51. U12 also helps keep the power supply noise to AMP 1 and 2 to a minimum.

U12 can be shut off by U11E, which is an open collector driver. When U11E is driven LOW by control line L_IF_OFF from the A4 microprocessor, it pulls U12(1), the ADJ pin, to ground. This removes power from the AMP 1 and AMP 2 circuits. With the voltage removed or reduced, the AGC Loop is turned off.

Transistor Q1 is used as an RF switch. When control line L_IF_TEST from the A4 microprocessor is HIGH, Q1 is OFF; thus, it does not affect the AGC Loop. When the L_IF_TEST line is LOW, Q1 is turned ON. With Q1 ON, the test signal on the AUX_A input line is injected into the AGC Loop to test the A6 Assembly.

A6 MISCELLANEOUS CIRCUITS. There are three miscellaneous circuits on the A6 Assembly: the Inband Driver, the Monitor Driver, and the Sample and Hold Buffer.

Inband and Monitor Drivers. The Inband Driver circuit (U6A, R11, R12, and R13) and the Monitor Driver circuit (U5A, R14, R20, and C23) are transistor amplifiers that are in an emitter follower configuration. The main function of the drivers is to isolate what they drive from the Amplifier 3 (Amp 3) and the Buffer Amplifiers (Buffer Amps) circuits. The isolation is needed because at the output of the Buffer Amplifiers circuit is where the linear IF signal gets converted to an ECL signal. Frequency errors can occur if this point is disturbed when the signal is going through its zero crossing.

The bias for these amplifers (the Inband and Monitor Drivers) comes from AMP 3 bias point. To eliminate oscillation of the drivers, the base resistors R11 (for Inband Driver) and R14 (for Monitor Driver) are connected at the base of U6A and U5A, respectively. Both drivers are set up to have a 50-ohm output impedance. Resistor R13 in series with U6A output, sets the Inband Driver for a 50-ohm output impedance; and the parallel combination of resistors R19 and R20 sets the Monitor Driver for a 50-ohm output impedance.

Sample/Hold Buffer. The Sample/Hold Buffer consists of two amplifiers, U13A and U13D. Operational amplifier U13A and resistor R55C are used as a buffer amplifier for the low-pass filter (LPF) formed by resistor R55B and capacitor C57. This LPF removes digital feedthrough which is caused by the Sample/Hold control line.

U13D and its associated components form a summation amplifier. The summation amplifier adds the Sample/Hold positive voltage to the negative AGC Loop REF circuit voltage. When

the loop is leveled these two voltages should be equal in magnitude so that the output voltage should be "zero" volts. When no signal is present the output is positive, and when the loop is overloaded or leveling the voltage will be negative.

5-141. A7 Keyboard/Display Logic Assembly

The A7 Keyboard/Display Logic Assembly, which is part of the Front Panel Assembly, and shown on Sheet 2 of *Figure 5-15*, consists of two major sections: the keyboard circuit, and the display logic circuit. The keyboard circuit includes the keyboard matrix (S2-S21), a key encoder (U4) and microprocessor interface circuitry (U2C, U2D, U3, U5B). The display logic circuit consists of a synchronization buffer circuit (U1). The front panel POWER switch circuit makes up the remainder of the A7 Assembly. Ribbon cable W1 provides all connection between the A7 Assembly and the A8 Motherboard Assembly.

For the following paragraphs, refer to *Figure 5-24. A7 Keyboard/Display Logic Assembly Schematic Diagram.*

KEYBOARD CIRCUIT. The HP 5361B keyboard consists of 20 switches, S2-S21, for the front panel data and function entry. The CMOS key encoder, U4, scans the lines to the keys and, when a key is pressed, makes available a code related to the key's X-Y position in the matrix. Key debouncing is performed internally. The debounce timing is controlled by the capacitor C8 on the KBM input of the encoder, U4(7). Scan rate is controlled by C9 on the OSC input, U4(6). U4 contains internal pull-up resistors on columns 1 through 5 of about 1MΩ each, and additional pull-up is provided by external resistors pack R5.

Once the keypress has passed the debounce time, the DA (Data Available) output at U4(13) goes high. The DA signal is latched by flip-flop U5 to produce an interrupt signal for the A4 microprocessor. The output of U5 is buffered by NAND gate U2C, which sends the inverted interrupt signal (L KB IRQ) to the A4 Microprocessor Assembly. The DA signal also goes to the A4 microprocessor through buffer U2D as the L KB DAVL signal. The microprocessor uses the L KB DAVL signal to detect a key being held down for repeating. The U2C and D buffers block noise on the DA line which may cause spurious keyboard interrupts. The 5-line output of the U4 key encoder goes to tri-state inverting octal buffer U3, and then to the microprocessor via data bus lines DBUS 3 - DBUS 7. The active low L KB READ signal from the microprocessor enables the data transfer onto the bus, and resets the U5 flip-flop.

DISPLAY LOGIC CIRCUIT. The display logic circuit consists of buffer U1, and the L_DSP_SDA and L_DSP_SCL lines from the A4 microprocessor. The L_DSP_SDA and L_DSP_SCL lines via U1 buffers enables the microprocessor to interface with the A9 Display/Driver Assembly. When the L_DSP_SDA (Low Display Synhronization Data) signal goes LOW, it enables display data to be sent to the A9 Assembly. The data (DBUS 3 – DBUS 7) from the A4 Microprocessor Assembly, which enters the A9 Assembly through connector A8J10 via flat-ribbon cable W1, is accepted and displayed when the L_DSP_SCL (Low Display Synchronization Clock) signal goes LOW.

POWER SWITCH AND DC FILTER. POWER Switch S1 is a low-powered toggle switch. When in Standby, S1 is closed, connecting LSTBY and the cathode of DS1 to ground. This causes the STBY LED to light and most of the power supply to shut down. When set to ON, the POWER switch is open, allowing L STBY to remain high.

Both the +5V and +15V from the motherboard are filtered on the A7 board. The filtered +5V is used by keyboard-related circuits. Display-related circuits use both +5V and +15V. Cable W1 carries filtered +5V to power the backlight LEDS (in the A9 Assembly) for the display.

5-142. A11 HP-IB Interface Assembly

The HP-IB Assembly, shown on Sheet 2 of *Figure 5-15*, controls all HP-IB interfacing between the HP 5361B and an external controller. Commands from the controller are partially decoded and sent to the main microprocessor (A4U2), and output data from the main microprocessor is formatted and sent back to the controller.

Major components of the HP-IB board are the HP-IB processor (U5), two TTL logic IC's (U3,U4), and two transceiver IC's (U1,U2). The HP-IB processor U5 is internally programmed to control all HP-IB Interface functions and overall operation of the HP-IB board. Quad NAND gate U3 and quad S-R latch U4 are used to speed the detection and response of the HP 5361B to particular HP-IB status and control lines. The 3-line bidirectional bus transceivers U1 and U2 drive the 8 data, 5 control, and 3 handshake lines used over the HP-IB.

For the following paragraphs, refer to *Figure 5-25. A11 HP-IB Assembly Schematic Diagram.*

The 3870 microprocessor (U5) receives commands from the external controller, interprets them, and sends them to the A4 Assembly. It also receives measurement data from A4, formats it, and sends it out on HP-IB when addressed to talk. The bus protocol that performs these tasks is generated by software contained in the program ROM of the processor. The HP-IB processor has four 8-bit I/O ports, for a total of 32 I/O lines. The 16 lines of Port 1 and Port 5 and 1 line of Port 0 are used for data, control, and interface functions between the instrument and the external controller. The remaining 7 lines of Port 0 are used for data, control, and monitoring functions between the HP- IB Assembly and the rest of the instrument. All the lines of Port 4 are used for addressing and testing functions that can be set using Address Switch S1. The L uP RST signal from the power-up detection circuit on the A1 Assembly resets the HP-IB processor and the main (A4) microprocessor when the instrument POWER switch is set to ON.

The open-collector bus transceivers U1 and U2 each drive 8 of the 16 lines used in HP-IB, with an internal driver/receiver pair of buffer amplifiers for each line. Direction of data flow is controlled by Send/Receive inputs on each IC, U1(1,8,11,14,17) and U2(1,8,11,14,17). The SRQ line is set to a permanent Send mode, and the ATN line is set to a permanent Receive mode due to their respective Send/Receive inputs being tied to +5V. The IFC and REN lines

are set to permanent Receive mode due to their Send/Receive inputs being tied to ground. All other lines are switched by U5 or the external controller via U3 and U4.

NAND gate U3A also pulls the NDAC line low to start the handshake for the information which is sent from the controller. The other two handshake lines, DAV and NFRD, are driven directly by the HP-IB processor.

Quad latch U4 speeds the HP 5361B response by latching in the REMOTE ENABLE (REN) and INTERFACE CLEAR (IFC) signals. The HP-IB processor clears the latches within 1 ms after they have been set by sending a STROBE pulse from U5(7) to the active low inputs at U4B(6) and U4D(15). U3 and U4 together speed the response to the ATTENTION (ATN) signal. When ATN goes LOW, the interface immediately releases control of the HP-IB data lines and goes into the acceptor handshake mode. When IFC goes LOW, control of the data and the handshake lines is relinquished.

The HP-IB Assembly is provided with two +5V power sources from the motherboard: +5V CMC (Common Mode Choke) via J2(13), and the standard +5V via J2(14). The +5V CMC circuit (on the A8 Assembly) contains additional filtering elements and is used to provide Vcc to the A11 transceivers U1 and U2 to prevent digital signal noise from the HP-IB getting back to the A8 Power Supply circuit. The standard +5V, filtered by L1 and C4, provides Vcc for all other IC's on the A11 Assembly.

5-143. A12 Microwave Module (A12 Microwave Assembly/U1 Sampler)

The basic function of the microwave module, shown on Sheet 1 of *Figure 5-15*, in the HP 5361B is to down-convert microwave signals in the 500 MHz to 26.5 GHz region to the intermediate frequency (IF) region of the counter. The 30 to 175 MHz IF signal is amplified and detected by the A6 IF Amplifier/ Detector Assembly, and then counted by the A3 Counter Assembly.

To perform the down-conversion, the module receives a medium power local oscillator (LO) signal from the A5 Synthesizer board, as well as dc power (+13V, +5V, –5V) from the power supply circuit. The microwave module can be divided into three sections: the sampler driver, sampler, and the IF preamplifier.

For the following paragraphs, refer to *Figure 5-26. A12 Microwave Module Schematic Diagram.*

SAMPLER DRIVER (PART OF A12 ASSEMBLY). The sampler driver circuit on the A12 board is a medium power, class B power amplifier. The LO signal (295 to 350 MHz, +14 dBm) from the A5 Synthesizer board enters via connector J3 and is ac coupled to the impedance matching network consisting of L17, C28, C29, C21, and C22 to drive power transistor Q2. The inverted signal at the collector of Q2, amplified 10 dB, is ac coupled to the impedance matching network consisting of L15, C24, L14, and C19, and then goes to the sampler.

U1 SAMPLER. Hybrid sampler U1 is the heart of the down- conversion system. The medium power LO signal from the sampler driver section enters at pin 3 of the sampler. This signal drives a step-recovery diode (SRD) in the sampler which produces a very narrow voltage pulse. This pulse is used to control the sampling of the microwave signal entering the sampler RF connector J1. When a harmonic of the LO sampling frequency is close to the microwave input signal frequency, a signal within the IF frequency range is generated and sent to the IF preamplifier from the sampler.

IF PREAMPLIFIER (PART OF A12 ASSEMBLY). The IF preamplifier on the A12 board performs several functions, including: boosting the IF signal to a level less susceptible to RF noise, providing a flat IF response from 1MHz to 175 MHz to allow proper automatic amplitude discrimination, controlling dc bias current for U1's internal sampling diodes, converting the relatively high impedance of the sampler output to a 50Ω source impedance, and isolating the residual LO feedthrough signal and its harmonics from the IF signal. The IF preamplifier consists of eight stages: a bias/matching network, a buffer amplifier, two gain amplifiers, two low-pass filters, a PI (the Greek letter π) attenuator, and a frequency compensation network.

DC bias current through the sampling diodes (within the sampler) is controlled by resistor R7. The IF signal generated in the sampler is ac coupled through capacitors C9 and C12 to the impedance matching network consisting of L1 and R1. Emitter follower transistor Q1 translates the 1.5 KΩ sampler impedance to approximately 50Ω to match the input impedance of the following stages.

The IF signal is ac coupled to the first gain stage, U1. Amplifier U1 provides 16 dB of gain, set by bias resistor R3. Resistors R3, R5, and R6 form a PI attenuator network that controls the overall gain of the microwave module. Coupling capacitor C10 prevents R5 and R6 from affecting the bias current supplied to U1 by R3. The IF signal is then connected to the first low-pass filter stage consisting of L2, C4, L3, C16, and L4. Besides generally reducing the LO signal and its harmonics from the IF signal, the low-pass filter prevents the second gain stage from getting saturated by the relatively high-level LO feedthrough signal.

Amplifier U2 provides another 16 dB of gain. The bias current for the amplifier is supplied through inductor L7.

Capacitor C11 ac couples the signal to the second low-pass filter/matching network consisting of L5, C5, and L6.

Two of the power supplies for the A12 Assembly are switched supplies, +13 SW and +5V SW. The two supplies are turned off by the A4 microprocessor, via a microwave turn off circuit on the A1 Motherboard, when INPUT 2 is selected or when the "SLEEP" mode has been turned on via the HP-IB.

MICROWAVE MODULE RF SHIELD. The microwave module is contained in a metal case for two reasons: a) To shield the IF circuitry from the effects of outside noise sources, and

thereby improve instrument sensitivity, and b) to shield the rest of the instrument from the relatively high power LO signal which radiates off the sampler driver circuitry.

5-144. Option 006 Limiter

Refer to *Figure 5-9* for discussion of Microwave Limiter theory.

The Microwave Limiter uses a PIN diode (CR1) as a limiter. As high power (+20 dBm and greater) is applied, the PIN diode begins conducting. The I region of the diode stores charge. The stored charge does not allow the diode to turn off, shorting power to ground. Though the diode remains on during both the positive and negative half cycles of the input signal, the resistance across the junction is slightly greater in the normally reversed biased direction than in the forward biased direction. The inductor to ground is used to prevent a charge from the building up on the C1 and C2 blocking capacitors.

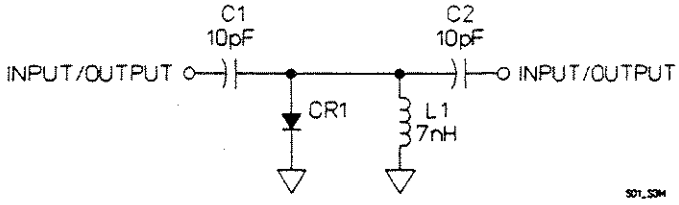


Figure 5-9. Limiter Schematic Diagram

5-145. A14 Gate Board Assembly

The main function of the A14 Gate Board Assembly, as shown on Sheet 1 of *Figure 5-15*, is to provide the A3 Counter Assembly with a gating or arming signal, enabling the A3 Counter Assembly to correctly count the carrier IF of a microwave pulse burst or continuous wave (CW) signal. All timing signals required for INPUT 1 measurements pass through the A14 Gate Board Assembly.

A14 Gate Board Assembly functions differently for pulse and CW measurements. During CW measurements, A14 divides the IF signal from the A6 IF Assembly by two before sending it to A3 Counter Assembly. The A4 microprocessor generated gate signal also passes through A14 to A3. During pulse measurements, A14 Gate Assembly decides when and where the measurement is made within a pulse. It also determines how long the gate must remain open during a measurement. The A14 Assembly along with A3 Assembly ensures that only valid measurements are made. These assemblies also function with each other to reduce the rate at which measurements occur so that the A3 counter and A4 microprocessor can correctly process the information gathered during the measurement.

The gating section has nine inputs and five outputs. The inputs include: +IF_NEW, -IF_NEW, ENVELOPE_DET, and L_IF_INBAND arriving from the A6 IF assembly; DATA BUS, CONTROL, and H_GATE arriving from the A4 Microprocessor Assembly; EXT_GATE_ARM arriving via the front panel GATE/ARM IN connector; and L_HOLDOFF arriving from the A3 Counter Assembly. The outputs are: EVENTS, ARM_MRC (H_GATE), and ENVELOPE_CTR routed to the A3 Counter Assembly; ENVELOPE_OUT routed to the rear panel PULSE OUT connector; and GATE+IF routed to the front panel SCOPE-VIEW connector.

The A14 Gate Board Assembly consists of four main blocks. These blocks are as listed below:

- Microprocessor Interface
- Gate/Event Generation
- Event Counter/Width Generator
- Gating and Arming

These blocks are described in detail in the following paragraphs. Refer to *Figure 5-28. A14 Gate Board Assembly Schematic Diagram.*

MICROPROCESSOR INTERFACE. The A14 Gate Board Assembly communicates with the A4 microprocessor via the Microprocessor Interface block. This block allows the A14 Gate Board to be programmed for different measurement modes such as CW or pulse, envelope measurements, and internal or external gate.

The Microprocessor Interface block is mostly comprised of the circuits that allow the A14 Gate Board Assembly to talk to the A4 Microprocessor Assembly. Transceiver U13 receives or sends data via the data bus (DBUS 0 – DBUS 7). U13 is always enabled because U13(19) is tied to ground, and the direction of data flow on the data bus is controlled by the

H_GTBD_WR signal from the A4 microprocessor. When the H_GTBD_WR signal is HIGH, the microprocessor writes or sends data to the A14 Gate Board through U13. When this signal is LOW, the microprocessor reads or receives data from U13.

The on-board data bus of the A14 Assembly is called GATEBD_D0 - GATEBD_D7. The on-board data bus supplies all the data to various circuits on the A14 Assembly. These circuits are the Command Latch (U12), the Event Input Latch (U2), the Event/Status Latch (U1), and the Timer (U3) of the Event Counter/Width Generator block. These circuit are selected by the 3-to-8 Decoder (U27). This decoder decodes the GTBD_RSC0 - GTBD_RSC2 lines from the A4 Microprocessor Assembly while the L_GTBD_EN line enables it. To avoid any glitches at the output of Decoder U27, the microprocessor ensures that the selected input lines change only when the decoder is not enabled (L_GTBD_EN equal HIGH).

Event Input Latch U2 holds the nibble (one half of a byte; i.e., four bits) for the 4-bit Event Counter (U19) as well as the four bits for the 4-bit Remainder Counter (U7). The outputs of U2 are always enabled, and the data is clocked by low-to-high transistion of the L_ENCNT_WR signal from pin 13 of Decoder U27. Resistor packs R2, R3, and R4 convert the TTL outputs of U2 to ECL levels. The ECL nibble signals for Event Counter U19 are EVT_NIB0 - EVT_NIB3, and the ECL nibble signals for Remainder Counter U7 are RMDR_NIB0 - RMDR_NIB3. These counters are described in details in the Event Counter/Width Generator section.

Command Latch U12 outputs, which are always enabled, set the A14 Gate Board into different modes. The command output from U13 is latched through U12 by the low-to-high transition on the L_CMND_WR output of Decoder U27. Resistor packs R39 and R40 convert the TTL level signals (L_TTL_GTGEN_EN, L_TTL_EXT_μP, and L_TTL_EXT_INT) into ECL level signals (L_GTGEN_EN, L_EXT_μP, and L_EXT_OR_INT, respectively).

The L_GTGEN_EN signal enables the Gate Generation circuits. (The Gate Generation circuits are disabled when CW frequency is being measured.) The L_EXT_μP and L_EXT_OR_INT signals select the various gating modes of the A14 Gate Board. The following table describes how each gating mode is selected:

SIGNALS		DESCRIPTION
L_EXT_μP	L_EXT_OR_INT	
0	0	Selects External gate for the measurement.
0	1	Selects Processor gate for the measurement.
1	0	Selects the Internal gate for the measurement.
1	1	Select the Diagnostics and Calibration gate.

The other three outputs from Command Latch U12 are the H_ARM_MODE, L_TTL_E_DIS, and H_8254_O_SEL signals. The H_ARM_MODE signal selects the ARM mode. The L_TTL_E_DIS signal disables the envelope signal going to the A3 Counter Assembly. The

H_8254_O_SEL signal selects the output "OUT0" of Timer U3 (8254 counter chip) for the Gate Generation circuits.

Event/Status Latch U1 is the buffer which the A4 microprocessor reads to get the least significant nibble of Event Counter U19. It also gives the status of various faults on A14 Gate Board. The following table describes the least significant nibble and the various faults:

LATCH INPUT	DATA BUS (A14 ON-BOARD BUS)	DESCRIPTIONS
E_BIT0 – E_BIT3	GTBD_D0 – GATE_D3	The least significant nibble for the Event Counter in case of External gate.
GATE_FAULT	GTBD_D4	Gets set if the gate close on or after the last pulse/event in the burst.
INBND_FAULT	GTBD_D5	Gets set if the signal goes out of band during External gate.
ARM_FAULT	GTBD_D6	Gets set if the next pulse after being armed is out of band.
L_SIG_INBND	GTBD_D7	Gets set if the signal is within band while making a measurement in the Armed or External Gate mode.

Timer U3 of the Event Counter/Width Generator block houses three 16-bit counters. Two of these counters are used for gate generation while one is not used. U3 is programmed via the on-board data bus (GTBD_D0 – GTBD_D7), and it is selected by the L_8254_SEL signal out of Decoder U27. The address lines (MRC_REG0, MRC_REG1), the read control line (L_MRC_STB), and the write control line (H_MRC_READ) are shared between the MRC (U5) on the A3 Counter Assembly and the Timer U3 on the A14 Assembly. However, the active polarities are different on A14 Assembly. Both the L_MRC_STB and H_MRC_READ signals are LOW when reading from Timer U3. L_MRC_STB is HIGH and H_MRC_READ is LOW when writing to Timer U3. All of the address lines and controls to Timer U3 are driven by the A4 Microprocessor Assembly.

GATE/EVENT GENERATION. This circuit generates the gate synchronous with the incoming IF signal. The timing of these two signals is critical for the counter's measurement process. During Internal Gate mode, the Gate/Event Generation block opens the gate synchronous with the second IF pulse and closes the gate when signaled by the Event Counter/Width Generator block. In External Gate mode, it opens and closes the gate with the external gate signal.

This block is the core of the A14 Gate Board Assembly, since it produces the gate for the measurement of the pulsed frequency. The pulsed frequency measurements and the calibration/diagnostics mode use the most of A14 Gate Board circuits. In CW mode, the A14 Gate Board is used minimally. The Gate/Event Generation circuits are mostly disabled as the measurement is performed with the gate (H_GATE) generated by the A4 Microprocessor

Assembly. (The Event Counter/Width Generator block is also not used in the CW mode.) During envelope parameter measurements, the Gate/Event Generation and Event Counter/Width Generator circuits are also not used. The following paragraphs describes how the Gate/Event Generation block works with both CW frequency and pulsed frequency measurements.

CW Frequency Measurements. For counting CW frequency, the incoming IF signal is divided by two and sent to MRC U5 on the A3 Counter Assembly to be counted. The firmware (ROM) on the A4 Microprocessor Assembly adjusts the reading to get the correct IF. The following paragraphs describes in detail how the circuitry measures CW frequency.

The microprocessor writes the command, via Transceiver U13, into Command Latch U12 to disable the gate generation logic signal (L_GTGEN_EN) and to disable the envelope signal going to the A3 Counter Assembly. The envelope signal is disabled by a LOW L_TTL_E_DIS signal to U28B(5) of the Gating and Arming block circuitry which causes the ENV_CRT signal out of U28B(6) to go LOW. This LOW disables interference with the CW frequency measurements.

The microprocessor also sets the A14 Gate Board to the CW mode by making L_CW_MODE signal LOW. This causes the outputs of U5(4), H_IN_CW, to go HIGH, and U5(2), L_IN_CW, to go LOW. Thus, these true conditions reset Meas Qual flip-flop (U10A), and set Event Gate flip-flop (U20B). The low L_CW_MODE signal also forces the output at U21(14) to LOW, thus the L_OK signal (wired-OR with U10 pin 2) is forced LOW. This L_CW_MODE signal also causes the L_WIDTH_MODE to be HIGH through U18(7).

L_IN_CW, U5(2) being LOW forces the set input to the Synch1 flip-flop (U10B) to HIGH. Effectively, the L_Q_ARM signal at U10(14) and the L_E_GT2 at U20(14) are forced LOW all the time, causing U22(3) and U21(6) to be LOW, respectively. The LOW signals at U22(3) and U21(6) causes the wired-OR line (H_EVENT_GEN) to follow the output of U21(3). U21 now acts as an inverter for P_EVENT (Q output of the Event Gen flip-flop, U34). U34, therefore, acts as a divide-by-2.

The Differential Input Receiver (U32) of the Gating and Arming block converts the differential IF signals (+IF_NEW and -IF_NEW) to single-ended IF which then is buffered for fan-out and for maintaining better timing accuracy. One of the buffered output, IF3 from U32(3), clocks Event Gen F/F U34 of the Gate/Event Generation block. The output at U34(3), EVENTBAR, is then inverted by U33 and sent out as the EVENTS signal to the A3 Counter Assembly. The frequency of the signal on the EVENTS line is half that of the IF.

The microprocessor has to generate the H_GATE signal for the MRC to take a measurement on the A3 Assembly.

Pulsed Frequency Measurement. As mentioned in previously, pulsed frequency measurements use most of the A14 Gate Board circuits. There are three different modes of operation in the pulsed mode as shown below:

1. Internal Gate mode
2. External Gate mode
3. Armed mode

In Internal Gate mode, the gate opens on the second pulse in the IF burst and closes after counting a preprogrammed number of pulses in the A3 Counter Assembly. The A14 Gate Board generates two narrow pulses to correspond with opening and closing of the gate on the EVENTS line (pin 2 of U33) to the A3 Counter Assembly. The MRC (U5) on the A3 Assembly then measures the time elapsed for between opening and closing of the gate. The ROM on the A4 Microprocessor Assembly divides the preprogrammed number of events (E) by the time (T) that the gate was open to get the frequency. In reality, the measurement does not exactly happen on one burst but multiples of the bursts.

In External Gate mode, the gate is opened and closed with the external gate signal synchronized to the incoming IF. The counting circuits, which in the Internal Gate mode were preprogrammed with the number of events that the gate should remain open, now count the number of pulses while the gate is actually open. Two pulses on the EVENTS line (pin 2 of U33) are still produced to represent opening and closing of the gate. The firmware reads the number of pulses that were accumulated during the time the gate was open and divides it by the time the gate was open (as measured by the MRC on the A3 Assembly) to get the frequency.

In armed mode, the high-to-low transistion on the EXT_IN input is fed through U16B and sets a flip-flop which allows the measurement to take place with the internal gate. The measurement always waits for the active transition on the gate or EVENTS line (pin 2 of U33), and the measurement does not depend on the width of the external gate and arm pulse from the GATE/ARM IN front panel connector.

INTERNAL GATE MODE. To place the A14 Gate Board Assembly into the Internal Gate mode, the firmware of the A4 Microprocessor Assembly has to send the following command word to Command Latch U12:

SIGNAL NAME	VALUE	EXPLANATION
H_ARM_MODE	0	Not in ARMed mode.
L_TTL_E_DIS	0	Envelope always disabled for frequency measurements.
L_TTL_GTGEN_EN	0	Enable the gate generation circuits.
L_TTL_EXT_μP	1	Select Internal gate.
L_TTL_EXT_INT	0	Select Internal gate.
H_8254_O_SEL	X	Depend on the gate width programmed. Explained later.

The A4 Microprocessor Assembly also sets the L_CW_MDE line to HIGH for pulsed frequencies. This line is fed to U5(5) of the Gating and Arming block, causing U5(4), H_IN_CW, to be LOW and U5(2), L_IN_CW, to be HIGH. This high L_IN_CW signal causes the output U21(3) of the Gate/Event Generation block to not affect the H_EVENT_GEN line. The set input (pin 12) of Synch1 F/F U10 follows the L_EXT_STR line through U9(9). It also removes the reset from the Meas Qual F/F U10(4), and removes the set from Event Gate F/F U20(12).

The command word from the microprocessor disables the ENV_CTR from going LOW to the A3 Counter Assembly. This prevents the interference with the frequency measurements. The low H_ARM_MODE line at U12(2) of the Microprocessor Interface block causes the H_ARMED output of U26A(5) of the Gating and Arming block to be always HIGH.

The L_EXT_μP and L_EXT_OR_INT signals (which in the internal mode are HIGH and LOW, respectively) are select lines for Start/Stop MUX U8. U8 outputs — H_STARM, U8(2) and L_STARM, U8(15) — will follow the ECL_HIGH signal at U8(4), and the L_CLOSE_GATE signal at U8(12), respectively; that is, the output signal H_ARM of U9(2), will follow L_SPARM because H_STARM is always HIGH. MUX U8 select lines also cause the H_EXT_EN signal at U31(3) of the Gating and Arming block to be LOW. This forces the L_W_MDE signal at U18(7) of the Event Counter/Width Generator block to be always LOW as all three inputs to the U18 are LOW.

Assuming that every thing is in steady state and proper initial condition, here is what happens when the IF burst is input to the A14 Gate Board Assembly. Initially, the following states for each signal of interest is as follows (The last paragraph of this Internal Gate mode section describes how this initial condition is achieved between every pulse burst):

SIGNAL	IC	STATE
L_CLOSE_GATE	U23(15)	1
L_Q_ARM	U23(14) or U10(14)	1
H_SYNC_ARM	U10(15)	0
L_E_GT2	U20(14)	1
H_E_GT2	U20(15)	0
L_PLD_EN	U20(2)	0
L_E_GT1	U20(3)	1
L_EOW	U7(4)	1

As the L_CLOSE_GATE signal goes HIGH, the L_SPARM and hence H_ARM signals go HIGH. The H_EVENT_GEN signal, which is a wired-OR of three different outputs — U22(3), U21(3), U21(6) — is LOW. The very first IF event in the burst from the output of Differential Input Receiver U32 at pin 15 (IF2) clocks the high H_ARM signal into Synch1 F/F U10(11), causing the H_SYNC_ARM signal at U10(15) to go HIGH and the L_Q_ARM

signal at U10(14) to go LOW. This causes the signal at U22(3), H_EVENT_GEN, which is the D-input to Event Gen F/F U34 to go HIGH.

The high H_SYNC_ARM clocks the status of the L_ECL_MEAS_OK line into Meas Qual F/F U10(7). The L_OK signal out of U10(2) will be LOW if the L_ECL_MEAS_OK is LOW; otherwise, it will be HIGH, keeping Event Gen F/F U34 in its reset state. The L_ECL_MEAS_OK will be LOW only if H_ARMED, H_GATE, and L_HOLDOFF are all HIGH. These three signals control the rate at which the measurements are taken. H_ARMED is always HIGH unless the A14 Gate Board is in Armed mode. The microprocessor controls the rate of measurements by the H_GATE signal. Since the microprocessor may take more time to bring the H_GATE line LOW (inactive) than the "off" time of the incoming pulse bursts, the A14 Gate Board may initiate another measurement even though the A3 Counter Assembly may not be ready. The L_HOLDOFF signal from the A3 Assembly will prevent the A14 Gate Board from making further measurements. For a first measurement, the L_HOLDOFF signal is HIGH. When the microprocessor decides to take a measurement, it will make H_GATE go HIGH, causing the L_ECL_MEAS_OK signal to be LOW. The rising edge of H_SYNC_ARM clocks a LOW into Meas Qual F/F U10(7), causing L_OK to be LOW.

The second IF pulse in the burst will clock the status of the H_EVENT_GEN signal, which is now a HIGH, into Event Gen F/F U34, causing U34(2), P_EVENTS, to go HIGH and U34(3), EVENTBAR, to go LOW. U33 inverts the EVENTBAR signal into the EVENTS signals at U33(2); thus, the EVENTS line will go HIGH. The high P_EVENTS signal at U34(2) causes the L_OK line to be HIGH via U22(10) and U21(14). The high L_OK line at U21(14) resets Event Gen F/F U34, producing a pulse on the EVENTS line. The high P_EVENTS signal also toggles Event Gate F/F U20, causing the outputs lines of the flip-flop to be in their TRUE state (that is, L_PLD_EN and H_E_GT2 are HIGH; L_E_GT1 and L_E_GT2 are LOW). The amount of time the H_E_GT2 or the L_PLD_EN signals stay HIGH is called the gate time. The low L_E_GT2 signal forces the output at U22(3), H_EVENT_GEN, to be LOW. This causes Event Gen F/F U34 to not produce any more pulses as subsequent IF pulses clock only "0" into U34.

The high L_PLD_EN signal from U20(2) tells the A3 Counter Assembly to start down counting the preprogrammed value. The L_PLD_EN signal is connected to pin 5 of U7 (Remainder Counter in the Event Counter/Width Generator block). When the A3 Assembly is done counting, the L_PLD_EN signal sets the L_EOW (End-of-Width) signal from U7(4) to LOW. The output of U21(6) then goes HIGH as all its inputs are LOW. This causes the H_EVENT_GEN line to be HIGH, and the next IF pulse will produce a pulse on the P_EVENTS. Hence, a pulse is also produced on the EVENTS line U33(2), and it is sent to the A3 Counter Assembly. The pulse on the P_EVENTS line will toggle Event Gate F/F U20 to put its outputs in their inactive state (that is, L_PLD_EN and H_E_GT2 are LOW; L_E_GT1 and L_E_GT2 are HIGH). This closes the gate. Thus, Event Gen F/F U34 has produced two pulses – one at the beginning of the gate, and the other at end of the gate. The MRC on the A3 Assembly will then measure the time between these pulses.

The L_EOW signal from Remainder Counter U7(4) goes HIGH after one more IF cycle, causing the L_CLOSE_GATE signal from U23(15) to be LOW. This causes the H_ARM signal

out of U9(2) to go LOW. Thus, the L_QUAL_ARM signal at U10(14) goes HIGH. This HIGH signal to the exclusive-OR gate U22(2,3,4,5) will cause the H_EVENT_GEN signal at U22(30) to be HIGH, producing one more pulse on the EVENTS line, U33(2). The H_ARM signal being LOW for the remainder of the time will not allow any measurement to be taken during the remainder of the pulse. After the pulse goes away, the envelope going away produces a reset pulse that will reset the Synch1 (U10) and Event Gate (U20) flip-flops, bringing all the lines to their initial conditions, which are listed in the sixth paragraph of this section (that is, Internal Gate mode section).

EXTERNAL GATE MODE. The External Gate mode's gate generation logic is similar to the Internal Gate mode. There are two major differences:

- the gate opens with external gate synchronized to the IF, and
- the A3 Counter Assembly accumulates the number of IF pulses or events during the time the gate is open.

To set the A14 Gate Board Assembly into the External Gate mode, A4 microprocessor selects the external gate as the output of Command Latch U12 of the Microprocessor Interface block; that is, L_EXT_μP and L_EXT_OR_INT lines are LOW. The L_EXT_μP and L_EXT_OR_INT lines are input to U8(9) and U8(7), respectively. These LOW level lines cause the H_ARM signal at U9(2) to follow the ECL_H_EXT_IN signal out of U5(14) of the Gating and Arming block, which is the ECL version of the TTL input H_EXT_OR_ARM out of U16B(4). The H_EXT_OR_ARM signal is the inverted version of the EXT_IN gate signal at J1 (GATE/ARM IN). The L_EXT_μP and L_EXT_OR_INT lines also are routed to NOR gate U31 of the Arming and Gating block. This causes the H_EXT_EN line at U31(3) to go HIGH, indicating that the instrument is External Gate mode. The HIGH at U31(3) is routed to U18(10) of the Event Counter/Width Generator block, causing the L_W_MODE signal at U18(7) to go HIGH. This forces the output of U21(6) of the Gate/Event Generation block, to be LOW and the W_MDE_RST signal out of U33(3), which is a reset for Event/Gate F/F U20, to be LOW or inactive. The L_W_MODE signal, however, activates the set input to the Event Gate F/F, causing the L_PLD_EN line at U20(2) to be always HIGH and the L_E_GT1 line at U20(3) to always LOW. The high L_PLD_EN line does not allow the A3 Counter Assembly to preload any count at all; therefore, The L_PLD_EN and L_E_GT1 lines of U20 cannot be programmed to any value. These lines are reset before the measurement cycle begins to count the events.

Only the lower half (U20 pins 10,12,13,14,15) of Event Gate F/F now controls the counting of events by the A3 Counter Assembly. Since the H_EVENT_GEN signal is a wired-OR of U21(3), U22(3), and U21(6) and U22(3) is active during the external gate measurements, the H_EVENT_GEN signal follows the L_Q_ARM and L_E_GT2 signals at U22(4) and U22(5), respectively. The first IF pulse after the H_ARM signal at U9(2) goes HIGH will clock the status of Synch1 F/F U10. If the L_ECL_MEAS_OK signal at U10(7) is LOW, it causes the L_OK signal at U10(2) to be LOW. U10(14), L_Q_ARM, going LOW causes the H_EVENT_GEN signal at U22(3) to go HIGH because U22 is an exclusive-OR gate. (L_E_GT2 at U22(5) was HIGH since the gate is not open yet.) The HIGH at U22(3) causes

Event Gate F/F U20 to produce a pulse on the next event of the IF as described previously in the Internal Gate Mode section. The H_E_GT2 signal at U20(15) goes HIGH, allowing the A3 Counter Assembly to count, and the L_E_GT2 signal at U20(14) goes LOW, causing the H_EVENT_GEN line at U21(6) to go LOW. This LOW causes no more pulses to be produced, and Event Gate F/F U20 is now clocked "0" by every IF event that follows.

When the external gate signal goes away, the H_ARM signal at U9(2) goes LOW. The next IF event after that will cause the L_Q_ARM signal out of U10(14) to go HIGH. This in turn will cause the H_EVENT_GEN signal to go HIGH because now the L_E_GT2 at U20(14) is LOW as the gate is opened. This causes Event Gen F/F U34 to produce another pulse on the next IF event. This then goes to the MRC on the A3 Assembly to close the MRC time measurement as explained before. This pulse toggles U20 and the gate closes, causing the H_E_GT2 signal at U20(15) to be LOW and L_E_GT2 signal at U20(14) to be HIGH. The high L_E_GT2 causes the H_EVENT_GEN line to go LOW by virtue of the exclusive-OR nature of gate U22. Now onwards the Event Gen F/F U34 gets clocked "0" and no more pulses are produced.

When the pulse or external gate signal goes away, the envelope going away is detected and a reset is produced that will reset flip-flops of Event Gen F/F U34 to their respective initial state.

The Ext Stretch F/F U35, capacitor C41, and resistor R59 of the Gating and Arming block, and NAND gate U9(pins 9,12,13) of the Gate/Event Generation block are used to stretch the external gate input signal for a minimum of 25 ns. This is performed to prevent the external gate signals from being too narrow, which would cause the two pulses on the EVENTS line at U33(2) to be too narrow to be effectively measured by the MRC on the A3 Assembly. When the H_SYNC_ARM signal out of U10(15) goes HIGH on response to clocking of the H_ARM signal into Synch1 F/F U10 at input U10(10), it clocks a LOW or "0" into Ext Stretch F/F U35. The ARM_FF_SET signal out of U9(9) goes HIGH, setting Synch1 F/F U10. This keeps the L_Q_ARM signal at U10(14) in its LOW or active state irrespective of what happens to the H_ARM input signal. The time for which the ARM_FF_SET signal remains HIGH is determined by R59 and C41. When H_SYNC_ARM clocks a LOW in Ext Stretch F/F U35, U35(14) goes HIGH, causing the voltage across C41 to slowly rise. When the voltage across C41 reaches the threshold for the set input, U35(12), it sets U35. This causes the ARM_FF_SET at U9(9) to be LOW, removing the set from Synch1 F/F U10. The L_Q_ARM signal will then follow the H_ARM, synchronized to the IF event.

ARMED MODE. In the Armed mode, the A14 Gate Board Assembly makes the measurement on the next IF pulse burst if it receives the trigger on the EXT_IN line via the front panel's GATE/ARM IN input connector (J1). The A14 Gate Board Assembly performs the measurement with the internal gate; therefore, the gate generation logic works exactly identical to the way explained in the previous Internal Gate Mode section.

The difference comes from the way the L_ECL_MEAS_OK input signal to Meas Qual F/F U10 becomes active. In Armed mode, the microprocessor sets up the H_ARM_MODE line in the command word to 1 (or HIGH); thus, removing the set from the Ext Arm Fault F/F

U26A of the Gating and Arming block. This causes the H_ARMED signal out U26A(5) to be active only if U26A gets an edge on its clock signal. Once U26A(5) is armed, the H_TTL_MEAS_OK signal out of U28A(12) goes HIGH, causing the a low L_ECL_MEAS_OK signal out of U5(12); thus, the measurement progresses as described in the previous Internal Gate Mode section. There must be at least 50 ns between the triggering edge and the beginning of the pulse burst for the triggering edge to be recognized; otherwise, Ext Arm Fault F/F U26A will be cleared by the falling edge of the envelope. Thus, the trigger will not be recognized. Once the measurement on one pulse burst is complete, flip-flop U26A will wait for the next trigger for its output, H_ARMED, to go HIGH again, stopping any further measurements.

EVENT COUNTER/WIDTH GENERATOR. This block performs two functions. During the External Gate mode, the counter circuit of this block counts the number of events while the gate is open. During Internal Gate mode, it generates a signal to close the gate after counting a preprogrammed number of events; after closing the gate, the counters of this block are preloaded for the next pulse.

The Event Counter/Width Generator block is comprised of Timer (or Width Counter) U3, Quad NAND gate U4, Remainder Counter U7, Event (or Divide-by-16) Counter U19, and parts of U6, U14, U15, U18, and U30.

Internal Gate Mode. As mentioned previously, the purpose of this block in the Internal Gate mode is to keep the gate open for the preprogrammed number of IF events. The IF events are down counted by the counters U19, U3, and U7.

Initially when the gate is not open, the Event Gate F/F (U20) of the Gate/Event Generation block outputs are in their inactive state; that is, U20(2) and U20(15) are LOW; and U20(3) and U20(14) are HIGH. The L_COUNT_EN line is wired-OR to U6(15) and U6(3). As the measurement is made with the internal gate, the L_EXT_μP line from Command Latch U12 via resistor R39C is HIGH, causing U6(3) to be always LOW. The L_COUNT_EN signal, therefore, follows U6(15). In the Internal Gate mode, the L_W_MDE signal at U6(13) is always LOW. Therefore, the L_COUNT_EN signal at U6(15) is nothing but an inverted L_R_CNTR_EN signal. U20(2), L_PLD_EN, of the Gate/Event Generation block is LOW, keeping Event Counter U19 and Remainder Counter U7 in parallel load; that is, with the first clock pulse, the values programmed in Event Input Latch U2 of the Microprocessor Interface block will be loaded into the counters (U19, U7) but will not count. As long as Event Counter U19 is in parallel load mode, its terminal count output is HIGH, causing the L_R_CNTR_EN signal to be HIGH and L_COUNT_EN to be LOW. A LOW L_COUNT_EN signal allows Event Counter U19 to count, provided it is not in parallel load. If L_COUNT_EN is HIGH, the counting is disabled.

The first IF pulse in the burst, loads the Event (U19) and Remainder (U7) counters with the preprogrammed values. When the second IF pulse in the burst opens the gate as described in the Gate/Event Generation block paragraphs, U20(2) and U20(15) of the Gate/Event Generation block go HIGH. This removes the Event (U19) and Remainder (U7) counters

from the parallel load mode into the ready-to-count mode. However, if the L_R_CNTR_EN signal from U18(15) is LOW, Remainder Counter (U7) will not count.

Event Counter U19 then counts the IF pulses in the burst. U19(14), BIT3 (divide-by-16 output), will then clock the Timer U3. The L_R_CNTR_EN signal is an effective wire-OR of two signals: terminal count of U19(4) and L_E_8254_DN. Thus, Remainder Counter U7 will not count until U19 and U3, have reached their terminal count. This coincidence is needed to synchronize the output delay of U3 with respect to the clock input.

When the L_R_CNTR_EN goes LOW, the L_COUNT_EN goes HIGH and disables further counting by the U19 and U3. It also enables Remainder Counter U7 to count events. When the events reach terminal count (15), the L_EOW line at U7(4) goes LOW for one IF clock cycle. When the L_EOW line goes HIGH, it clocks 0 into flip-flop U23 of the Gate/Event Generation block, causing the L_CLOSE_GATE signal at U23(15) to be LOW. The low L_EOW line also causes the H_EVENT_GEN signal at U21(6) to go HIGH, and the next IF event generates a pulse at the output of Event Gen F/F U34. This pulse at U34(2), P_EVENTS, closes the gate.

External Gate Mode. In External Gate mode, Event Gate F/F U20 of the Gate/Event Generation block is always in the set condition: U20(2) is HIGH, and U20(3) is LOW. As U20(2) is always HIGH, it does not allow the U19 and U7 to be preloaded. Therefore, these counters need to be reset to zero by A4 microprocessor. The microprocessor does this by pulsing the L_INTP_RST line LOW.

When the gate opens, U20(15) (H_E_GT2), goes HIGH. This causes the L_COUNT_EN signal to go LOW, through U6(3). Event Counter U19 starts counting the IF events. BIT3, U19(14), performs as a clock for the 16-bit counter-0 in Timer U3. The output of the counter-0, L_8254_SEL (pin 10 of U3), performs as a clock for 16-bit counter-1 in U3. Thus, U19 and the two counters in U3 form a 36-bit event counter, counting the IF events.

When the gate closes, U20(15) or H_E_GT2 goes LOW, causing the L_COUNT_EN signal to go HIGH. This disables counting in Event Counter U19; therefore, the counter-0 and counter-1 in U3 do not get any more clocks. Thus, these counters will not count any further.

GATING AND ARMING. The purpose of this block is to decide when to take a measurement, and to decide if the measurement taken is a valid one. The Gating and Arming block performs three functions to accomplish this. First, it prevents the Gate/Event Generation block from making a measurement until other conditions on the gating and counting sections are correctly synchronized. Second, it monitors the status of all gating section fault lines. And third, it controls the ENVELOPE signal routed to the counter section. The ENVELOPE signal is enabled only for OFFTIME, PRI, PRF, and PW measurements. For pulsed frequency measurements, the ENVELOPE signal is disabled.

The Gating and Arming block consists of two main circuits: the Measurement Qualifier circuit, and the Measurement Validation circuit.

Measurement Qualifier Circuit. This circuit consists of Ext Arm Fault F/F U26A, Envelope Qual F/F U26B, and parts of U28 and U5. U5(12) converts the high level H_TTL_MEAS_OK signal at U28A(12) to a LOW ECL signal, L_ECL_MEAS_OK. When this signal is LOW, it allows the Gate/Event Generation block to take a measurement. The high H_TTL_MEAS_OK signal from U28A(12) is also used to allow, via Envelope Qual F/F U26B, the envelope signal to pass through U28B(6) as ENVELOPE_CTR (ENV_CTR on schematic) to the A3 Counter Assembly for envelope measurements, if envelope is not disabled.

H_TTL_MEAS_OK will be HIGH only if H_GATE, L_HOLDOFF, and H_ARMED are all HIGH since these are three inputs going into NAND gate U28A, which generates the H_TTL_MEAS_OK signal.

A4 microprocessor controls when to take a measurement by controlling the H_GATE line. It brings this line HIGH for one measurement, and then brings it LOW after the measurement has taken place. If measurements are being taken on more than one pulse bursts, the microprocessor has to toggle this line that many times.

L_HOLDOFF comes from the A3 Counter Assembly, and it is active LOW. It will be LOW for the duration for which A3 Assembly circuitry will not be ready for a measurement. It also stops the A14 Gate Board from making a measurement in cases where the PRF is high enough that the microprocessor has not had a enough time to bring the H_GATE line LOW.

For frequency measurements, A4 microprocessor sets the H_ARM_MODE line, which connects to U26A(4), to LOW causing the H_ARMED signal at U26A(5) to always be in the HIGH state. In arming mode, the H_ARM_MODE line is set HIGH by A4 microprocessor; therefore, the H_ARMED signal will follow the status of the L_HOLDOFF signal when clocked by the H_EXT_OR_ARM signal from U16B(4), which is the external arm signal connected to the instrument's GATE/ARM IN input.

For envelope measurements, A4 microprocessor sets the L_TTL_E_DIS line HIGH through Command Latch U12(5) of the Microprocessor Interface block. The status of the H_TTL_MEAS_OK signal is sampled on the rising edge of the envelope signal, H_ENV_GTBD (from U15(13) of the Event Counter/Width Generator block). If it is okay to make a measurement, the ENV_QUAL signal from U26B(9) goes HIGH, allowing the envelope to pass through AND gate U28B on the EVN_CTR line, U28B(6). Because of the delay through U26B and the different propagation times for the high-to-low and low-to-high transitions through AND gate U28B, the ENV_CTR signal going to the A3 Assembly is effectively shortened by 5 to 10 ns.

Measurement Validation Circuit. This circuit consists of the Gate Fault part of F/F U23 of the Gate/Event Generation block, the Gate Fault part of F/F U35 of the Gating and Arming block, the ECL-to-TTL converter U15(pins 5,6,7), the Arm Fault F/F U25A, and the Inband Fault F/F U24B.

This circuit determines if the measurement just taken is a valid measurement or not. It does this by reading the status of various fault signals on the A14 Gate Board Assembly. These fault signals are as follows:

- GATE_FAULT
- ARM_FAULT
- INBAND_FAULT (External gate inband fault)

GATE_FAULT. This fault gets set if the gate closes on the last IF pulse or if the gate does not close at all. While a frequency measurement is taking place the Measurement Validation circuit checks that the gate has not closed on the last IF pulse, or has not closed at all. The circuit does this because the last edge (event) of the IF tends to have more timing associated with it. If the gate does not close at all, then the MRC on the A3 Assembly does not receive any time information until the gate opens again. In this case, the time measured will be the period between openings of two gates and the duration of the gate; thus, an incorrect time and hence frequency measurement will be made.

When the gate opens, the H_E_GT2 signal from U20(15) of the Gate/Event Generation block will go HIGH, forcing a "set" on Gate Fault F/F U23. This causes the H_POSS_FAULT signal from U23(2) to be HIGH. If the gate closes, the H_E_GT2 signal will go LOW, removing the set on U23. If the gate has closed on or after the last event or IF pulse, the H_POSS_FAULT signal will remain HIGH. If the gate closed in time, then the next IF pulse or event will clock a "0" or LOW into U23, causing H_POSS_FAULT to be LOW. The H_POSS_FAULT line is connected to the D input (pin 7) on the Gate Fault F/F U35 of the Gating and Arming block, and it is actually a wired-OR combination of the Q outputs of U35(2) and U23(2). The H_POSS_FAULT line is sampled by the envelope signal (L_ENV_IN) going away. If the L_ENV_IN signal at U35(6) is HIGH, U35(2) will go HIGH and keep H_POSS_FAULT line HIGH. This is required because the gate may subsequently close correctly. Once the Gate Fault F/F U35 is set, it can only be cleared by making the H_CNTR_RST line (from the Reset Generation Logic circuit (U30) of the Event Counter/Width Generator) LOW. This is done by the A4 microprocessor by making the L_INTP_RST line at U30(5) LOW. The TTL-to-ECL converter (U5 pins, 5,6,7) of the Gating and Arming block will cause the H_CNTR_RST line to go HIGH. The output at U35(2), H_POSS_FAULT, is then level translated and sent out to Event/Status Latch U1 of the Microprocessor Interface block as the GATE_FAULT signal. After performing a measurement, the A4 Microprocessor Assembly looks at the GATE_FAULT signal at U1(13). If GATE_FAULT is set, the firmware discards the entire measurement and restarts the measurement. If the measurement is performed on more than one pulse bursts (which it normally will be), then the entire set needs to be discarded as there is not way of knowing which pulse burst had a fault.

ARM_FAULT. This fault gets set if the very next pulse after being armed goes out of band during the entire measurement. Arm Inband F/F U11A, Arm Fault F/F U25A, inverter U16D, and flip-flop U11A form the ARM_FAULT circuit. *Figure 5-10* shows the timing diagram of this circuit.

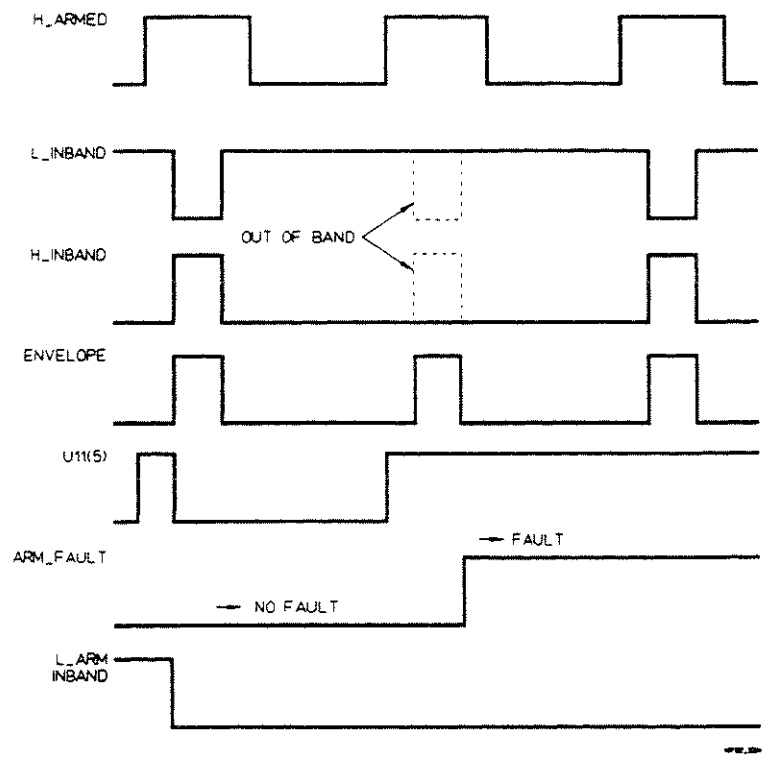


Figure 5-10. Armed Inband Detection Timing Diagram

Arm Inband F/F U11B checks if the signal was ever inband in the Armed mode. It does this by sampling the status of the H_ARMED signal at U11B(12) on on the rising edge of the H_IF_INBND signal at U11B(11). If the counter is triggered, H_ARMED is HIGH; therefore, the outputs at U11B(9), H_ARM_INBND, and U11B(8), L_ARM_INBND, become true (that is, U11B(9) is HIGH and U11B(8) is LOW). The low L_ARM_INBND signal at U11B(8) sets U11B, holding the H_ARM_INBND signal at U11B(9) in its HIGH state. When the L_ARM_INBND signal goes LOW, it also causes U28C(8), L_SIG_INBND, to be LOW, informing the A4 microprocessor that the signal was inband at least once during the measurement.

The H_ARM_INBND signal at U11B(9) going HIGH removes the reset from Arm Fault F/F U25A. The H_ARMED signal going HIGH clocks a "1" into F/F U11A. If the next pulse burst is inband, the L_IF_INBND signal at U11A(1) will go LOW. This will reset U11A; thus, U11(5) goes LOW. This removes the "1" from the J input (pin 3) of U25A. The falling edge of the envelope, therefore, does not change the output status of the ARM_FAULT signal at U25A(5) which remains LOW, indicating no fault occurred. If the next pulse burst is not inband, U25A(3) does not get reset to "0"; therefore, the falling edge clocks a "1" into U25A(3), causing the ARM_FAULT signal at U25A(5) to go HIGH. Once the output is set, it can not be reset because the K input (pin 2) of U25 is always tied LOW. The only way this circuit can be reset is by the microprocessor; the circuit is reset when the microprocessor pulls the L_μP_RST signal LOW via Decoder U27 of the Microprocessor Interface block. This

LOW signal is connected to pin 13 of the Arm Inband F/F U11B. When the reset (L_μP_RST) is applied, it clears out U11B, causing the U11B(9), H_ARM_INBND to go LOW. This resets U25A.

INBAND_FAULT. This fault is set if the signal goes out of band any time during the measurement with the external gate. Once the fault is set, it can be reset by the A4 microprocessor by making the L_μP_RST line LOW. Gate Inband Fault F/F-1 U14B, Gate Inband F/F-2 U24A, Inband Fault F/F U24B, NOR gate U16C, and AND gates U28B and U28C form the Inband Fault circuit. *Figure 5-11* shows how the circuit operates.

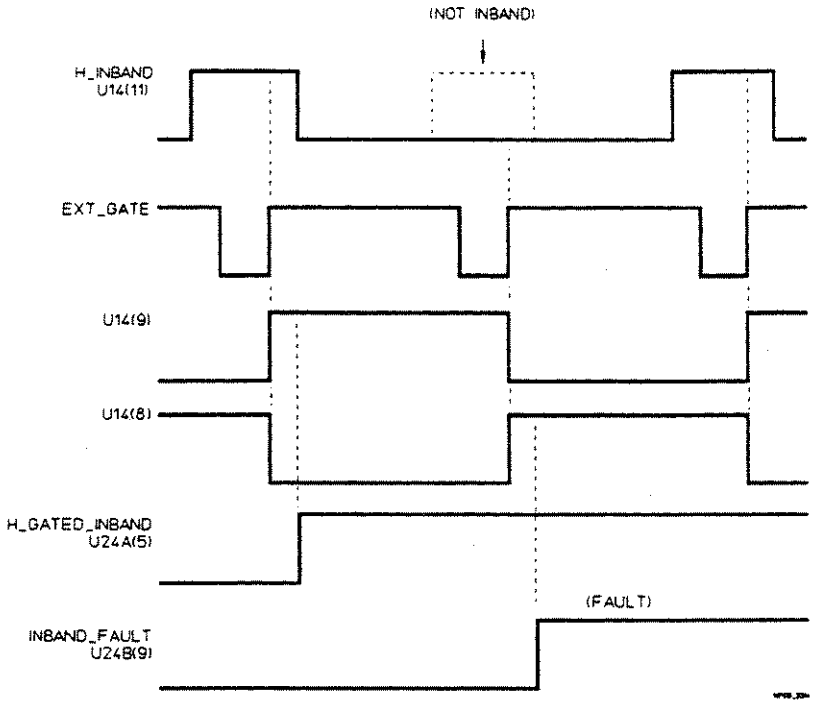


Figure 5-11. External Gate and Inband Detection Timing Diagram

Initially, the circuit is reset by the microprocessor by making the L_μP_RST line (pin 7 of Decoder U27 of the Microprocessor Interface block) LOW and then HIGH. This resets Gate Inband F/F-1 U14B and Gate Inband F/F-2 U24A. As U24A is reset, the H_GATE_INBAND signal out at U24A(5) goes LOW, causing the Inband Fault F/F U24B to also be reset; thus, the INBND_FLT signal at U24B(9) becomes LOW. The state of the inband signal (H_INBND) from U16C(10) is sampled by Gate Inband F/F-1 U14B at the falling edge of the external gate signal (or H_EXT_OR_ARM) at U10C(8).

If the H_INBND signal at U16C(10) is inband (that is, if it is HIGH), then Gate Inband F/F-1 U14B gets set. This clocks a "1" into Gate Inband F/F-2 U24A, causing the H_GTD_INBND

signal out of U24A(5) to go HIGH. This HIGH removes the reset from Inband Fault F/F U24B, resulting in a high INBND_FLT signal. Once this signal is set HIGH, only the microprocessor can reset it. Since U24A(5) is HIGH at this time, the L_GTD_INBND signal out of U24A(6) is LOW. This LOW signal forces the (L_SIG_INBND) output signal of U28C(8) to a LOW, indicating that the signal was inband at least once. If the signal was never inband, a "1" will never get clocked in the U24A, and U24B will never come out of its reset state.

Now, if the signal is ever goes out of band, the falling edge of the external gate signal (or H_EXT_OR_ARM) will then clock a "0" into Gate Inband F/F-1 U14B. This will cause the output at U14B(8) to go HIGH, clocking a "1" into Inband Fault F/F U24B. This will set the INBND_FLT signal at U24B(9) HIGH, indicating a fault to the A4 microprocessor through Event/Status latch U1 of the Microprocessor Interface block. After reading the latch, the microprocessor resets the circuit.

Note that the status of the INBAND signal is checked only when the external gate goes away. This allows the external gate to come in earlier than the pulse. In this case, the actual measurement gate is not yet open on the second IF pulse in the burst.

5-146. Schematic Diagrams

The following pages contain front and rear panel views, a top internal view, an overall block diagram, followed by a schematic diagram for each of the circuit-board assemblies in the HP 5361B. Each schematic diagram includes a component locator for each field repairable assembly. Where applicable, test and troubleshooting waveforms are placed adjacent to the schematic. The schematic diagrams are arranged in order by assembly number (except for the A8 Motherboard Assembly's component locator and schematic diagram).

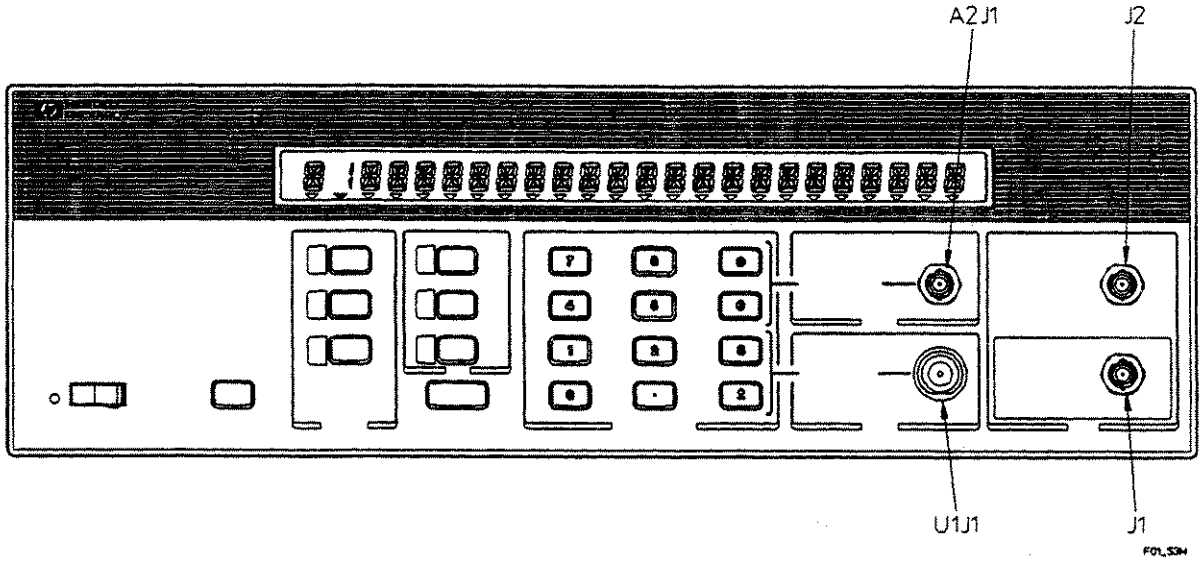


Figure 5-12. Front Panel View

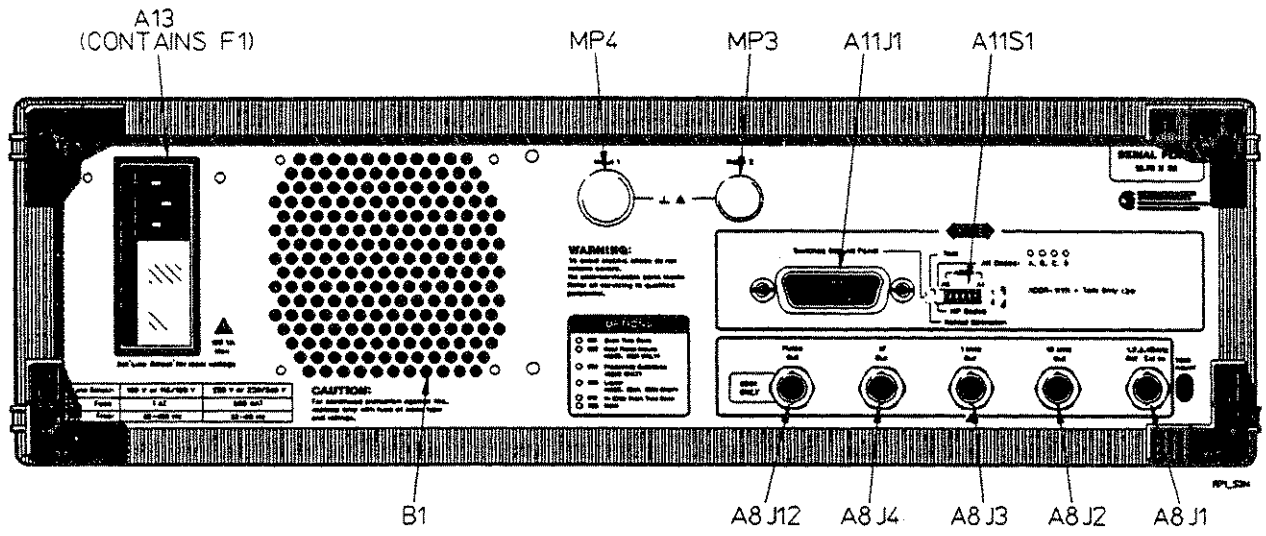


Figure 5-13. Rear Panel View

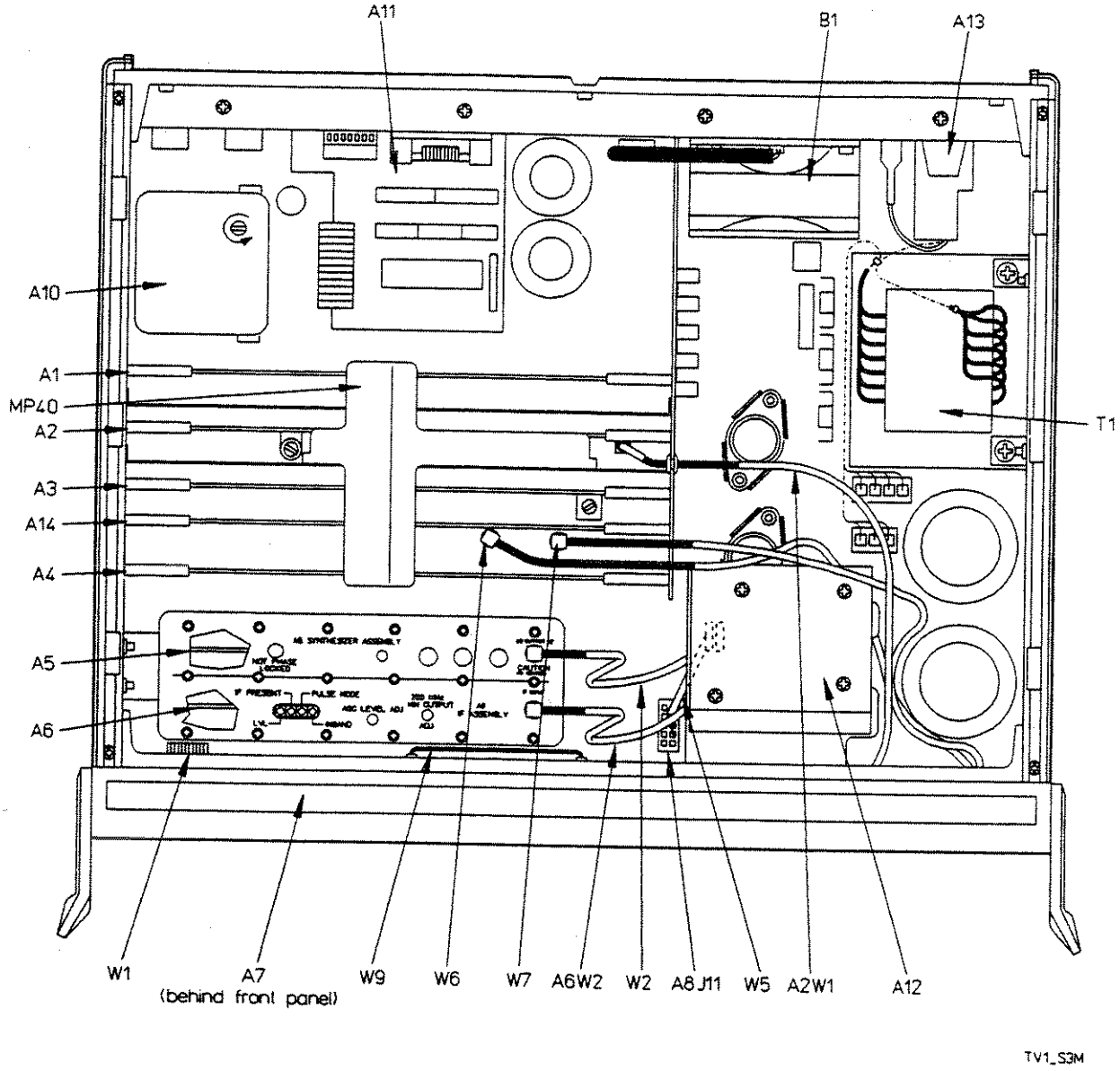


Figure 5-14. Top Internal View

A12 MICROWAVE MODULE

LO 295-350MHz +14dBm

MATCHING NETWORK C21,C22, C28,C29,L17

GAIN AMP +11dB

Q2 (R8,R9 L16,L18)

MATCHING NETWORK C19,C24, L14,L15

+25dBm

RF IN FROM INPUT 1

U1 SAMPLER

BIAS/ MATCHING NETWORK C9,C12, L1,R1,R7

Q1 (C1, R2,R10) BUFFER AMP 0dB

U1 (R3) GAIN AMP +16dB

LOW PASS FILTER C4,C16,L2,L3,L4

U2 (L7) GAIN AMP +16dB

C11

LOW PASS FILTER C5,L5,L6

FROM A8: +13V SW, +5V SW, -5V

A6 IF AMPLIFIER/DETECTOR ASSEMBLY

FROM A4: L_IF_TEST

FROM A5: AUX_A

FROM A4: L_IF_OFF

TEST/ DIAGNOSTICS U11E, U12, Q1, CR2

IF 0.5-175MHz 0 TO -33dBm

AGC LOOP

VARIABLE ATTENUATOR U16

AMP 1 U15 (+19dB)

LOW PASS FILTER 1 L11-17, C56, C62, C68 (7-POLE 175 MHz)

AMP 2 U10 (+19dB)

(4-POLE 200 MHz)

LOW PASS FILTER 2 L4, L5, C31, C32

AMP 3 U5C, E (+5dB)

BUFFER AMPS U5D, U5B

U6A INBAND DRIVER

INBAND 35-105MHz DECTECTOR U4

U9A ECL TO TTL CONVERTER LOGIC

SCHMITT TRIGGER U1, U2

+IF_NEW

+IF_NEW

GATE/ARM IN (FRONT PANEL)

(REAR PANEL IF OUT

MONITOR DRIVER

U5A

NEW_IF_MON

ENVELOPE

FROM A4: L_LOW_PRF

INTEGRATOR U13C, Q3

SAMPLE AND HOLD

U8

AGC DETECTOR U6D, U6E

AGC LOOP REF U13B, U14, CR6, R42

ENVELOPE DETECTOR U6B, U6C

ENVELOPE COMPARATOR

U7

ENVELOPE

U9B ECL TO TTL CONVERTER LOGIC

L_IF_INBAND

IF PRESENT AND OVERLOAD DECTECTOR U9D, U9C, U18C

L_IF_PRSNT

L_OVLD

FROM A8: +15V, +5.0V, -5.2V, GND

SAMPLE AND HOLD BUFFER U13A, U13D

L_LOW_PRF

SAMPLE AND HOLD CONTROL U17A, U17B, U18A, Q4

STATUS LATCH U19, U11A-U11D

L_PULSE_PRSNT_LCH

L_NO_IF_LCH

L_INBAND_LCH

L_MODE_LCH

TO A4

FROM A4: L_IF_BD_RST

A14 GATE BOARD ASS

GATE/EVENT GENER

L_CLOSE_GATE

H_GATE

EXT_ARM_GATE

ECL_HIGH

MUX_CONTROL

RESE

FROM A3

TO/FROM A4

GATING AND AR

L_IF_INB

ARM

ARMED

FROM A4: H_GATE

FROM A3: L_HOLDOFF

ENVELOPE_DETE

H_GATE

LF_OUT_A, LF_OUT_B (10Hz - 80MHz)

A2 LOW FREQUENCY INPUT ASSEMBLY

FROM A5: AUX_B, AUX_A

GATE U8

AUX_B

AUX_A

U6

U3 MUX

FROM A4: L_LF_TEST

IMPEDANCE CONVERTER Q6,Q9

SWITCH Q7,Q8, Q10,Q11

INPUT 2

10Hz - 80MHz

10MHz - 525MHz

SWITCH/ LIMITER CR7,CR8, CR9,CR10

U5,U7 +20dB

U4 +10dB

÷10 U1

Q3

DET C4,CR4,U2

FROM A4: H_LF_50

LF_OUT_SEL

SWITCH Q4,Q5

FROM A8: +15V, +5V

A5 SYNTHESIZER ASSEMBLY

SYN TEST1-4 FROM A4

100KHz OR 10MHz/R (LO OFF)

4 TO 1 MULTIPLEXER U8

AUX_A

AUX_B

TO A2, A3, A6

MODULUS CONTROL (100KHz VARIABLE DUTY CYCLE)

5.9-7.0MHz

+N DIVIDER (59 ≥N ≥70) P/O U3

÷ P, ÷(P+1) DIVIDER (P=50) U10,U7

29-35MHz

295-350MHz

SYN LATCH FROM A4

SYN DATA 0-7 FROM A4

LATCHES AND PROGRAMMING CIRCUITS U4,P/O U3

100KHz

A COUNTER AND MODULUS CONTROL P/O U3

CMOS TO ECL CONVERTER C10,C14,CR2,CR3 CR4,R9-R11

LO OFF Q5

ISOLATION AMPLIFIER Q7

10MHz FROM A1(TBB)

÷R DIVIDER (R=100) P/O U3

100KHz

PHASE DETECTOR (100KHz) P/O U3

INTEGRATOR U1

LOW-PASS/ NOTCH FILTER C19,C28,C29,C35, C39,L2,L3,R14

VOLTAGE CONTROLLED OSCILLATOR CR13, Q6

LIMITER/ ISOLATION AMPLIFIER U6

295-350MHz

U9 POWER AMPLIFIER +14dB

LO

FROM A8: +5V, -5V, -24V

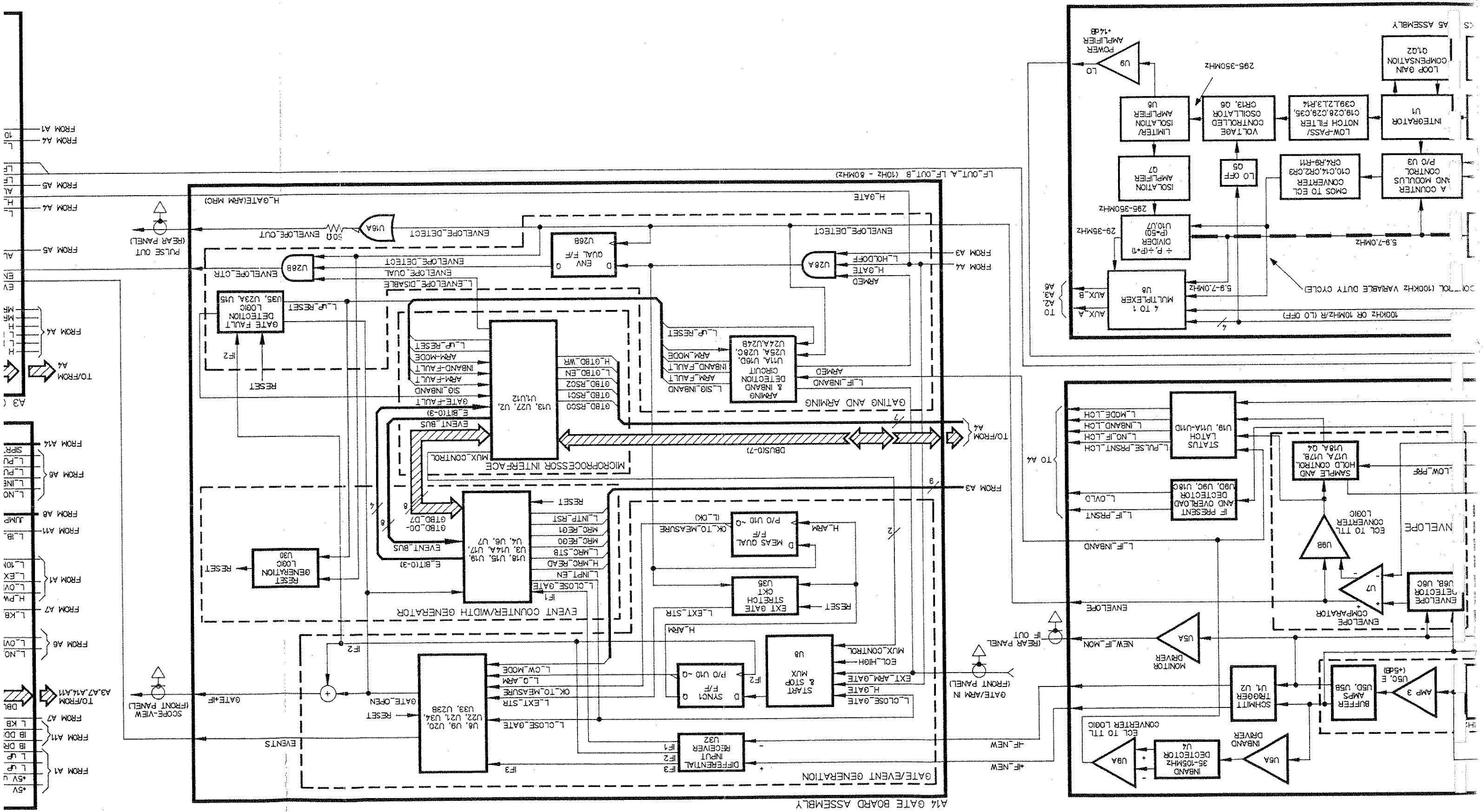
POWER SUPPLY FILTERS AND -20V REGULATOR C25-C27,C34 C41-C43 L4-L7,Q4,U5

LOCK DETECT INDICATOR DS1, Q3,U2

LOOP GAIN COMPENSATION Q1,Q2

TO ALL BLOCKS IN A5 ASSEMBLY

LF_OUT_A, LF_OUT_B (10Hz - 80MHz)


A14 GATE BOARD ASSEMBLY
GATING AND ARMING
EVENT COUNTER/WIDTH GENERATOR
MICROPROCESSOR INTERFACE
GATE/EVENT GENERATION
ENVELOPE
LF_OUT_A, LF_OUT_B (10Hz - 80MHz)
H_GATE(ARM MRC)
ENVELOPE_DETECT
ENVELOPE_OUT
50Ω
PULSE OUT (REAR PANEL)
ARMED
H_GATE
L_HOLDOFF
L_ENVELOPE_DISABLE
L_UP_RESET
GATE FAULT DETECTION LOGIC U35, U23A, U15
RESET
IF2
ARM_MODE
INBAND_FAULT
ARM_FAULT
SIG_INBAND
GATE_FAULT
E_BIT(0-3)
EVENT_BUS
GTBD_RS00
GTBD_RS01
GTBD_RS02
L_GTBD_EN
H_GTBD_WR
DBUS(0-7)
MUX_CONTROL
GTBD_D0-GTBD_D7
L_INTF_RST
MRC_REG1
MRC_REG0
L_MRC_STB
H_MRC_READ
L_INPT_EN
L_CLOSE_GATE
IF1
RESET GENERATION LOGIC U30
H_ARM
OK_TO_MEASURE
L_EXT_STR
EXT GATE STRETCH CKT U35
EOL_HIGH
EXT_ARM_GATE
L_CW_MODE
L_Q_ARM
IF3
DIFFERENTIAL INPUT RECEIVER U32
SCOPE-VIEW (FRONT PANEL)
GATE+IF
GATE_OPEN
EVENTS
IF_NEW
GATE/ARM IN (FRONT PANEL)
IF OUT (REAR PANEL)
NEW_IF_MON
MONITOR DRIVER
ENVELOPE COMPARATOR
ENVELOPE DETECTOR U8B, U8C
ECL TO TTL CONVERTER LOGIC
SAMPLE AND HOLD CONTROL U17A, U17B, U18A, Q4
LOW_PRF
STATUS LATCH U19, U14A-U14D
IF PRESENT AND OVERLOAD DETECTOR U9D, U9C, U18C
L_PULSE_PRSNT_LCH
L_NO_IF_LCH
L_INBAND_LCH
L_MODE_LCH
L_IF_PRSNT
L_OVLD
TO A4
SCHMITT TRIGGER U1, U2
BUFFER AMPS U5D, U5B
AMP 3 (+5dB)
U5C, E
INBAND DRIVER
INBAND 35-105MHz DECTECTOR U4
ECL TO TTL CONVERTER LOGIC
AUX_A
AUX_B
4 TO 1 MULTIPLEXER U8
100KHz OR 10MHz/R (LO OFF)
5.9-7.0MHz
÷ P, ÷(P+1) DIVIDER (P=50) U10,U7
29-35MHz
295-350MHz
A COUNTER AND MODULUS CONTROL P/O U3
CMOS TO ECL CONVERTER Q4,R9-R11
LO OFF Q5
ISOLATION AMPLIFIER Q7
LIMITER/ ISOLATION AMPLIFIER U8
VOLTAGE CONTROLLED OSCILLATOR CR13, Q6
LOW-PASS/ NOTCH FILTER C19,C28,C29, C39,L2,L3,R14
INTEGRATOR U1
LOOP GAIN COMPENSATION Q1,Q2
LO
POWER AMPLIFIER +14dB
U9
TO A2, A3, A6
FROM A3
FROM A4
FROM A5
FROM A1
TO/FROM A4
TO/FROM A3,A7,A14,A11

A4 MIC

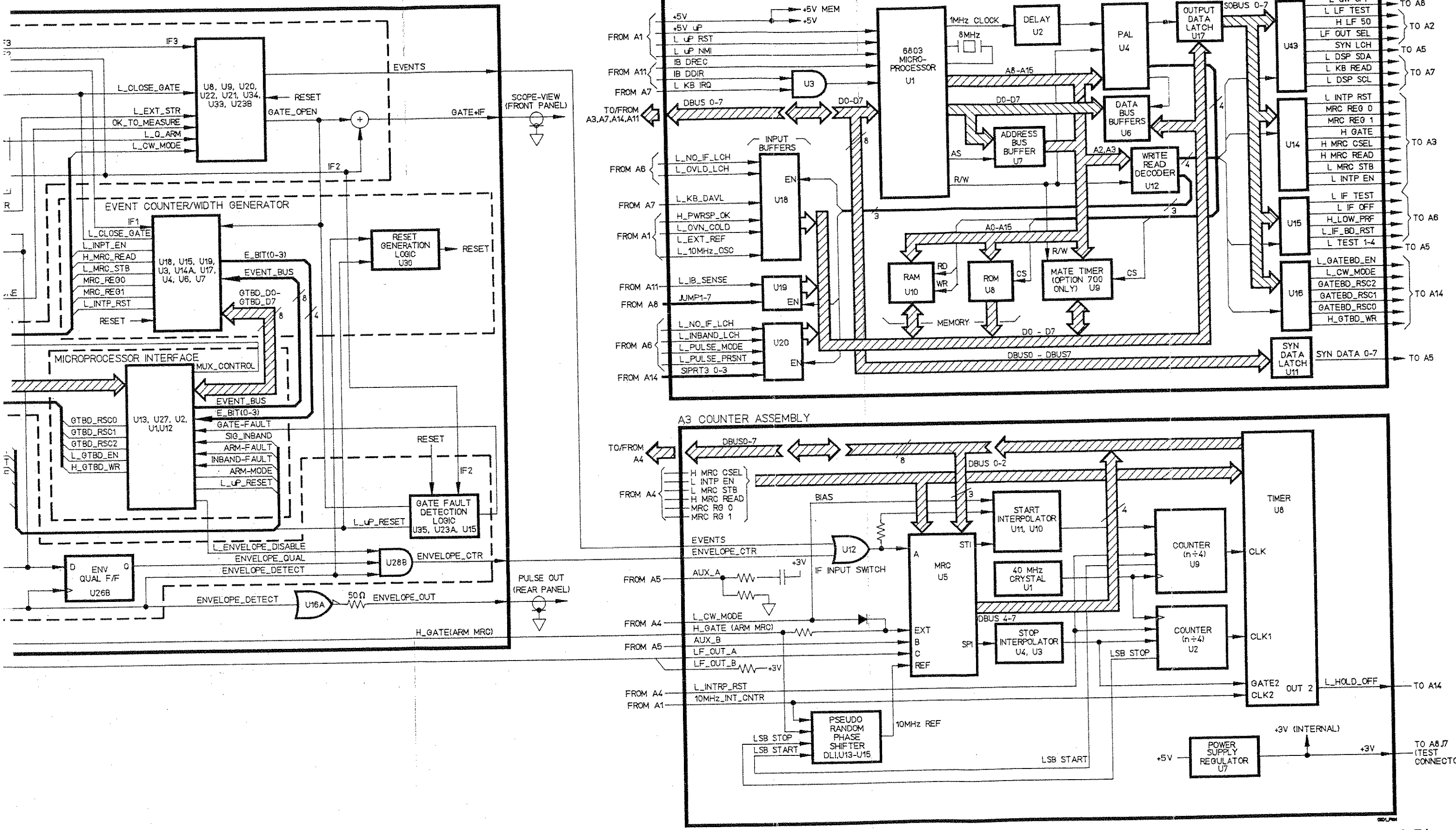


Figure 5-15. HP 5361B Overall Block Diagram (Sheet 1 of 2)

FRONT PANEL ASSEMBLY

A7 KEYBOARD/DISPLAY LOGIC ASSEMBLY

FROM A4 VIA A8.J10 THRU CABLE W1

L_DSP_SDA, L_DSP_SCL (2)

KEY ENCODER U4

KEYBOARD MICROPROCESSOR INTERFACE U2C, U2D, U3, U5D

DBUS3 - DBUS7

20-KEY MATRIX S2-S21

FRONT PANEL KEYBOARD

DISPLAY SYNCHRONIZATION TIMING U1

L_DSP_SDA, L_DSP_SCL (2)

L_KB_DAVL, L_KB_IRQ (2)

TO A4 VIA A8.J10 THRU CABLE W1

+5V

+15V

+5V

+5V

TO A9 VIA A8.J10 THRU CABLE W1

L STBY

TO A1 (POWER SUPPLY CONTROL) VIA A8.J10 THRU CABLE W1

FROM A1 (POWER SUPPLY CONTROL)

STBY LED

ON

POWER

STANDBY

STBY

A9 DISPLAY MODULE/DRIVERS

FROM A4 VIA A8.J10 THRU CABLE W1

DISPLAY DRIVERS

BACKLIGHT DISPLAY

LCD

FROM A1

L_uP_RST FROM A1 (PSC)

DBUS 0-3

TO/FROM A4

IB DVAL

IB DREC

IB DDIR

A8 MOTHERBOARD/POWER SUPPLY REGULATOR ASSEMBLY

FROM A1, A3, A7

DC VOLTAGES

TO POWER SUPPLY TEST CONNECTOR

V/-5.2V, +5V, +15V

I/-5.2V, +5V, +15V

RESISTOR NETWORK R1, R2

A13

AC IN

POWER MODULE

TRANSFORMER SECONDARIES T1

BRIDGE RECTIFIER CR13

+15V REGULATOR Q7

+15V DRIVE

FROM A1(PSC)

+15V

+15V V SENSE

+15V I SENSE

+15V UNREG

RECTIFIER CR11,CR12, CR15

+5V REGULATOR Q8, Q10

+5V DRIVE

FROM A1(PSC)

+5V

+5V V SENSE

+5V I SENSE

+5V UNREG

-5.2V REGULATOR Q9, Q11

-5.2V DRIVE

FROM A1(PSC)

-5.2V

-5.2V V SENSE

-5.2V I SENSE

RECTIFIER CR14

FAN REGULATOR Q2, Q6

FAN DRIVE

FROM A1(PSC)

-24V REGULATOR U1

-24V

TO A5, A10

-24V V SENSE

OVEN DRIVE

FROM A1(PSC)

L uW OFF FROM A4

+15V

+5V

MICROWAVE TURN_OFF Q1, Q3, Q4, Q5

+13V SW

+5V SW

TO A12

CONFIGURATION SWITCH S1A-S1G

TO A4

POWER SUPPLY CONTROL (PART OF A1 ASSEMBLY)

L OVN COLD FROM A1(TB8)

OVEN DRIVE Q21

+5V UNREG

+15V UNREG

+15V REF

+12V REF

BROWNOUT RECOVERY U15B

+15V I SENSE

+15V REGULATION AND CURRENT LIMIT Q12

+15V DRIVE Q10, Q13

+12V SUPPLY FOR P.S. CONTROL U2

LSTBY FROM A7 VIA A8.J10(12)

+15V V SENSE

+5V V SENSE

+5V I SENSE

-5.2V V SENSE

-5.2V I SENSE

-24V V SENSE

POWER SUPPLY STATUS

U7A-U7C, U8A, U8B, U14A, U14B

ELAPSED TIME COUNTER F1, R32, R33

FAN DRIVE Q22

-5.2V CURRENT LIMIT U15A, U15C, U15D

+5V REGULATION AND CURRENT U14C, U14D

+12V REF

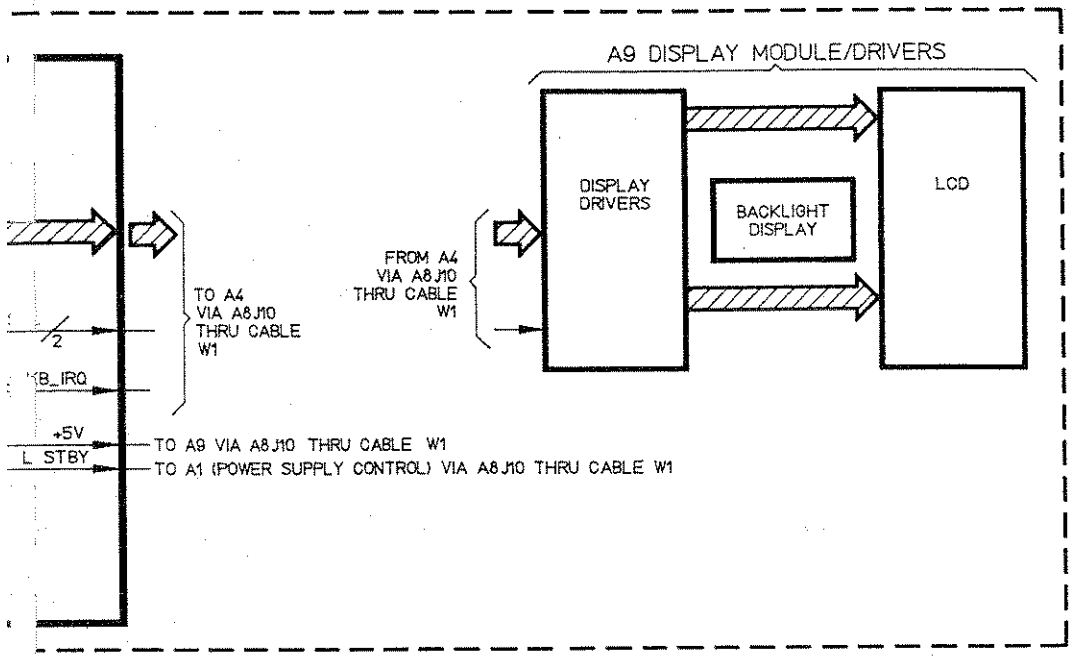
FROM A1 (TB8)

+5uP V SENSE

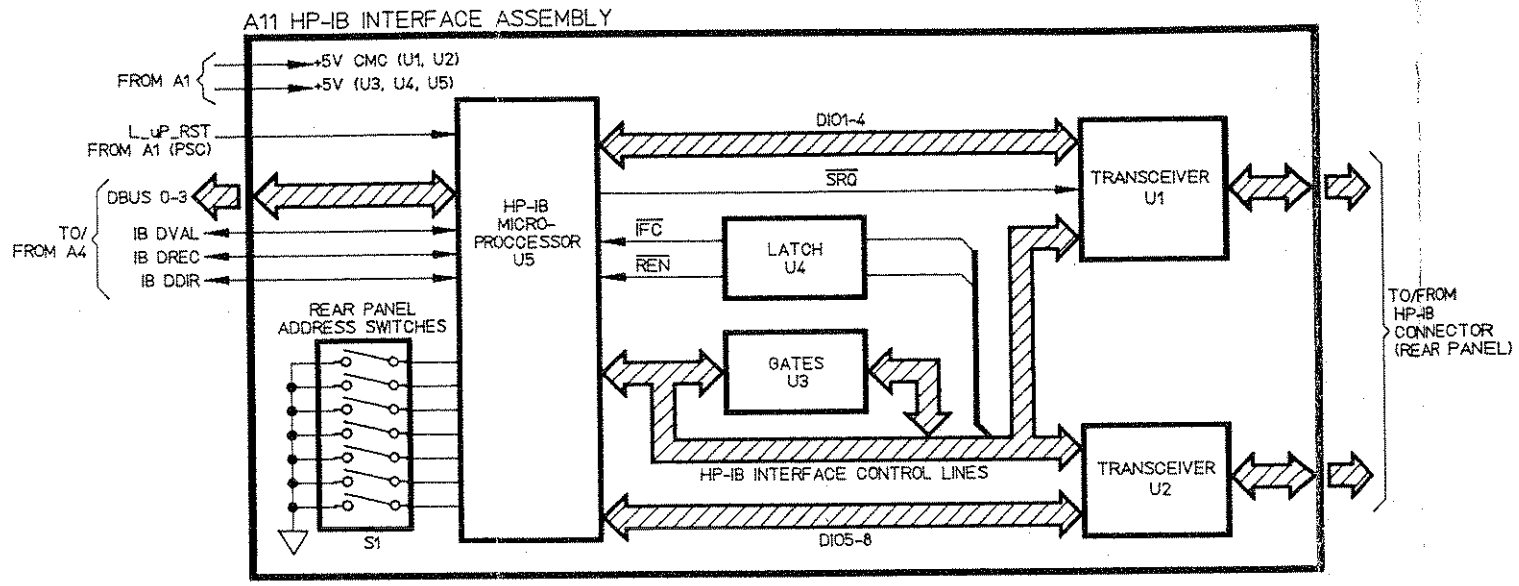
+5V OSC V SENSE

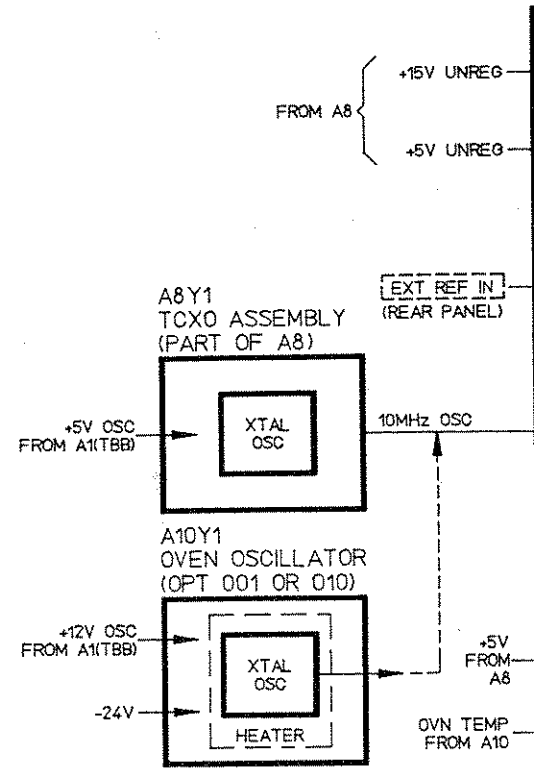
+12V OSC V SENSE

A9 DISPLAY MODULE/DRIVERS

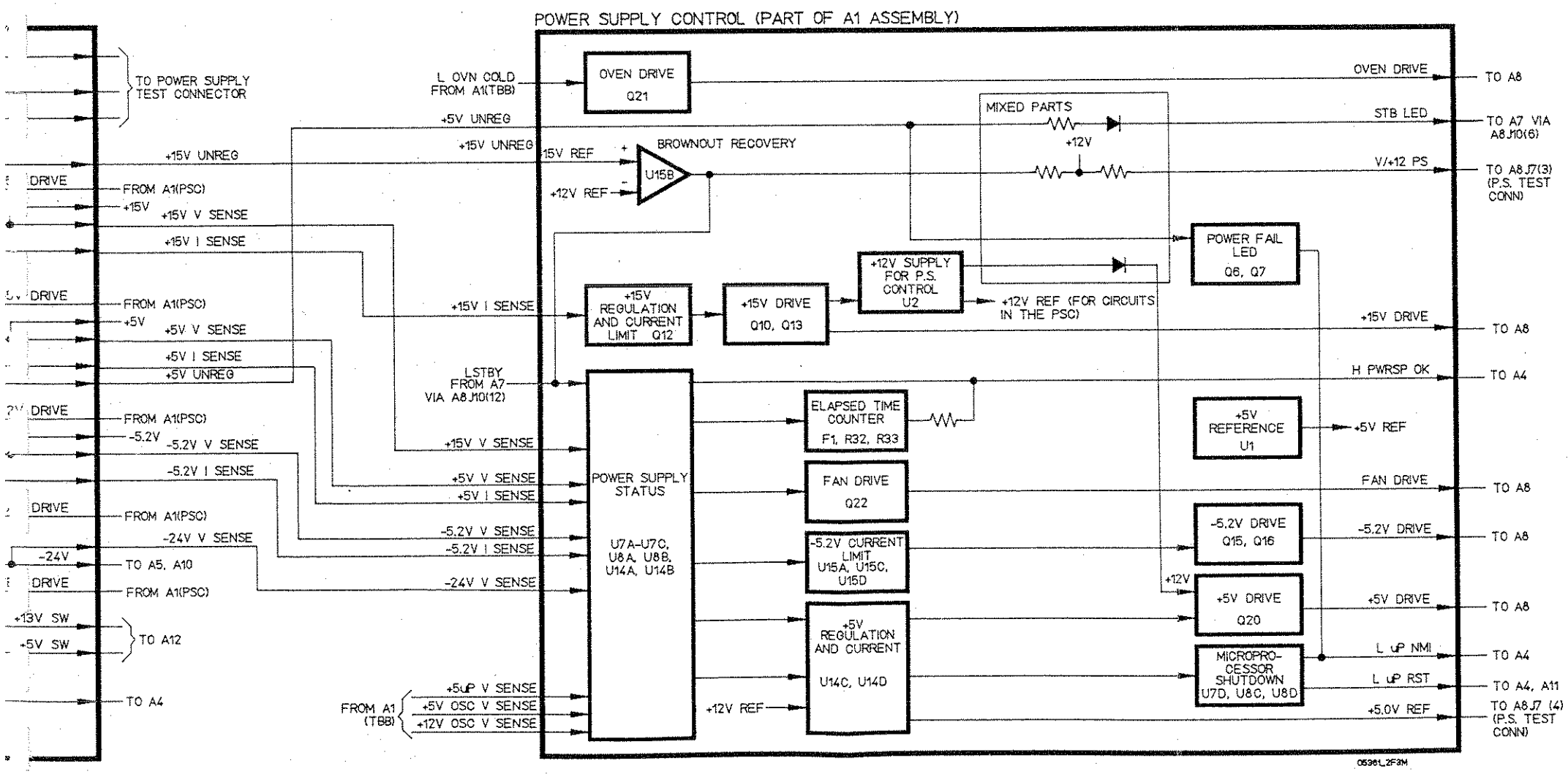


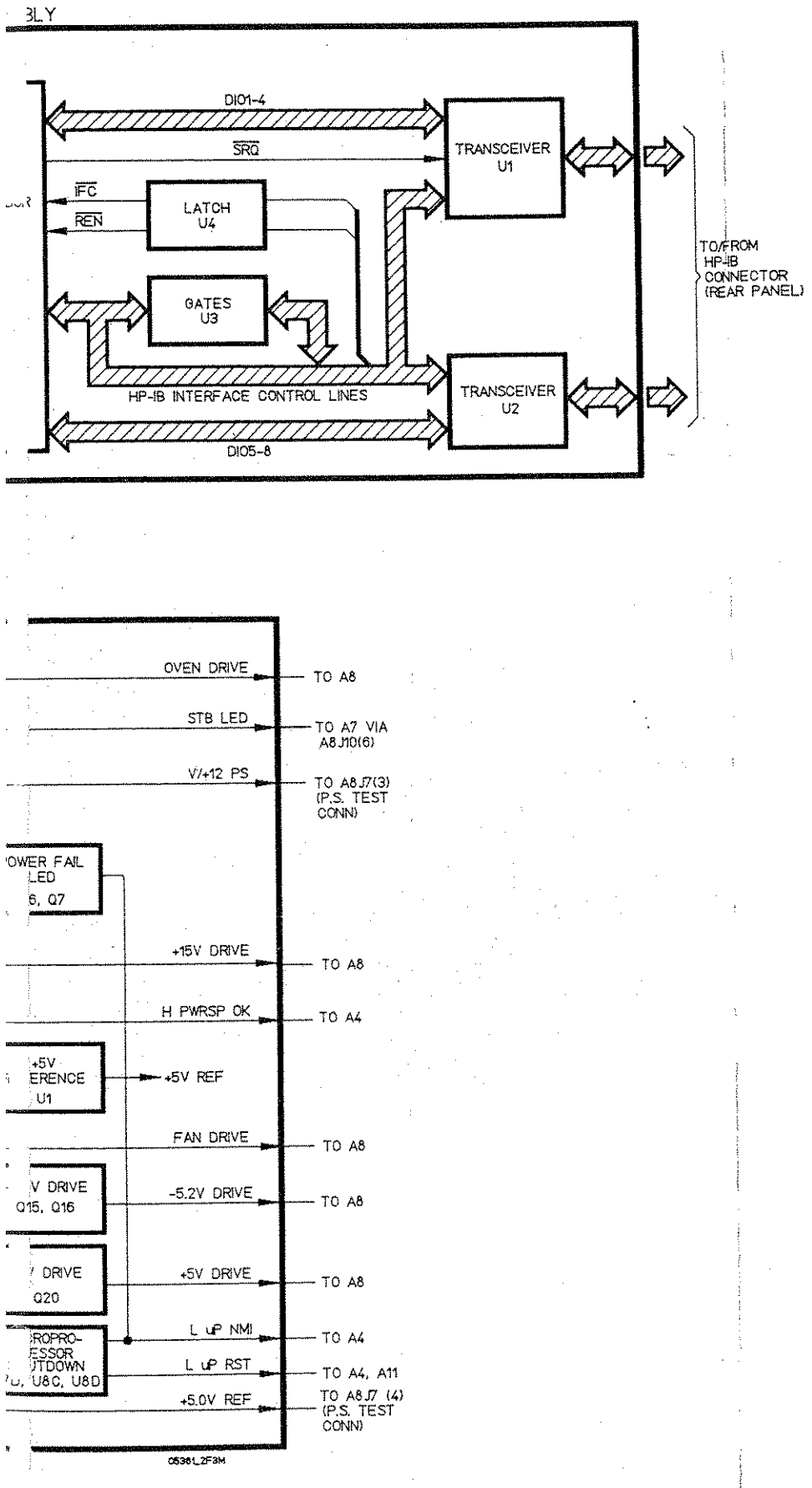
A11 HP-IB INTERFACE ASSEMBLY





POWER SUPPLY CONTROL (PART OF A1 ASSEMBLY)





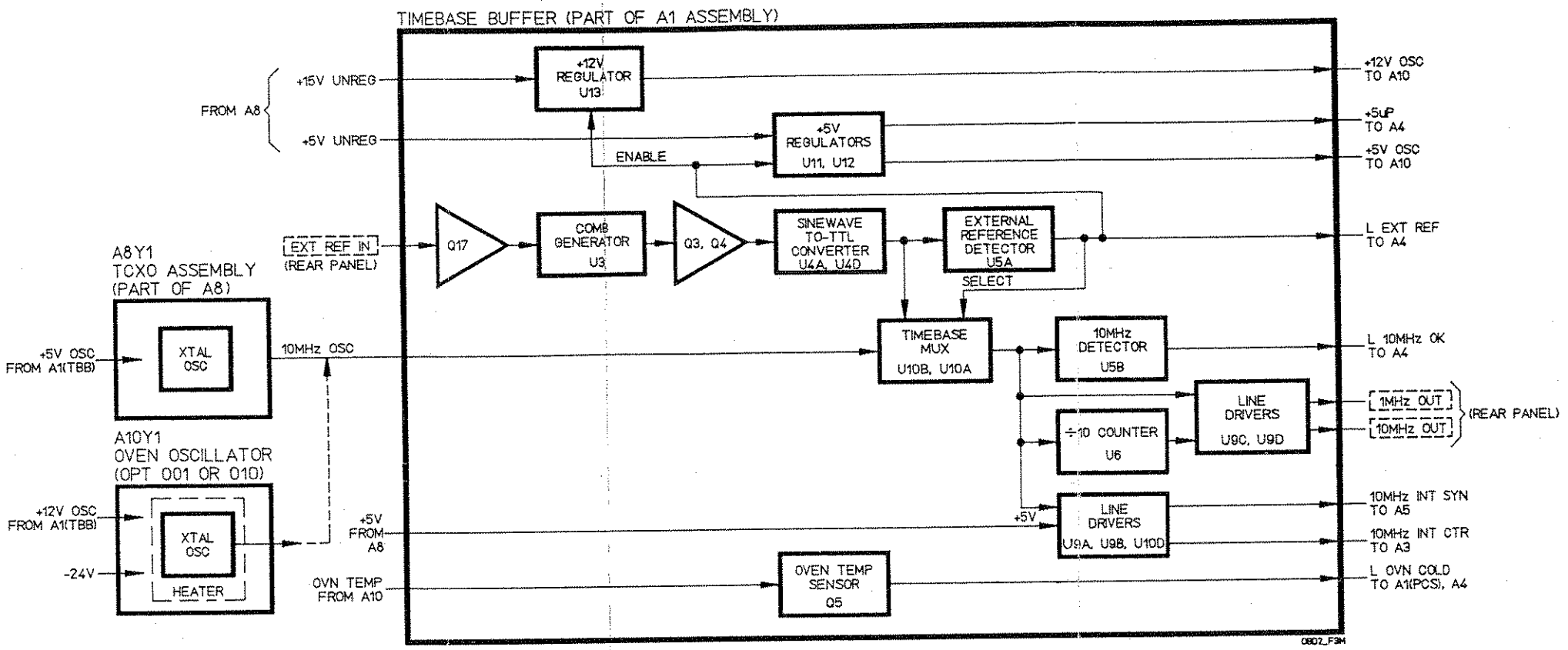


Figure 5-15. HP 5361B Overall Block Diagram
(Sheet 2 of 2)

TIMEBASE BUFFER/POWER SUPPLY CONTROL

XA1B

GND_MTHRPLN	1	26	GND_MTHRPLN
L_OVN_COLD	2	27	L_OVN_COLD
H_PWRSP_OK	3	28	H_PWRSP_OK
STBY_LED	4	29	STBY_LED
L_STBY	5	30	L_STBY
L_uP_RST	6	31	L_uP_RST
L_uP_NMI	7	32	L_uP_NMI
+12V_PS	8	33	+5V_REF
-24V	9	34	-24V
+15V	10	35	+15V
+15V_I_SENSE	11	36	+15V_I_SENSE
-5.2V	12	37	-5.2V
-5.2V_I_SENSE	13	38	-5.2V_I_SENSE
GND_PWRSPLY	14	39	GND_PWRSPLY
GND_PWRSPLY	15	40	GND_PWRSPLY
+5V	16	41	+5V
+5V_I_SENSE	17	42	+5V_I_SENSE
+15V_DRIVE	18	43	+15V_DRIVE
-5.2V_DRIVE	19	44	-5.2V_DRIVE
+5V_DRIVE	20	45	+5V_DRIVE
OVN_DRIVE	21	46	OVN_DRIVE
FAN_DRIVE	22	47	FAN_DRIVE
+15V_UNREG	23	48	+15V_UNREG
+-5V_RETURN	24	49	+-5V_RETURN
+5V_UNREG	25	50	+5V_UNREG

XA1A

EXT_REF_IN	1	26	EXT_REF_IN
GND_MTHRPLN	2	27	GND_MTHRPLN
GND_MTHRPLN	3	28	GND_MTHRPLN
10MHZ_INT_SYN	4	29	10MHZ_INT_SYN
GND_MTHRPLN	5	30	GND_MTHRPLN
GND_MTHRPLN	6	31	GND_MTHRPLN
10MHZ_INT_CTR	7	32	10MHZ_INT_CTR
GND_MTHRPLN	8	33	GND_MTHRPLN
GND_MTHRPLN	9	34	GND_MTHRPLN
10MHZ_OUT	10	35	10MHZ_OUT
GND_MTHRPLN	11	36	GND_MTHRPLN
GND_MTHRPLN	12	37	GND_MTHRPLN
1MHZ_OUT	13	38	1MHZ_OUT
GND_MTHRPLN	14	39	GND_MTHRPLN
L_EXT_REF	15	40	L_10MHZ_OK
GND_MTHRPLN	16	41	GND_MTHRPLN
10MHZ_OSC	17	42	10MHZ_OSC
GND_MTHRPLN	18	43	GND_MTHRPLN
L_OVN_COLD	19	44	OVEN_TEMP
+5V	20	45	+5V
+5V_OSC	21	46	+5V_OSC
+12V_OSC	22	47	+12V_OSC
+5V_uP	23	48	+5V_uP
+15V_UNREG	24	49	+15V_UNREG
+5V_UNREG	25	50	+5V_UNREG

LOW FREQUENCY INPUT ASSEMBLY

XA2

GND_MTHRPLN	1	26	GND_MTHRPLN
LF_OUT_B	2	27	GND_MTHRPLN
LF_OUT_A	3	28	GND_MTHRPLN
GND_MTHRPLN	4	29	GND_MTHRPLN
A2_TEST	5	30	A2_TEST
	6	31	
	7	32	
GND_MTHRPLN	8	33	GND_MTHRPLN
LF_OUT_SEL	9	34	
	10	35	
	11	36	
L_LF_TEST	12	37	
	13	38	GND_MTHRPLN
	14	39	
+5V	15	40	+5V
	16	41	
	17	42	
	18	43	
	19	44	
	20	45	
+15V	21	46	+15V
GND_MTHRPLN	22	47	GND_MTHRPLN
H_LF_50	23	48	
-5.2V	24	49	-5.2V
AUX_B	25	50	AUX_A

COU

+5V	1		
GND_DIGITAL	2		
	3		
L_CW_MODE	4		
GND_DIGITAL	5		
DBUS_0	6		
DBUS_2	7		
DBUS_4	8		
DBUS_6	9		
GND_DIGITAL	10		
L_INTP_RST	11		
MRC_REG0	12		
MRC_REG1	13		
ARM_MRC	14		
H_GATE	15		
GND_DIGITAL	16		
GND_DIGITAL	17		
GND_DIGITAL	18		
GND_DIGITAL	19		
EVENTS	20		
L_HOLDOFF	21		
H_10MHZ_DISABLE	22		
-5.2V	23		
IF_MON_RTN	24		
IF_MON_OUT	25		

P

SYNTHESIZER ASSEMBLY

XA5

10MHZ_INT_SYN	1	26	GND_MTHRPLN
GND_MTHRPLN	2	27	10MHZ_INT_SYN
GND_MTHRPLN	3	28	GND_MTHRPLN
SYN_DATA_0	4	29	SYN_DATA_0
SYN_DATA_1	5	30	SYN_DATA_1
SYN_DATA_2	6	31	SYN_DATA_2
SYN_DATA_3	7	32	SYN_DATA_3
SYN_DATA_4	8	33	SYN_DATA_4
SYN_DATA_5	9	34	SYN_DATA_5
SYN_DATA_6	10	35	SYN_DATA_6
SYN_DATA_7	11	36	SYN_DATA_7
SYN_LCH	12	37	SYN_LCH
GND_MTHRPLN	13	38	GND_MTHRPLN
-24V	14	39	-24V
-5.2V	15	40	-5.2V
+15V	16	41	+15V
GND_MTHRPLN	17	42	GND_MTHRPLN
+5V	18	43	+5V
+5V	19	44	+5V
GND_MTHRPLN	20	45	GND_MTHRPLN
L_TEST_2	21	46	L_TEST_1
L_TEST_3	22	47	L_TEST_4
GND_MTHRPLN	23	48	GND_MTHRPLN
AUX_A	24	49	AUX_B
AUX_B	25	50	AUX_A

MICROPROCESSOR ASSEMBLY

XA4A

SYN_DATA_0	1	26	SYN_DATA_1
SYN_DATA_2	2	27	SYN_DATA_3
SYN_DATA_4	3	28	SYN_DATA_5
SYN_DATA_6	4	29	SYN_DATA_7
GND_DIGITAL	5	30	GND_DIGITAL
SYN_LCH	6	31	IB_DDIR
IB_DREC	7	32	IB_DVAL
	8	33	L_KB_IRQ
DBUS_0	9	34	DBUS_1
DBUS_2	10	35	DBUS_3
DBUS_4	11	36	DBUS_5
DBUS_6	12	37	DBUS_7
GND_DIGITAL	13	38	GND_DIGITAL
L_uP_RST	14	39	
L_uP_NMI	15	40	
+5V_uP	16	41	
SYN_LCH	17	42	L_DSP_SCL
L_KB_READ	18	43	L_DSP_SDA
L_uN_OFF	19	44	L_LF_TEST
H_LF_50	20	45	LF_OUT_SEL
GND_DIGITAL	21	46	GND_DIGITAL
L_INTP_EN	22	47	L_INTP_RST
L_MRC_STB	23	48	MRC_REG0
H_MRC_CSEL	24	49	MRC_REG1
H_MRC_READ	25	50	H_GATE

XA4B

L_TEST_4	1	26	L_TEST_1
L_TEST_2	2	27	L_TEST_3
L_NO_IF_RST (LOW PRF)	3	28	L_IF_BD_RST
L_IF_TEST	4	29	L_IF_OFF
GND_DIGITAL	5	30	GND_DIGITAL
	6	31	L_GATEBD_EN
H_10MHZ_DISABLE	7	32	L_CW_MODE
GATEBD_RSC1	8	33	GATEBD_RSC2
H_GIBD_WR	9	34	GATEBD_RSC0
L_10MHZ_OK	10	35	L_EXT_REF
L_OVN_COLD	11	36	H_PWRSP_OK
L_KB_DAVL	12	37	
L_OVLD_LCH	13	38	L_NO_IF_LCH
GND_DIGITAL	14	39	GND_DIGITAL
L_IB_SENSE	15	40	L_JMP1
L_JMP2	16	41	L_JMP3
L_JMP4	17	42	L_JMP5
L_JMP6	18	43	L_JMP7
L_PULSE_MODE	19	44	L_IN_BAND_LCH
L_IF_PRSNT	20	45	L_PULSE_PRSNT
(SIPRT3_3)	21	46	SIPRT3_2
SIPRT3_1	22	47	SIPRT3_0
GND_DIGITAL	23	48	GND_DIGITAL
GND_DIGITAL	24	49	+5V
+5V	25	50	+5V

+5V_UP_TEST	
-24V_TEST	
+12V_PS	
+5V_REF	
GND_PWRSPLY	
L_STBY	
+15V_TEST	
+15V_I	
A2_TEST	
	1

MICR

+13V_SW	
GND_MTHRPLN	
+5V_SW	
-5.2V	
GND_MTHRPLN	
+15V	
-5.2V	
-5.2V	
+5V	1

QUENCY INPUT ASSEMBLY

XA2

LN	1	26	GND_MTHRPLN
	2	27	GND_MTHRPLN
	3	28	GND_MTHRPLN
L	4	29	GND_MTHRPLN
	5	30	A2_TEST
	6	31	
	7	32	
	8	33	GND_MTHRPLN
	9	34	
	10	35	
	11	36	
	12	37	
	13	38	GND_MTHRPLN
	14	39	
	15	40	+5V
	16	41	
	17	42	
	18	43	
	19	44	
	20	45	
	21	46	+15V
	22	47	GND_MTHRPLN
	23	48	
	24	49	-5.2V
	25	50	AUX_A

COUNTER ASSEMBLY

XA3

+5V	1	26	+5V
GND_DIGITAL	2	27	GND_DIGITAL
	3	28	+3V
L_CW_MODE	4	29	10MHZ_INT_CTR
GND_DIGITAL	5	30	GND_MTHRPLN
DBUS_0	6	31	DBUS_1
DBUS_2	7	32	DBUS_3
DBUS_4	8	33	DBUS_5
DBUS_6	9	34	DBUS_7
GND_DIGITAL	10	35	GND_DIGITAL
L_INTP_RST	11	36	L_INTP_EN
MRC_REG0	12	37	L_MRC_STB
MRC_REG1	13	38	H_MRC_CSEL
ARM_MRC	14	39	H_MRC_READ
H_GATE	15	40	GND_DIGITAL
GND_DIGITAL	16	41	GND_DIGITAL
GND_DIGITAL	17	42	LF_OUT_B
GND_DIGITAL	18	43	LF_OUT_A
GND_DIGITAL	19	44	GND_DIGITAL
EVENTS	20	45	ENVELOPE_CTR
L_HOLDOFF	21	46	AUX_B
H_10MHZ_DISABLE	22	47	AUX_A
-5.2V	23	48	-5.2V
IF_MON_RTN	24	49	IF_OUT
IF_MON_OUT	25	50	IF_RTN

IF AMP/DET ASSEMBLY

XA6

L_OVLD_LCH	1	26	L_OVLD_LCH
	2	27	H_ENVELOPE_IF
L_IF_BD_RST	3	28	L_IF_BD_RST
L_NO_IF_LCH	4	29	L_NO_IF_LCH
L_NO_IF_RST(LOW PRF)	5	30	L_NO_IF_RST(LOW PRF)
+IF_NEW	6	31	-IF_NEW
GND_MTHRPLN	7	32	GND_MTHRPLN
AUX_A	8	33	AUX_A
GND_MTHRPLN	9	34	GND_MTHRPLN
GND_MTHRPLN	10	35	GND_MTHRPLN
+5V	11	36	-5.2V
L_IF_OFF	12	37	L_IF_OFF
L_IF_TEST	13	38	L_IF_TEST
GND_MTHRPLN	14	39	GND_MTHRPLN
GND_MTHRPLN	15	40	L_IF_BAND
L_PULSE_PRSNT	16	41	GND_MTHRPLN
-5.2V	17	42	-5.2V
L_IF_PRSNT	18	43	+15V
+5V	19	44	+5V
GND_MTHRPLN	20	45	GND_MTHRPLN
L_PULSE_MOD	21	46	L_IN_BAND_LCH
GND_MTHRPLN	22	47	GND_MTHRPLN
GND_MTHRPLN	23	48	IF_RTN
GND_MTHRPLN	24	49	IF_OUT (IF_MON)
GND_MTHRPLN	25	50	GND_MTHRPLN

A14 GATE BOARD ASSEMBLY

XA14

+5V	1	31	GND_DIGITAL
+5V	2	32	GND_DIGITAL
DBUS_0	3	33	DBUS_1
DBUS_2	4	34	DBUS_3
DBUS_4	5	35	DBUS_5
DBUS_6	6	36	DBUS_7
GND_DIGITAL	7	37	GND_DIGITAL
	8	38	ARM_MRC
H_GATE	9	39	H_MRC_READ
L_MRC_STB	10	40	SIPRT3_2
SIPRT3_1	11	41	SIPRT3_0
MRC_REG0	12	42	GND_MTHRPLN
MRC_REG1	13	43	L_HOLDOFF
ENVELOPE_CTR	14	44	ENVELOPE_OUT
L_IF_BAND	15	45	L_INTP_RST
	16	46	GND_DIGITAL
	17	47	GND_DIGITAL
H_GTBD_WR	18	48	GATEBD_RSC0
GATEBD_RSC1	19	49	GATEBD_RSC2
	20	50	L_GATEBD_EN
H_ENVELOPE_IF	21	51	L_CW_MODE
GND_MTHRPLN	22	52	GND_DIGITAL
-IF_NEW	23	53	GND_MTHRPLN
+IF_NEW	24	54	GND_MTHRPLN
GND_MTHRPLN	25	55	EVENTS
AUX_B	26	56	GND_DIGITAL
-5.2V	27	57	(AUX_A)
-5.2V	28	58	GND_DIGITAL
-5.2V	29	59	GND_DIGITAL
-5.2V	30	60	GND_DIGITAL

POWER SUPPLY TEST

J7

+5V_UP_TEST	1	11	+5V_OSC_TEST
-24V_TEST	2	12	+12V_OSC_TEST
+12V_PS	3	13	+3V
+5V_REF	4	14	-V_FAN
GND_PWRSPLY	5	15	+5V_I
L_STBY	6	16	+5V_TEST
+15V_TEST	7	17	-5.2V_I
+15V_I	8	18	-5.2V_TEST
A2_TEST	9	19	A2_TEST
	10	20	

FRONT PANAL KEYBOARD/DISPLAY ASSY.

J10

L_DSP_SCL	1	9	GND_DIGITAL
+5V	2	10	
+15V	3	11	L_KB_IRQ
L_KB_DAVL	4	12	L_STBY
L_DSP_SDA	5	13	L_KB_READ
STBY_LED	6	14	DBUS_3
DBUS_4	7	15	DBUS_5
DBUS_6	8	16	DBUS_7

OVEN OSCILLATOR (USE IS OPIONAL)

XA10

10MHZ_OSC	1		
GND_MTHRPLN	2		
+12V_OSC	3		
GND_MTHRPLN	4		
GND_MTHRPLN	5		
GND_MTHRPLN	6		
+5V_OSC	7		
	8		
	9		
	10		
OVEN_TEMP	11		
	12		
	13		
GND_OVN	14		
-24V	15		

XA4B

	1	26	L_TEST_1
	2	27	L_TEST_3
W_PRF)	3	28	L_IF_BD_RST
	4	29	L_IF_OFF
ITAL	5	30	GND_DIGITAL
	6	31	L_GATEBD_EN
SABLE	7	32	L_CW_MODE
	8	33	GATEBD_RSC2
	9	34	GATEBD_RSC0
OK	10	35	L_EXT_REF
OLD	11	36	H_PWRSP_OK
	12	37	
	13	38	L_NO_IF_LCH
L+HL	14	39	GND_DIGITAL
NSE	15	40	L_JMP1
	16	41	L_JMP3
	17	42	L_JMP5
	18	43	L_JMP7
MODE	19	44	L_IN_BAND_LCH
SNT	20	45	L_PULSE_PRSNT
	21	46	SIPRT3_2
	22	47	SIPRT3_0
	23	48	GND_DIGITAL
ITAL	24	49	+5V
	25	50	+5V

MICROWAVE

J11

	1	
+13V_SW	2	
GND_MTHRPLN	3	
+5V_SW	4	
-5.2V	5	
GND_MTHRPLN	6	
+15V	7	
-5.2V	8	
-5.2V	9	
+5V	10	

HP-IB

J6

IB_DDIR	1	
IB_DREC	2	
IB_DVAL	3	
DBUS_0	4	
DBUS_1	5	
DBUS_2	6	
DBUS_3	7	
L_IB_SENSE	8	
L_uP_RST	9	
GND_DIGITAL	10	
GND_CMC	11	
GND_CMC	12	
+5V_CMC	13	
+5V	14	

FAN

J5

GND_MTHRPLN	1	
-V_FAN	2	

TRANSFORMER SECONDARY OUTPUTS

J9

GRY_J9_1	1	
VIO_J9_2	2	
VIO_J9_3	3	

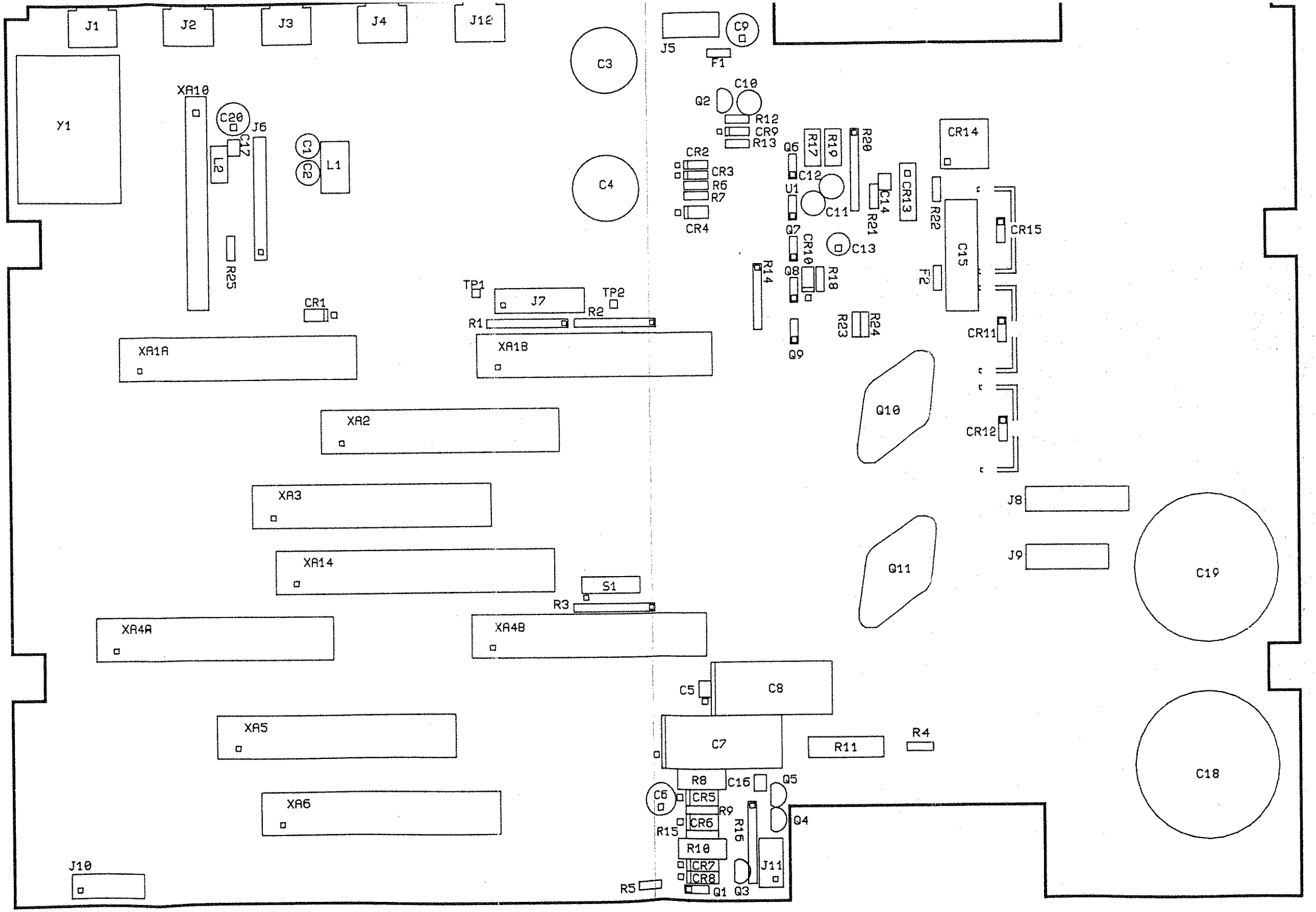
J8

GRN_J8_1	1	
RED_J8_2	2	
BRN_J8_3	3	
YEL_J8_4	4	

REAR PANEL BNC'S

J4	1	IF_MON_OUT
	2	IF_MON_RTN
J2	1	10MHZ_OUT
	2	GND_MTHRPLN
J3	1	1MHZ_OUT
	2	GND_MTHRPLN
J1	1	EXT_REF_IN
	2	GND_MTHRPLN
J12	1	ENVELOPE_OUT
	2	GND_MTHRPLN

Figure 5-16. A8 Interconnections



P/O Figure 5-17. A8 Component Locator

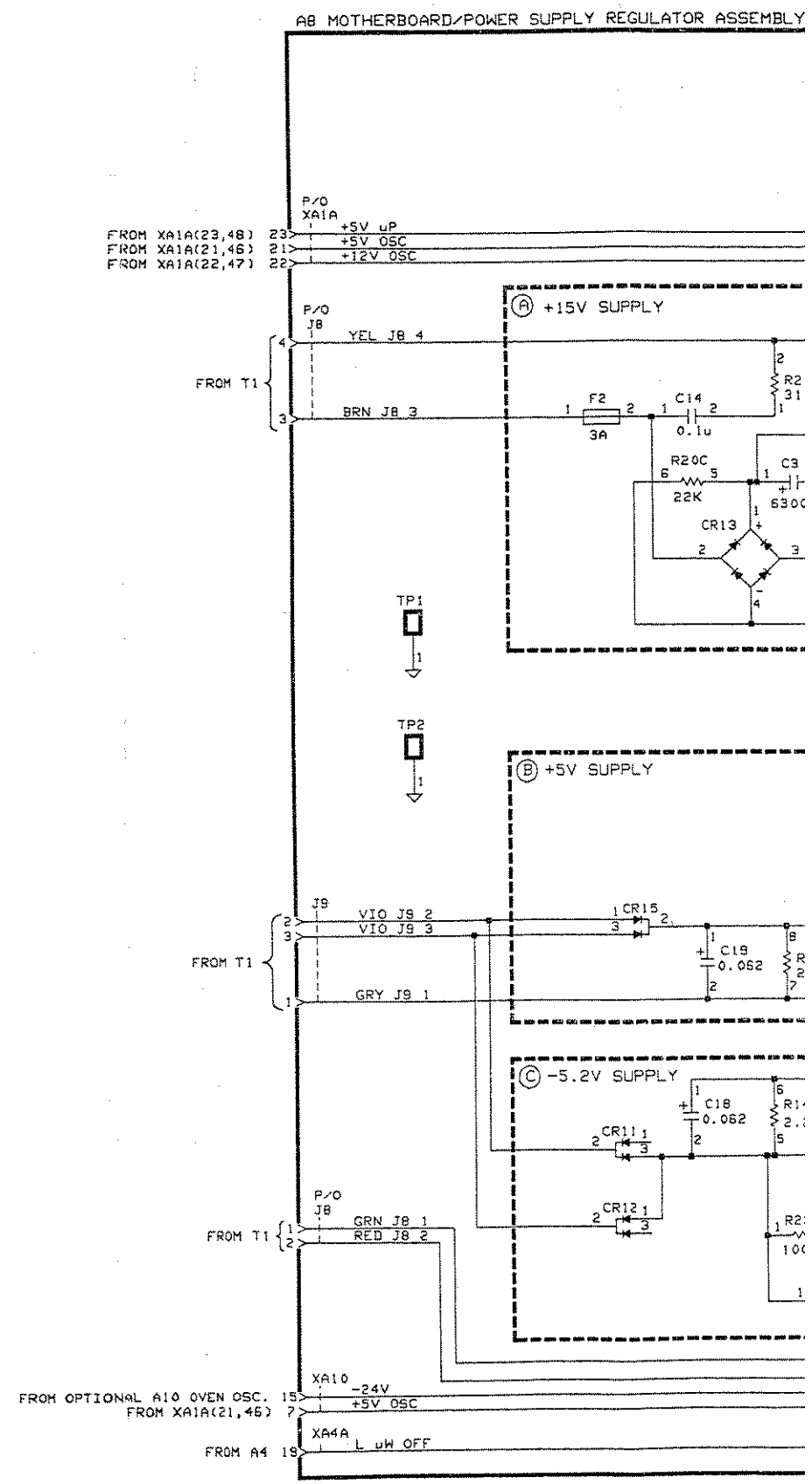
A8 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A8 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN FARADS, INDUCTANCE IN HENRIES.

3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.

4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.



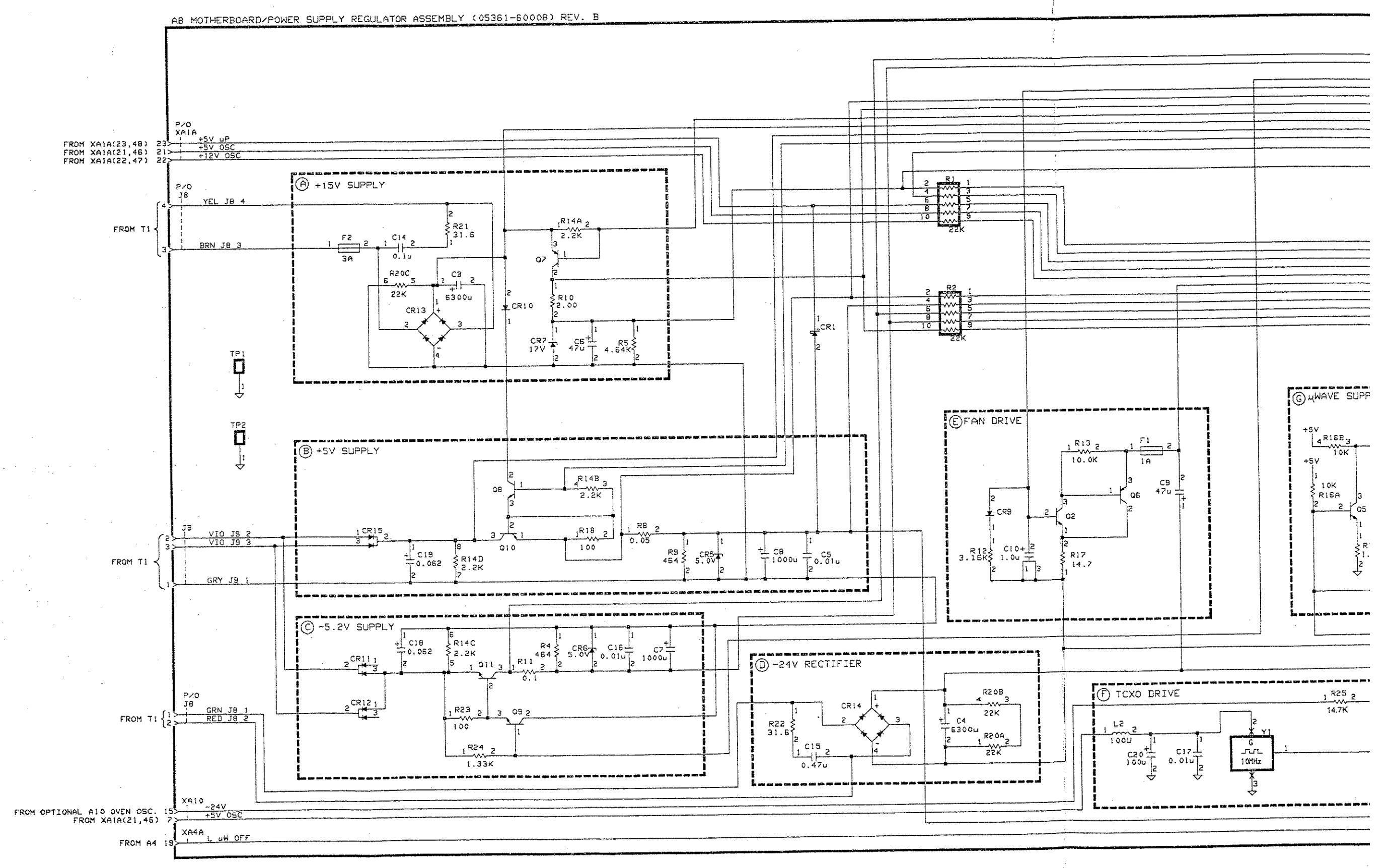
A8 MOTHERBOARD/POWER SUPPLY REGULATOR ASSEMBLY (05361-60008) REV. B

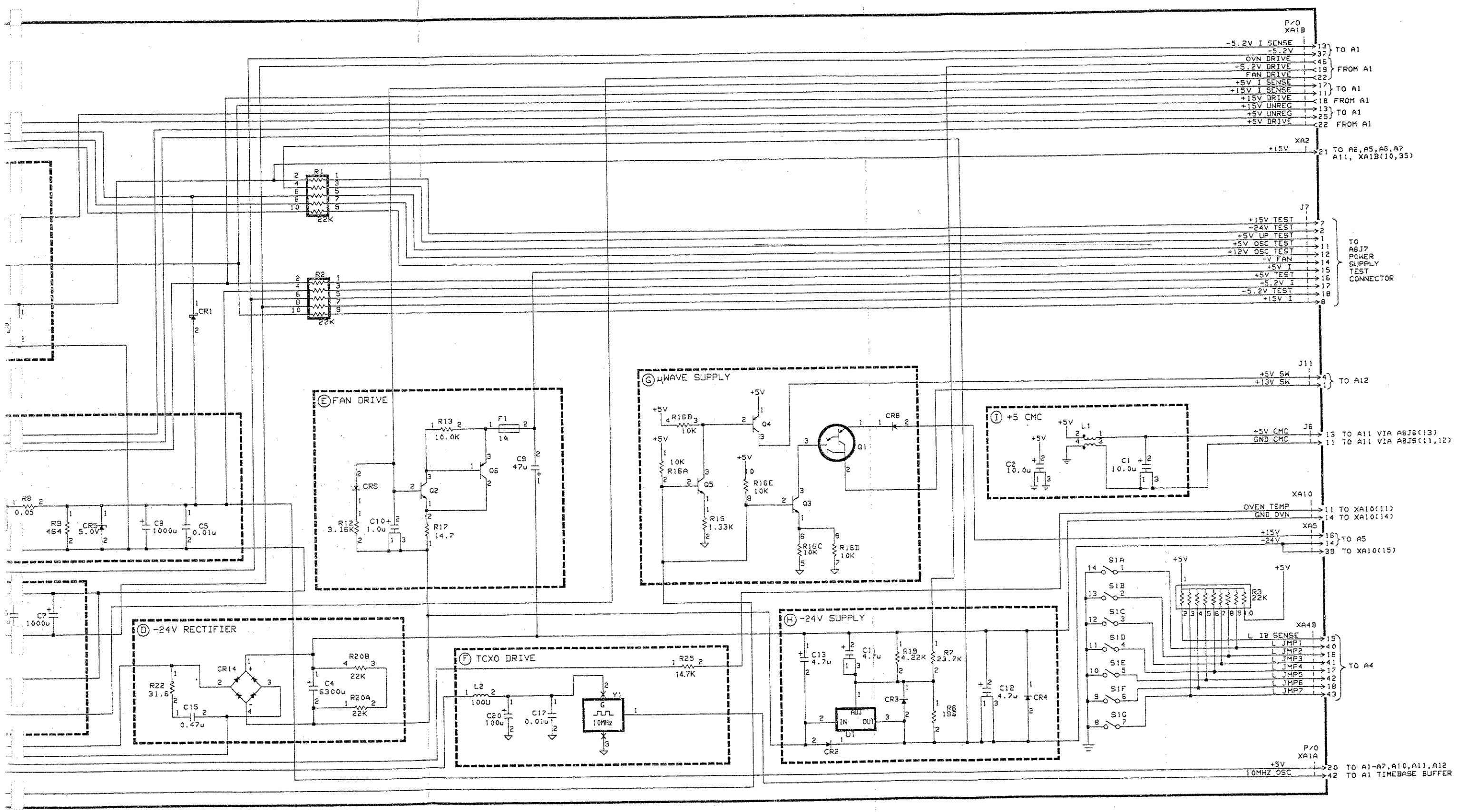
SEMBLY
BER TO
ON.

NCE IN
NCE IN

D COM-

ES A NEGA-





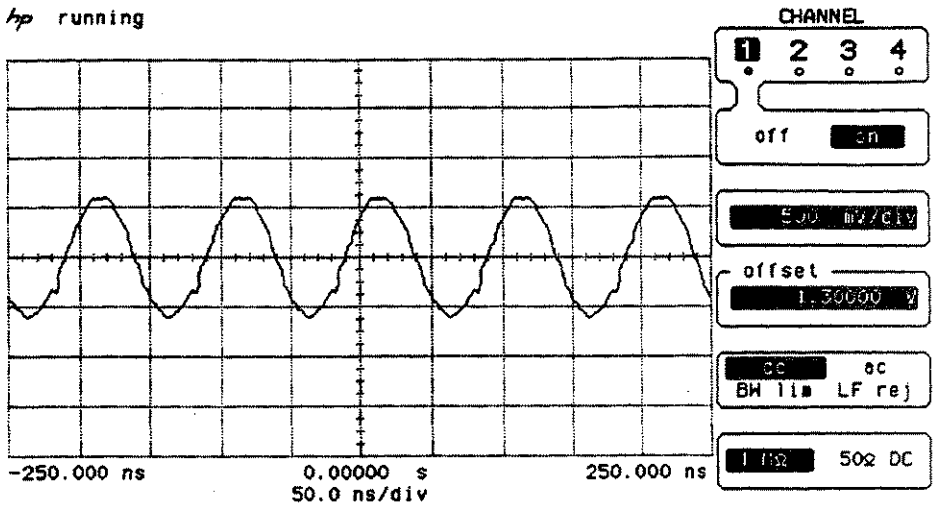
P/O Figure 5-17. A8 Motherboard/Power Supply Regulator Assembly Schematic Diagram

WAVEFORM A

TEST POINT: A1Q17 COLLECTOR

COUNTER SETUP: EXT. REF. IN. (REAR PANEL)

COUNTER INPUT: 10 MHZ, -5 DBM

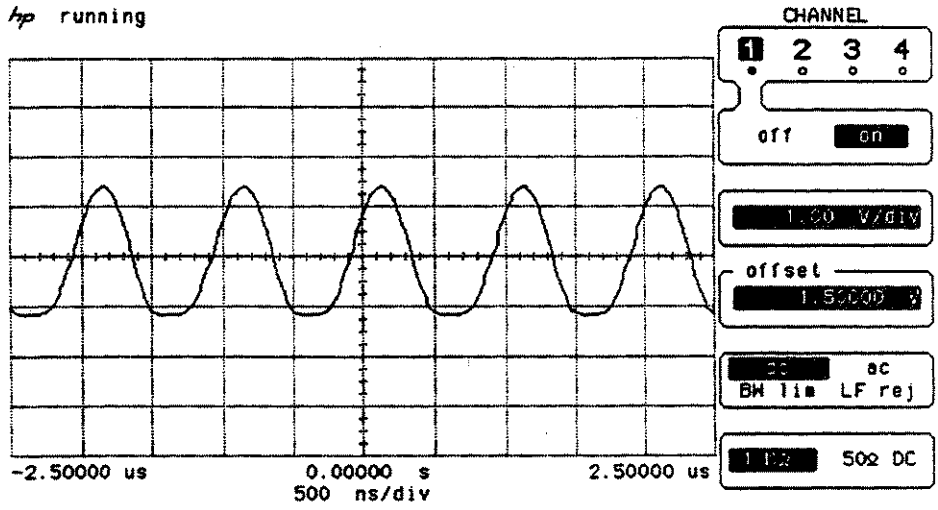


WAVEFORM B

TEST POINT: A1Q17 COLLECTOR

COUNTER SETUP: EXT. REF. IN. (REAR PANEL)

COUNTER INPUT: 1 MHZ, -5 DBM

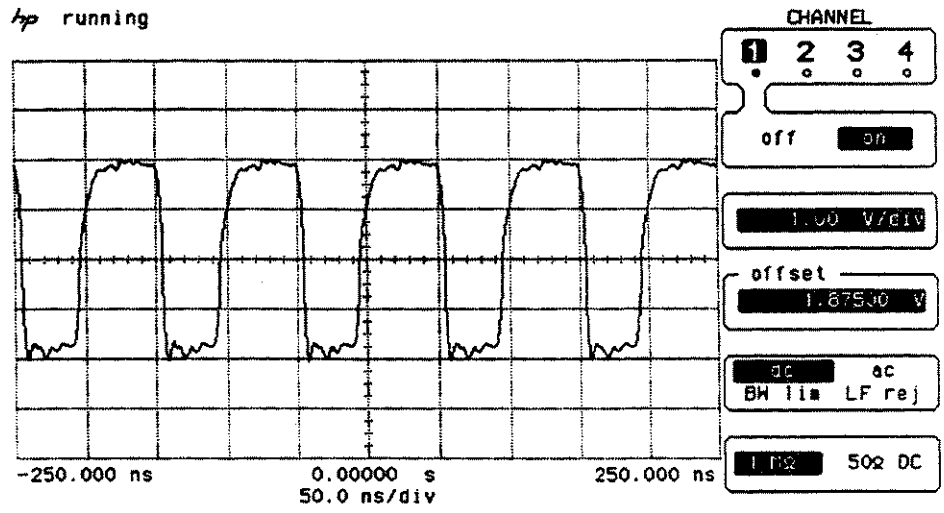


WAVEFORM C

TEST POINT: A1U3(4)

COUNTER SETUP: EXT. REF. IN. (REAR PANEL)

COUNTER INPUT: 10 MHZ, -5 DBM



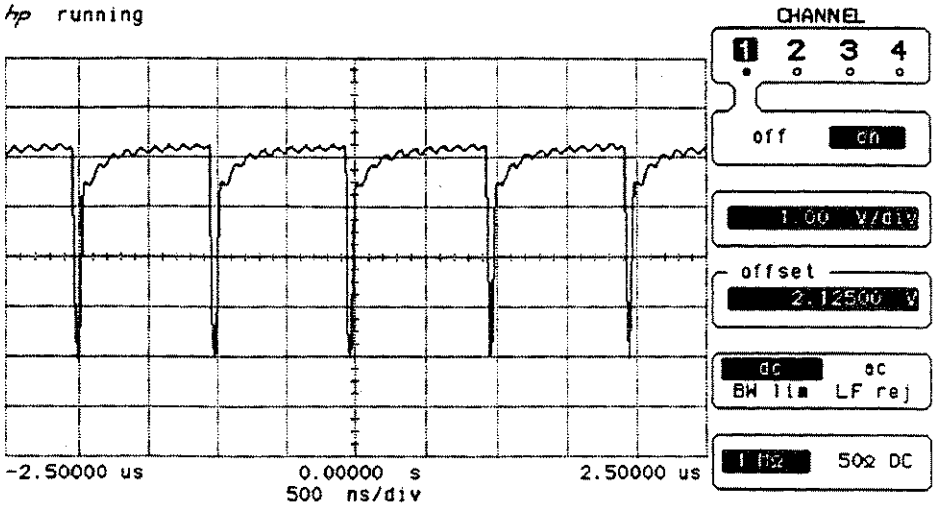
P/O Figure 5-18. A1 Waveforms

WAVEFORM D

TEST POINT: A1U3(4)

COUNTER SETUP: EXT. REF. IN. (REAR PANEL)

COUNTER INPUT: 1 MHZ, -5 DBM

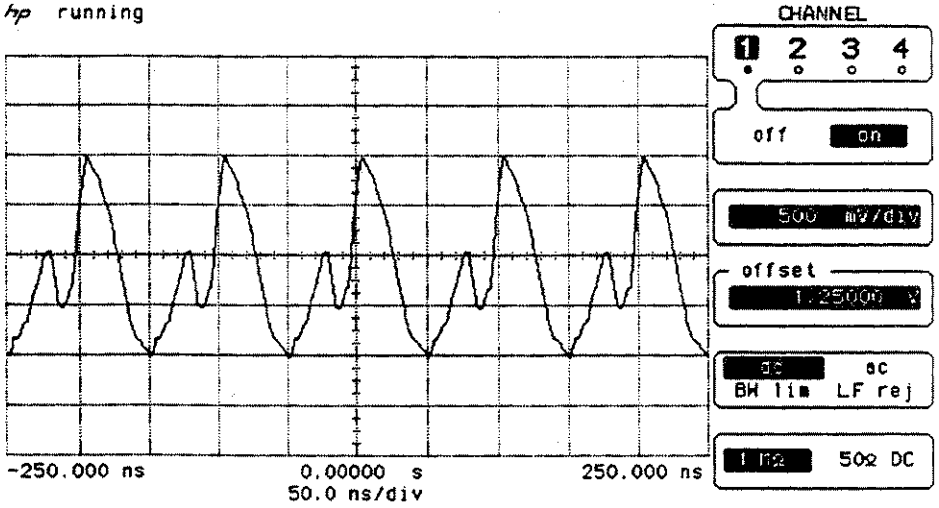


WAVEFORM E

TEST POINT: A1Q4 EMITTER

COUNTER SETUP: EXT. REF. IN. (REAR PANEL)

COUNTER INPUT: 10 MHZ, -5 DBM

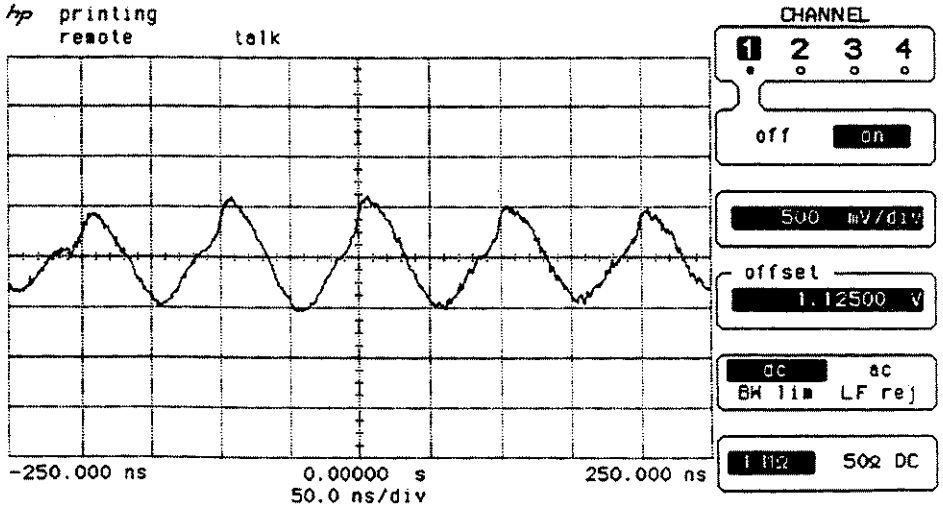


WAVEFORM F

TEST POINT: A1Q4 EMITTER

COUNTER SETUP: EXT. REF. IN. (REAR PANEL)

COUNTER INPUT: 1 MHZ, -5 DBM



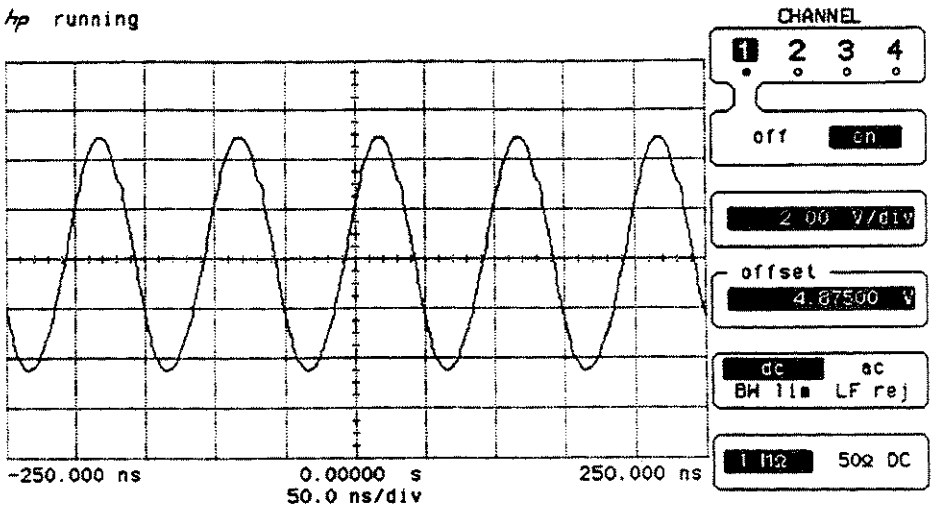
P/O Figure 5-18. A1 Waveforms

WAVEFORM G

TEST POINT: A1Q3 COLLECTOR

COUNTER SETUP: EXT. REF. IN. (REAR PANEL)

COUNTER INPUT: 10 MHZ, –5 DBM

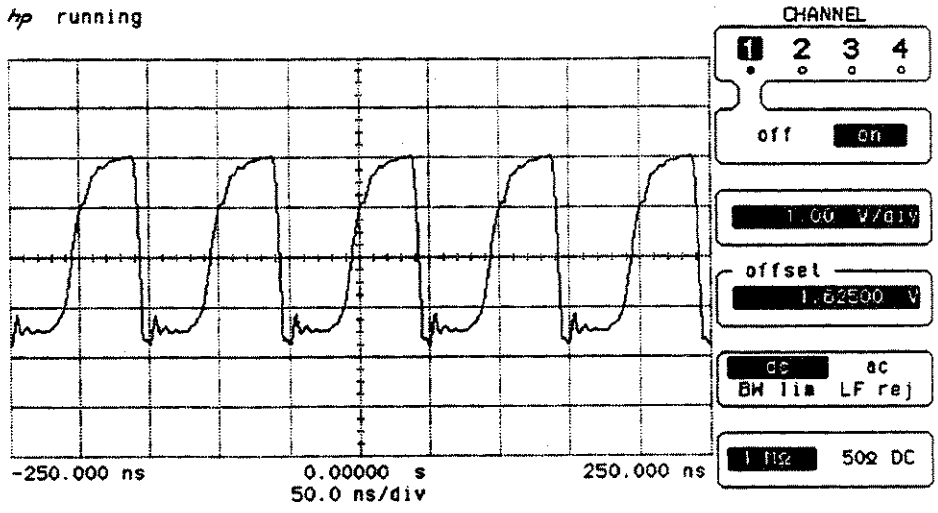


WAVEFORM H

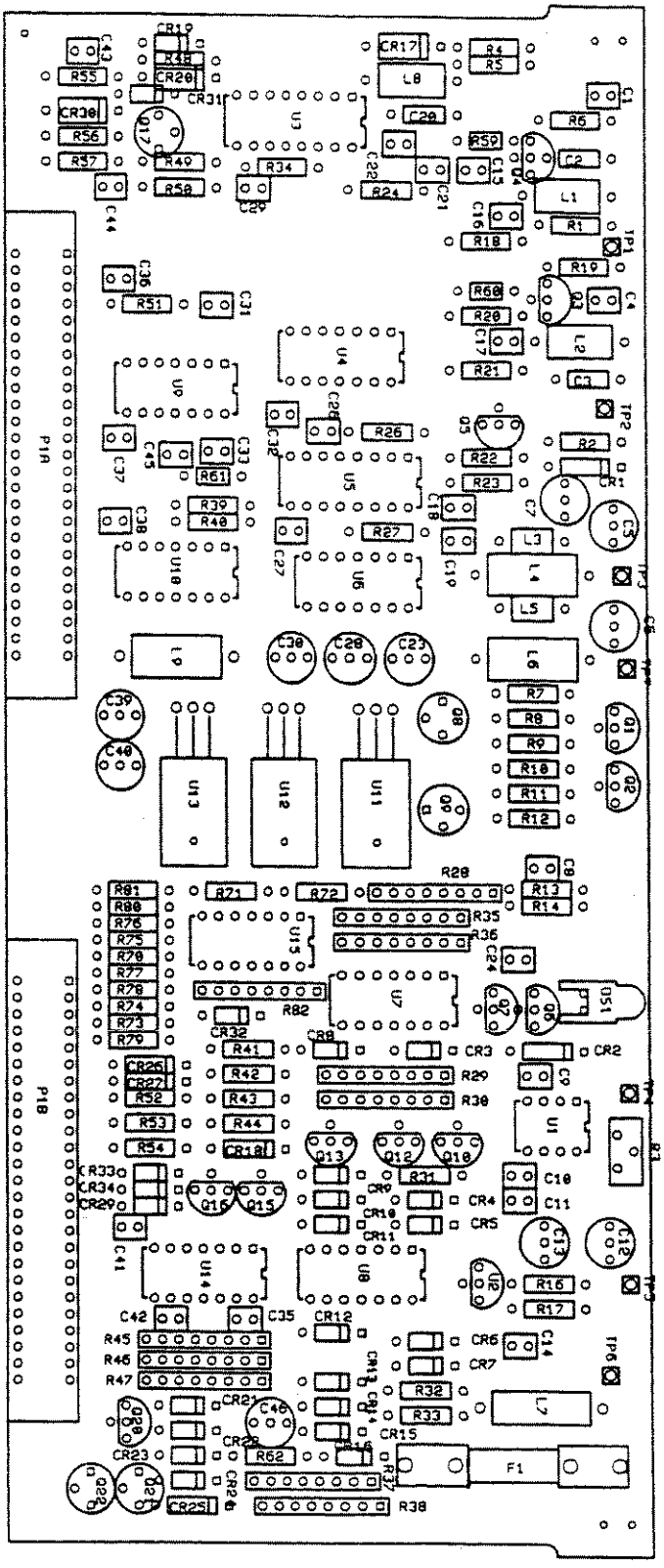
TEST POINT: A1U10A(3)

COUNTER SETUP: EXT. REF. IN. (REAR PANEL)

COUNTER INPUT: 10 MHZ, –5 DBM



P/O Figure 5-18. A1 Waveforms



P/O Figure 5-18. A1 Component Locator

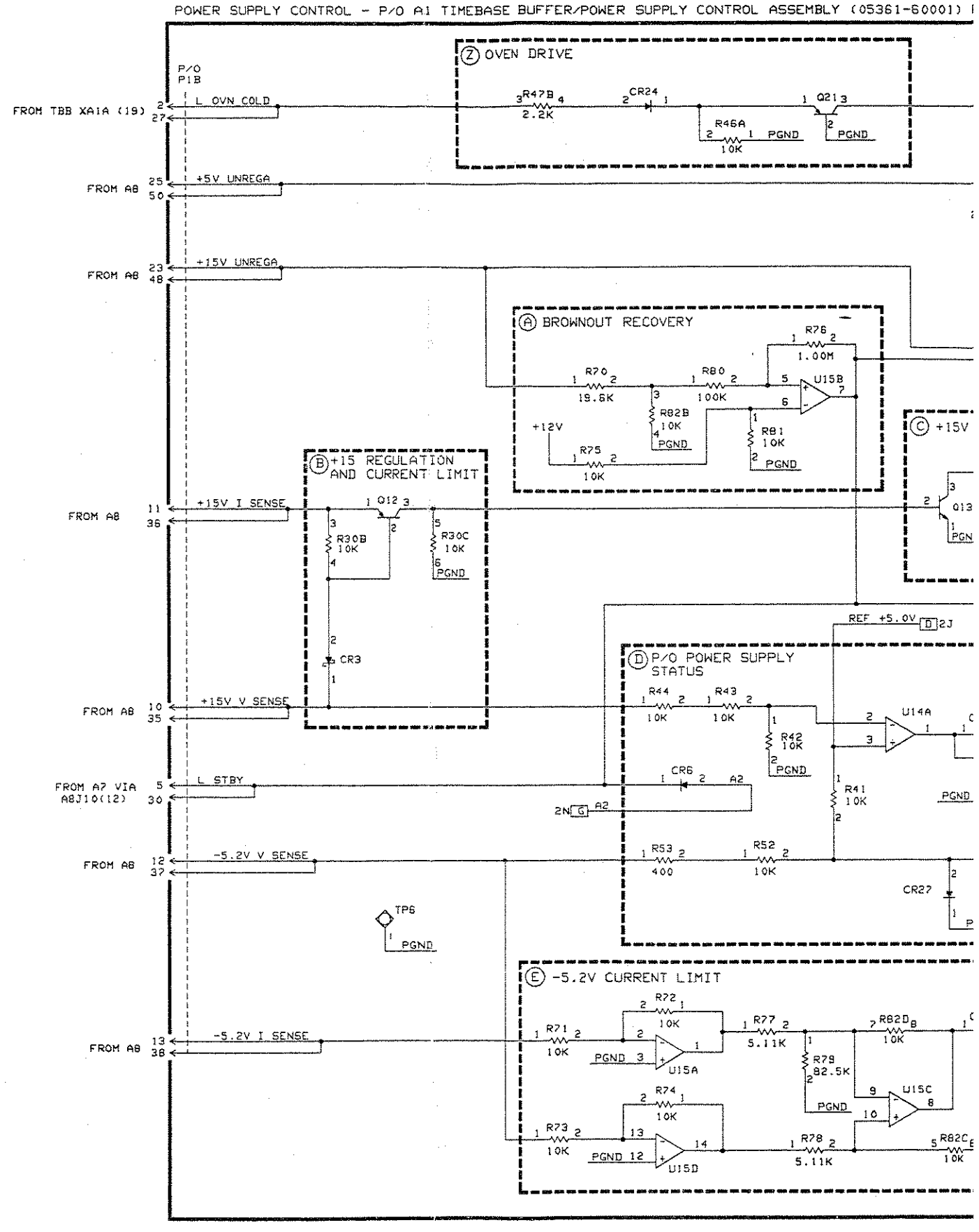
A1 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A1 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN FARADS, INDUCTANCE IN HENRIES.

3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.

4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.



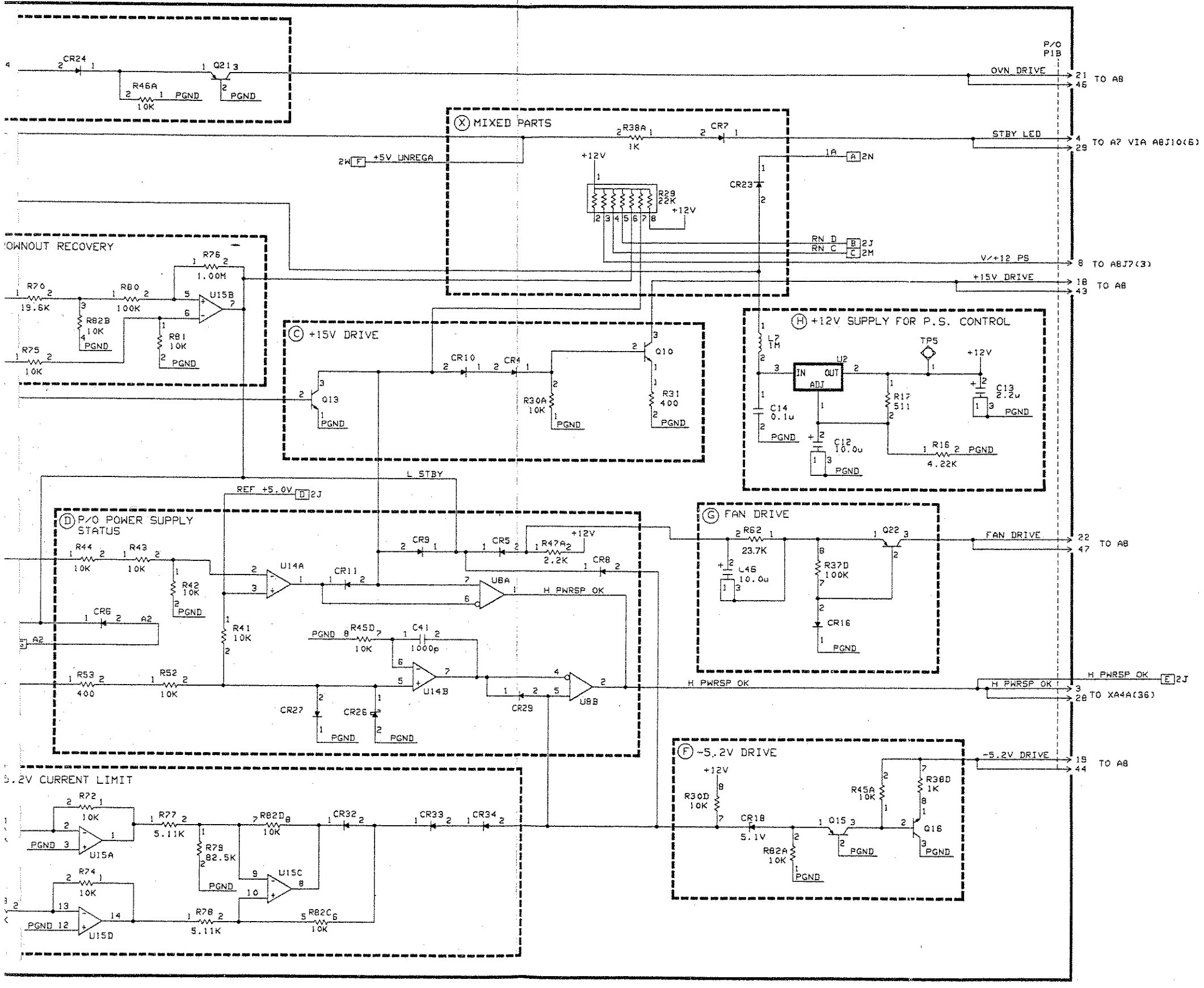
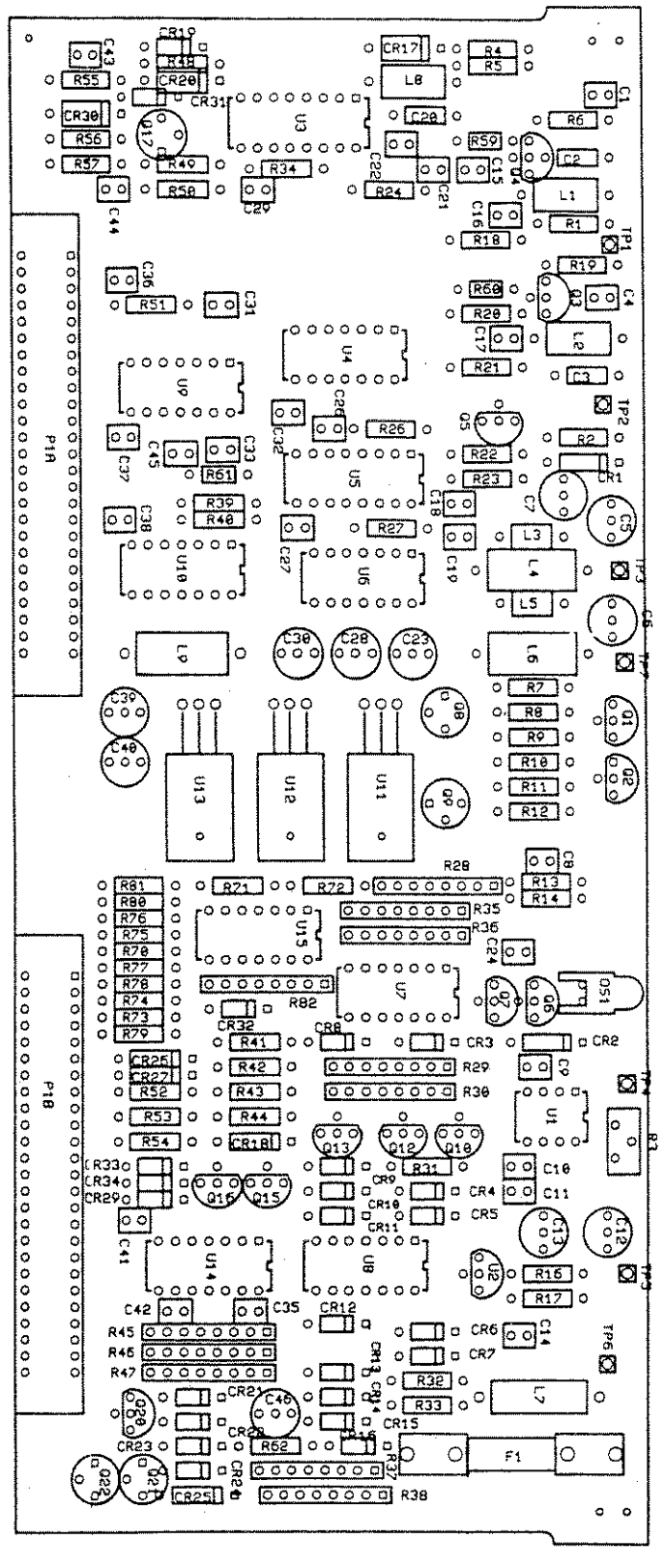


Figure 5-18. A1 Timebase Buffer/Power Supply Control Assembly Schematic Diagram (Sheet 1 of 3)



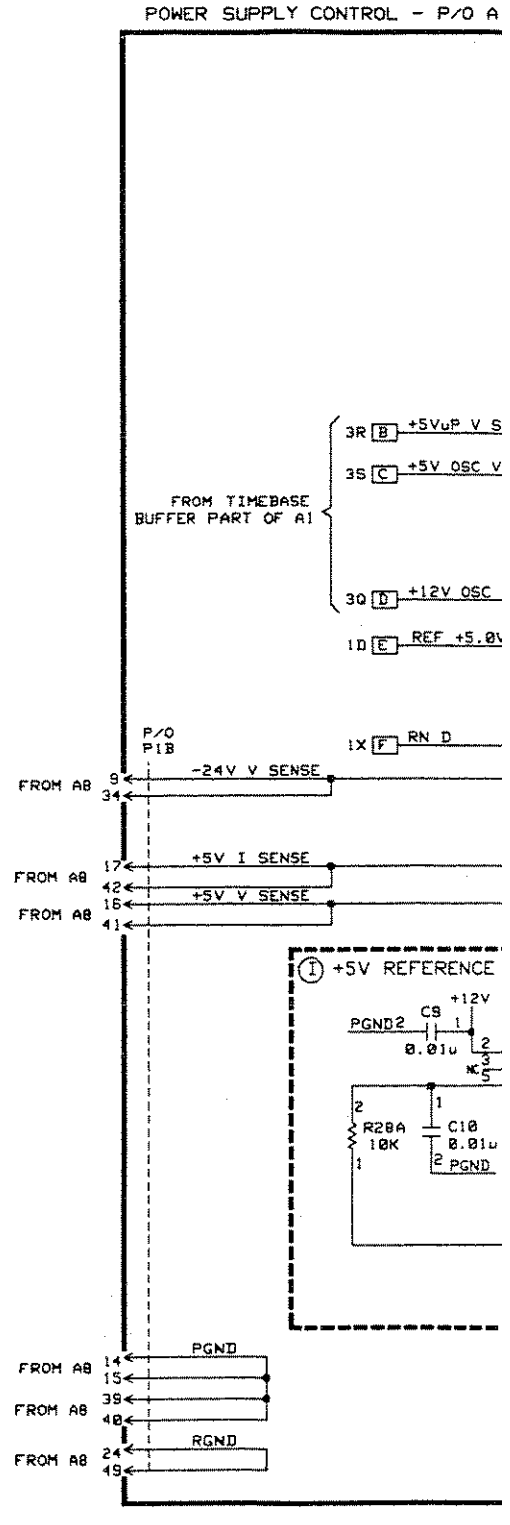
A1 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A1 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN FARADS, INDUCTANCE IN HENRIES.

3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.

4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.



ATIC DIAGRAM NOTES

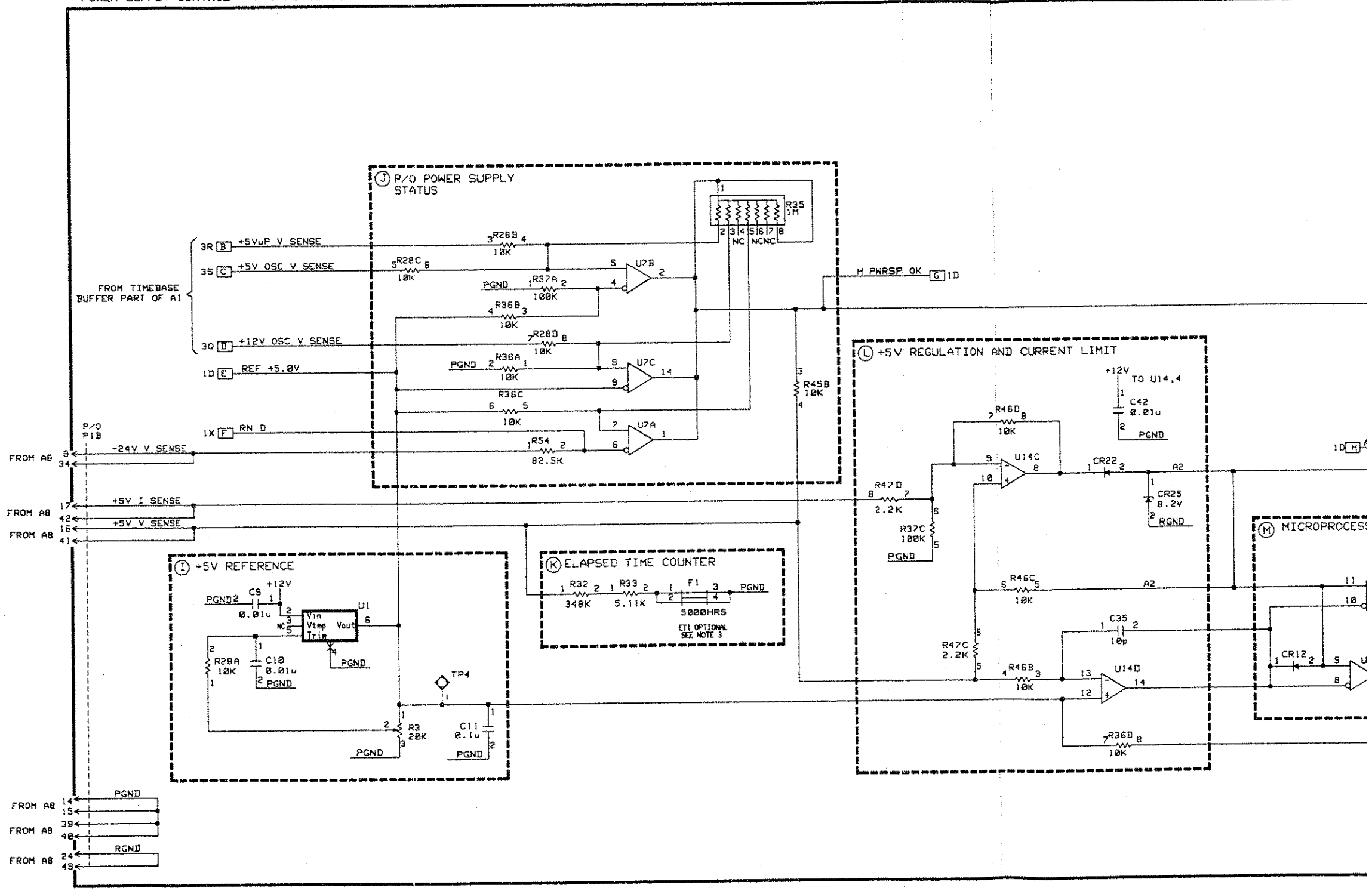
ENCE DESIGNATIONS WITHIN THIS ASSEMBLY ABBREVIATED. ADD A1 ASSEMBLY NUMBER TO REVIATION FOR COMPLETE DESCRIPTION.

S OTHERWISE INDICATED: RESISTANCE IN , CAPACITANCE IN FARADS, INDUCTANCE IN RIES.

ISK (*) INDICATES FACTORY SELECTED COM- NT. AVERAGE VALUE SHOWN.

DE ("~") PRECEDING A SIGNAL INDICATES A NEGA- RUE SIGNAL.

POWER SUPPLY CONTROL - P/O A1 TIMEBASE BUFFER/POWER SUPPLY CONTROL ASSEMBLY (05361-60001) REV. B (SHEET 2 OF 3).



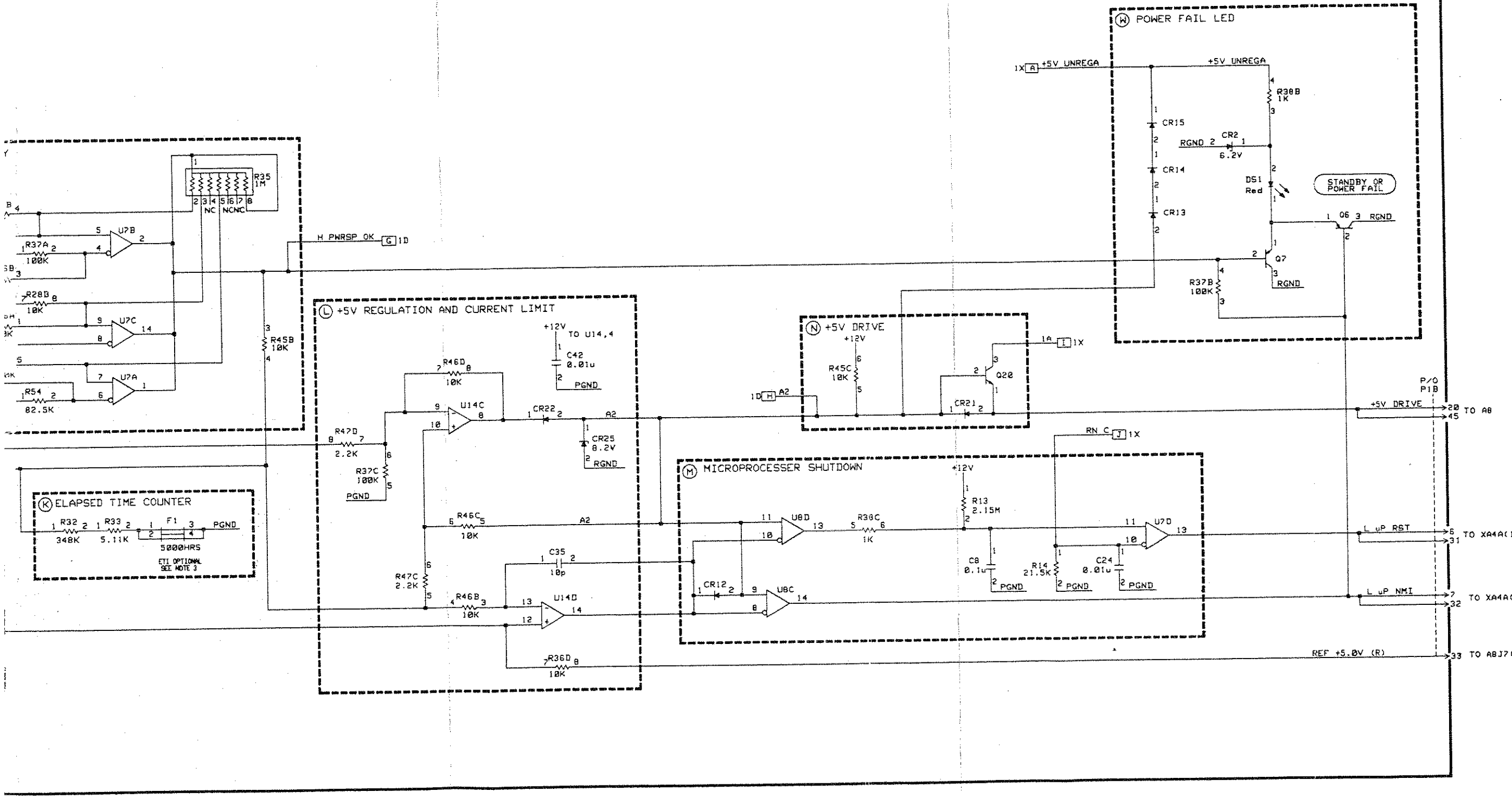


Figure 5-18. A1 Timebase Buffer/Power Supply Control Assembly Component Locator/Schematic Diagram (Sheet 2 of 3)

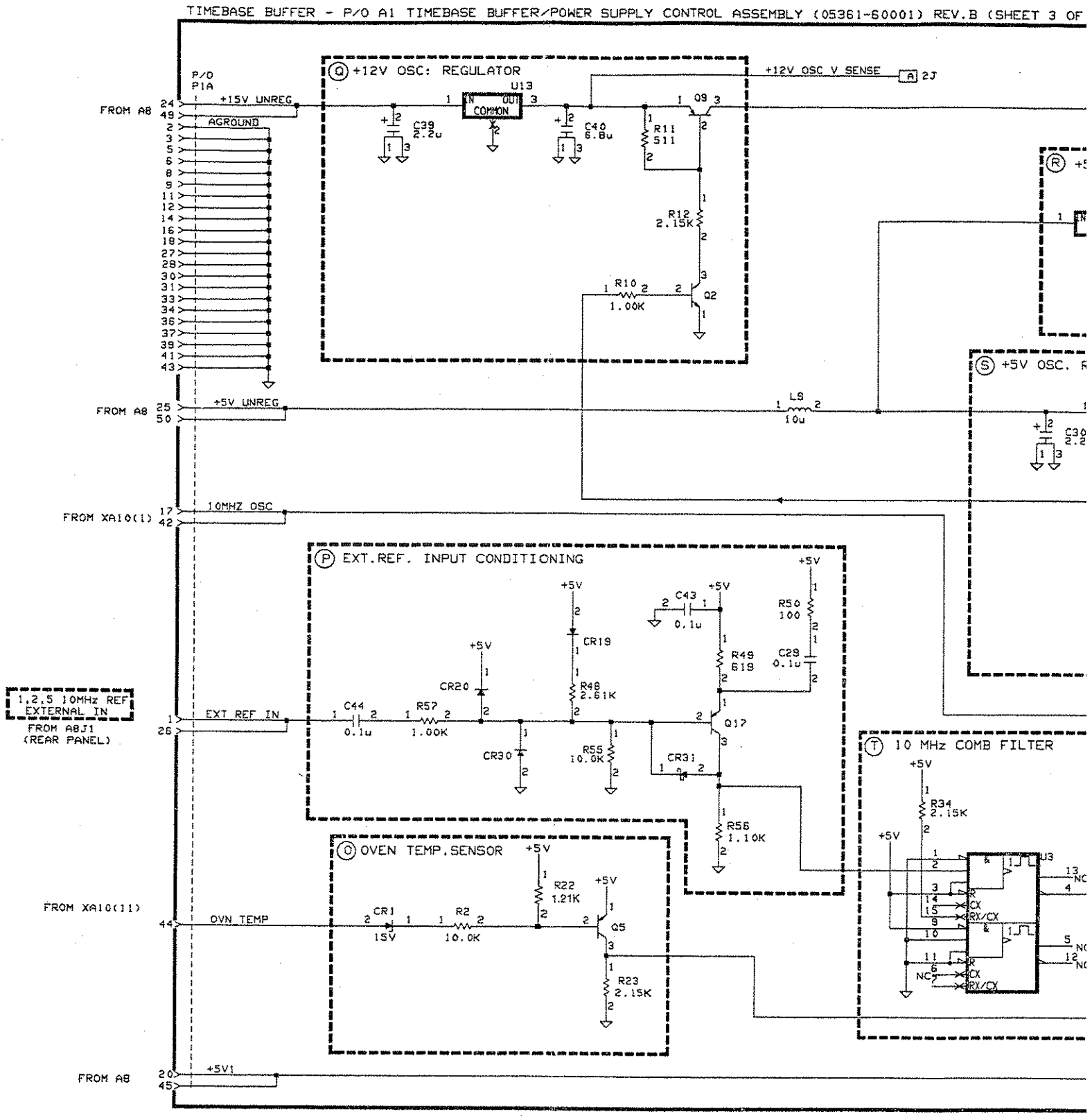
A1 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A1 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN FARADS, INDUCTANCE IN HENRIES.

3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.

4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.



TIMEBASE BUFFER - P/O A1 TIMEBASE BUFFER/POWER SUPPLY CONTROL ASSEMBLY (05361-60001) REV.B (SHEET 3 OF 3)

P/O P1A

+15V UNREG

AGROUND

+5V UNREG

10MHZ OSC

EXT REF IN

OVN TEMP

+5V1

O +12V OSC: REGULATOR

U13 COMMON

C39 2.2u

C40 6.8u

Q9

R11 511

R12 2.15K

R10 1.00K

Q2

+12V OSC V SENSE A 2J

R +5V REGULATOR

U11 COMMON

L5 22u

C23 33.0u

+5VuP V SENSE

L6 8.2u

L3 22u

C7 1.0u

C6 33.0u

+5V D1

+5V D2

+5VuP V SENSE B 2J

S +5V OSC. REGULATER

U12 COMMON

C30 2.2u

C28 33.0u

L9 10u

+5V OSC V SENSE

L4 8.2u

C5 33.0u

+5V

Q8

R8 511

R9 2.15K

L EXT REF

R7 1.00K

Q1

+5V OSC V SENSE C 2J

P EXT.REF. INPUT CONDITIONING

C43 0.1u

R50 100

C29 0.1u

CR19

R49 619

CR20

R48 2.61K

C44 0.1u

R57 1.00K

CR30

R55 10.0K

CR31

Q17

R56 1.10K

O OVEN TEMP.SENSOR

CR1 15V

R2 10.0K

R22 1.21K

Q5

R23 2.15K

T 10 MHz COMB FILTER

R34 2.15K

U3

NC

CX

RX/CX

R24 5.11K

L8 1.0u

C20 240p

C21 22p

C22 0.1u

C15 10p

CR17

R4 23.7K

R5 21.5K

R59 100

C1 0.1u

L1 1.0u

C2 240p

C16 10p

R1 23.7K

R18 21.5K

C4 0.1u

L2 1.0u

C3 240p

C17 10p

R60 100

Q3

Q4

R6 215

R19 215

10MHZ

TP1

V TIMEBASE DETE

H EXT REF

TP7

C27 100

Y SINEWAVE TO TTL/ TIMEBASE MUX

R40 5.11K

C38 0.01u

R39 1.47K

R21 10.0K

R20 1.21K

U4A

U4B

U10B

U10D

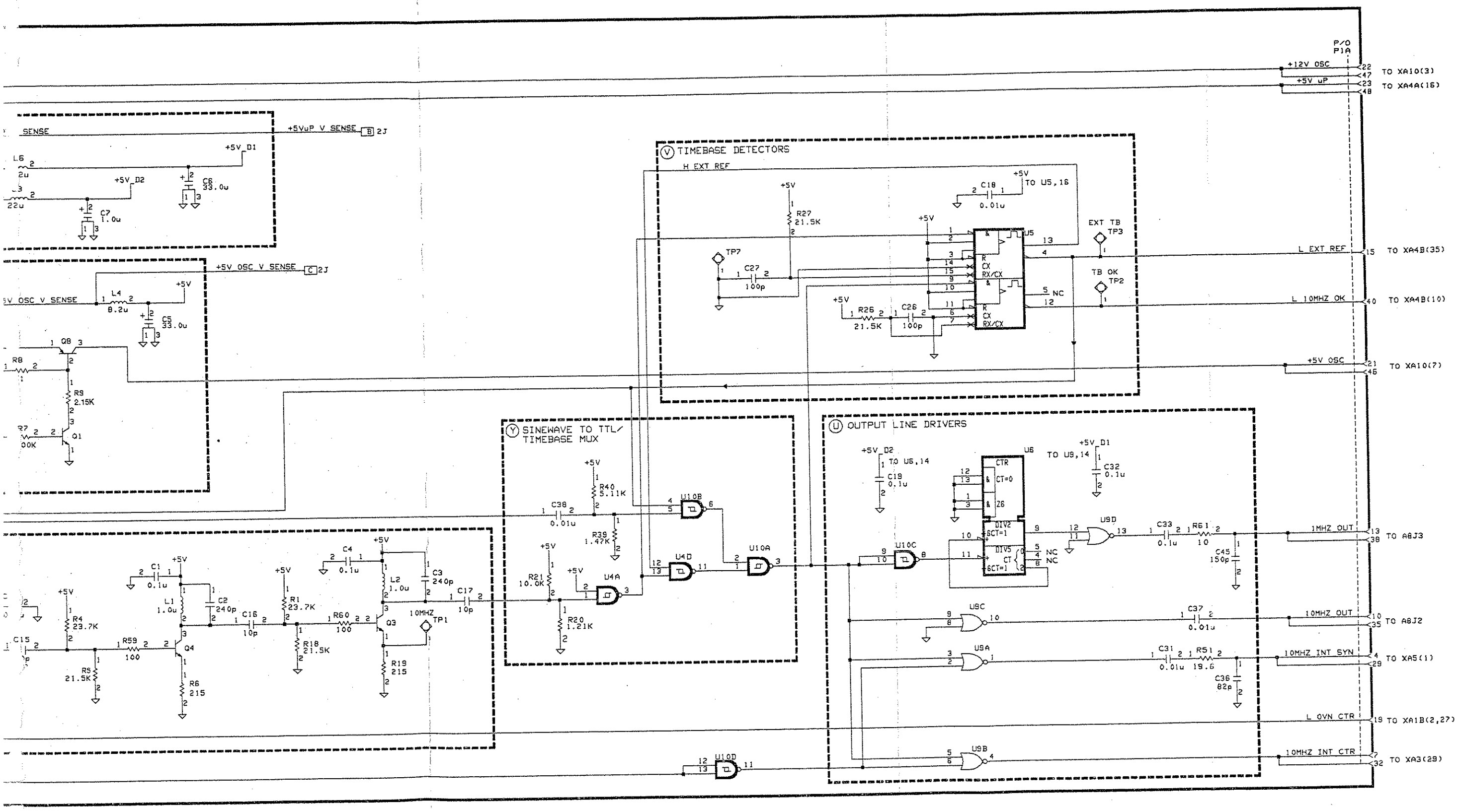


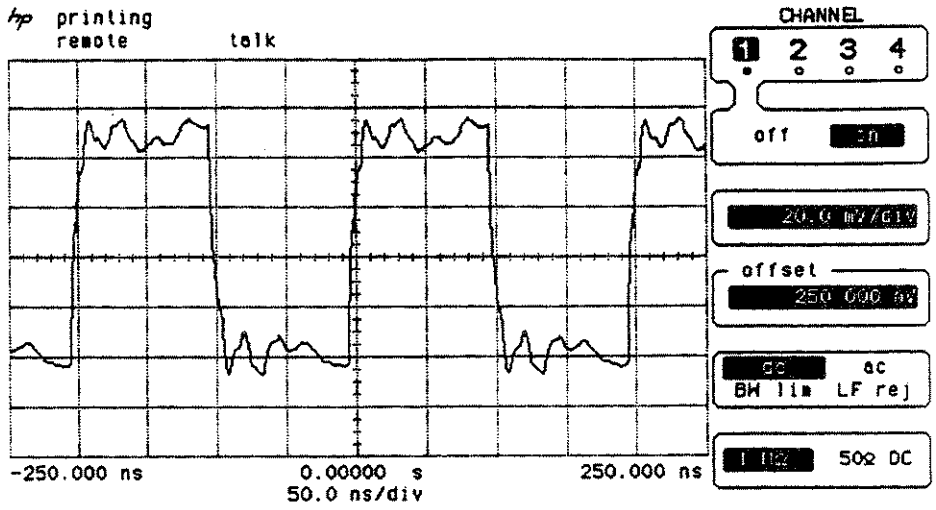
Figure 5-18. A1 Timebase Buffer/Power Supply Control Assembly Schematic Diagram (Sheet 3 of 3)

WAVEFORM A

TEST POINT: A2PI(3), LF OUT A

COUNTER SETUP: INPUT 2, 50Ω FREQUENCY MODE

COUNTER INPUT: 50 MHZ, –10 DBM

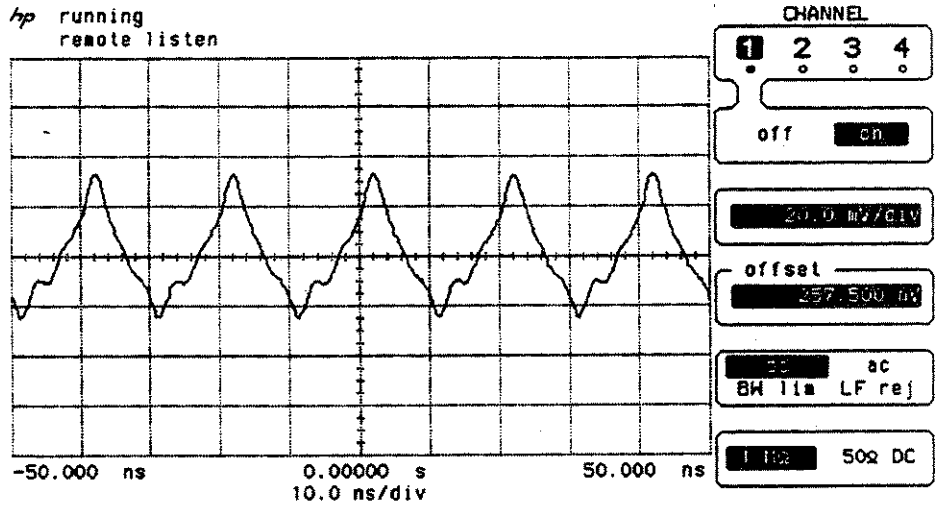


WAVEFORM B

TEST POINT: A2PI(3), LF OUT A

COUNTER SETUP: INPUT 2, 1MΩ FREQUENCY MODE

COUNTER INPUT: 50 MHZ, –10 DBM

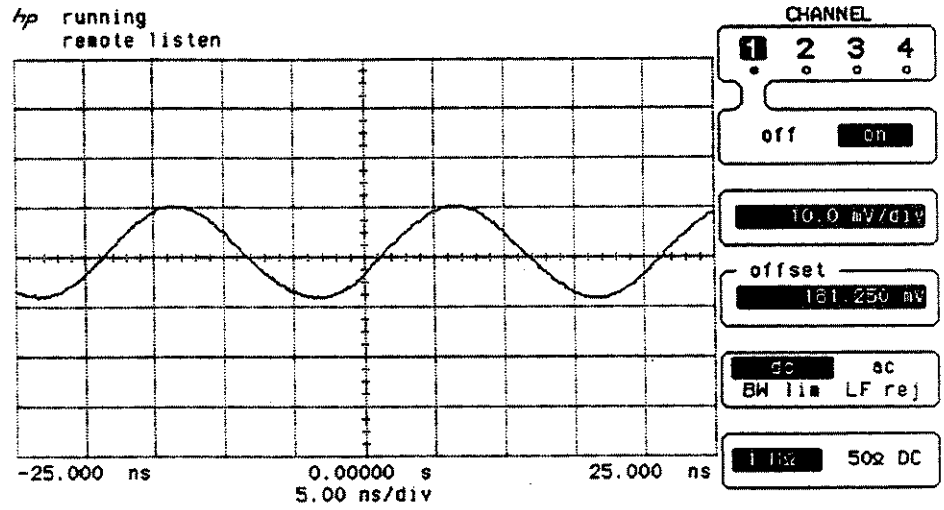


WAVEFORM C

TEST POINT: A2U7(2)

COUNTER SETUP: INPUT 2, 50Ω FREQUENCY MODE

COUNTER INPUT: 50 MHZ, 100 MV P-P



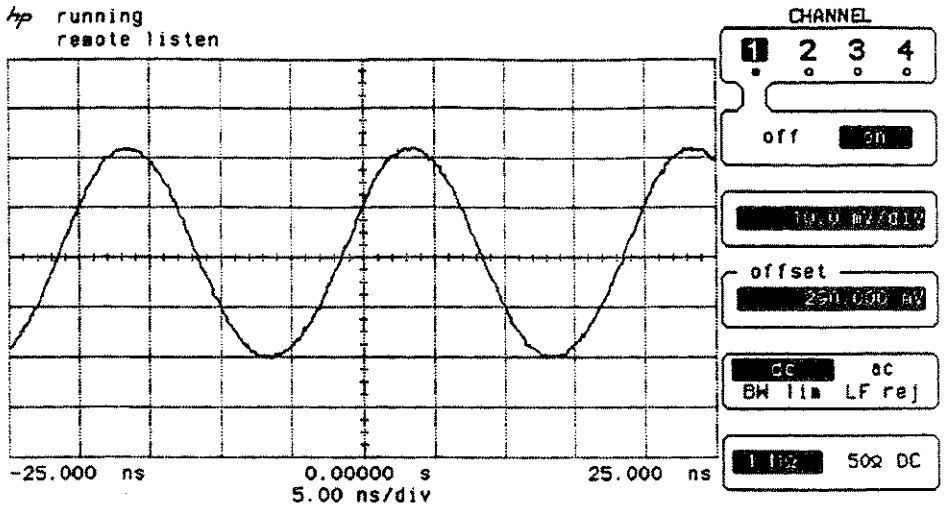
P/O Figure 5-19. A2 Waveforms

WAVEFORM D

TEST POINT: A2U5(2),

COUNTER SETUP: INPUT 2, 50Ω FREQUENCY MODE

COUNTER INPUT: 50 MHZ, 100 MV P-P

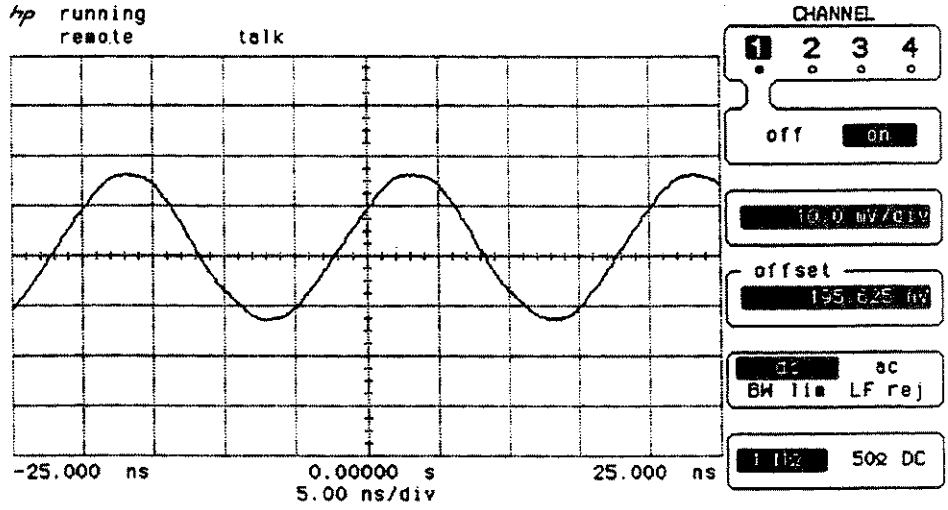


WAVEFORM E

TEST POINT: SOURCE OF A2Q9

COUNTER SETUP: INPUT 2, 1MΩ FREQUENCY MODE

COUNTER INPUT: 50 MHZ, 100 MV P-P

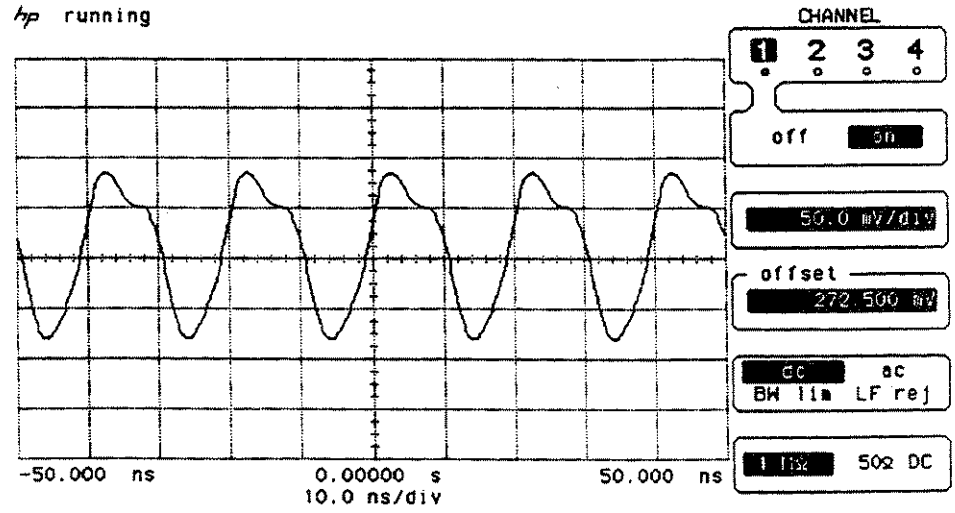


WAVEFORM F

TEST POINT: A2U4(2)

COUNTER SETUP: INPUT 2, 50Ω FREQUENCY MODE

COUNTER INPUT: 50 MHZ, 100 MV P-P



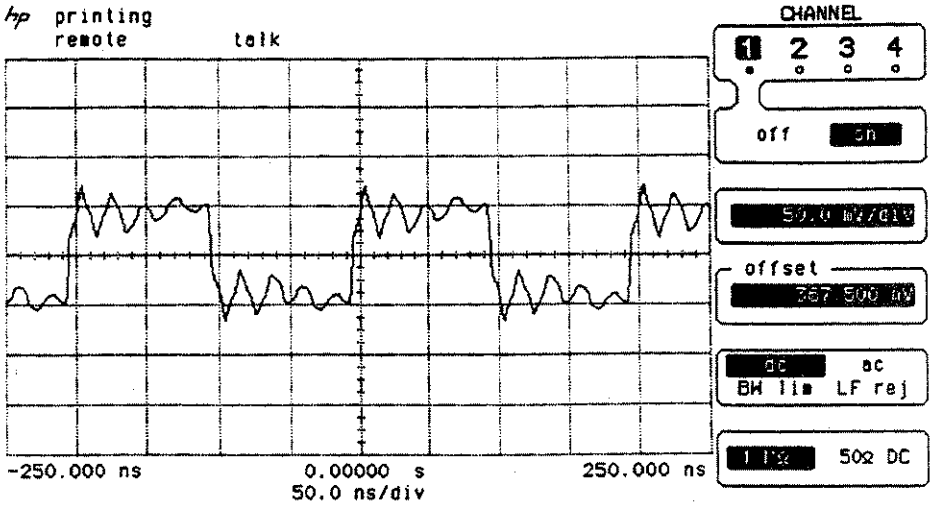
P/O Figure 5-19. A2 Waveforms

WAVEFORM G

TEST POINT: A2U1(8)

COUNTER SETUP: INPUT 2, 50Ω FREQUENCY MODE

COUNTER INPUT: 50 MHZ, −10 DBM

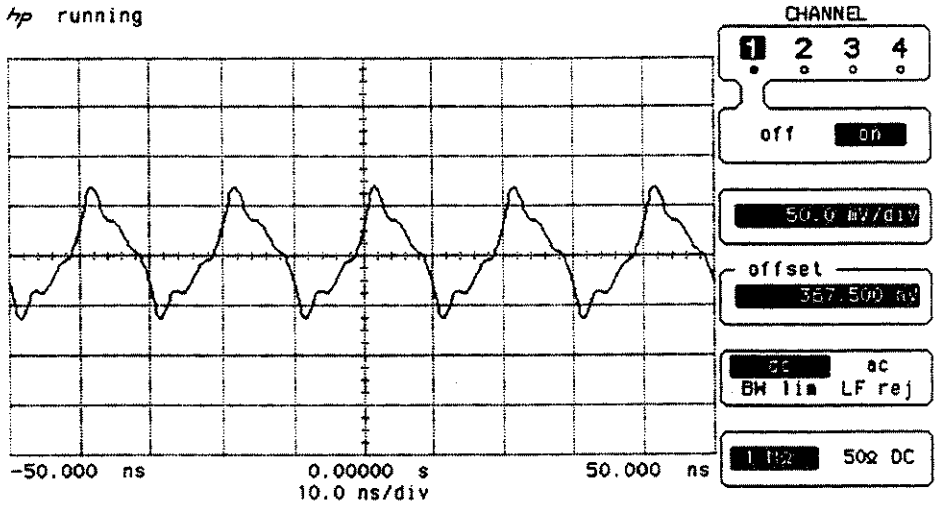


WAVEFORM H

TEST POINT: A2U6(7)

COUNTER SETUP: INPUT 2, 1MΩ FREQUENCY MODE

COUNTER INPUT: 50 MHZ, 100 MV P-P AT A2U6(10)

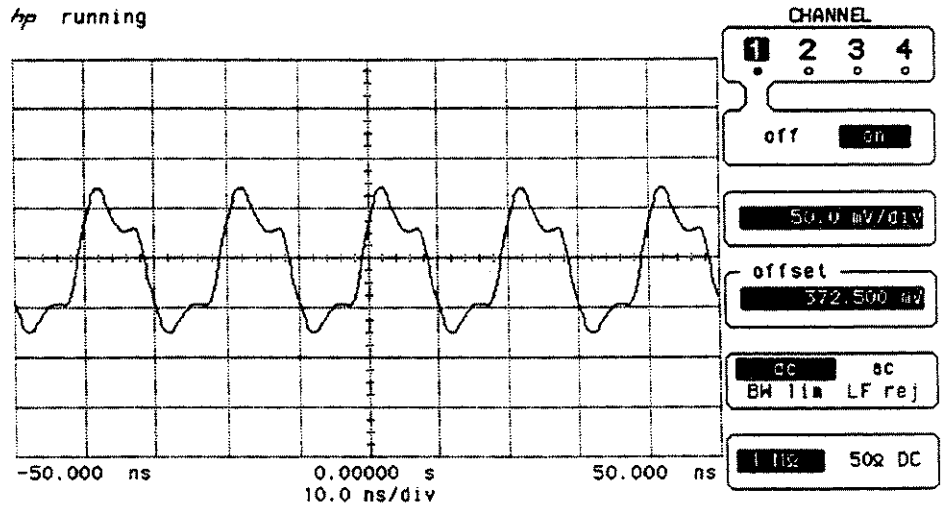


WAVEFORM I

TEST POINT: A2U6(2)

COUNTER SETUP: INPUT 2, 1MΩ FREQUENCY MODE

COUNTER INPUT: 50 MHZ, 100 MV P-P AT A2U6(5)



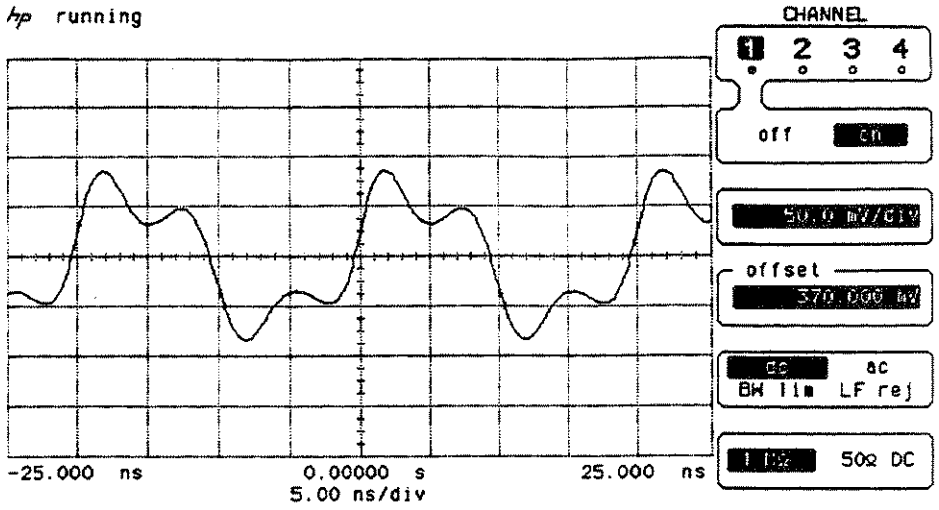
P/O Figure 5-19. A2 Waveforms

WAVEFORM J

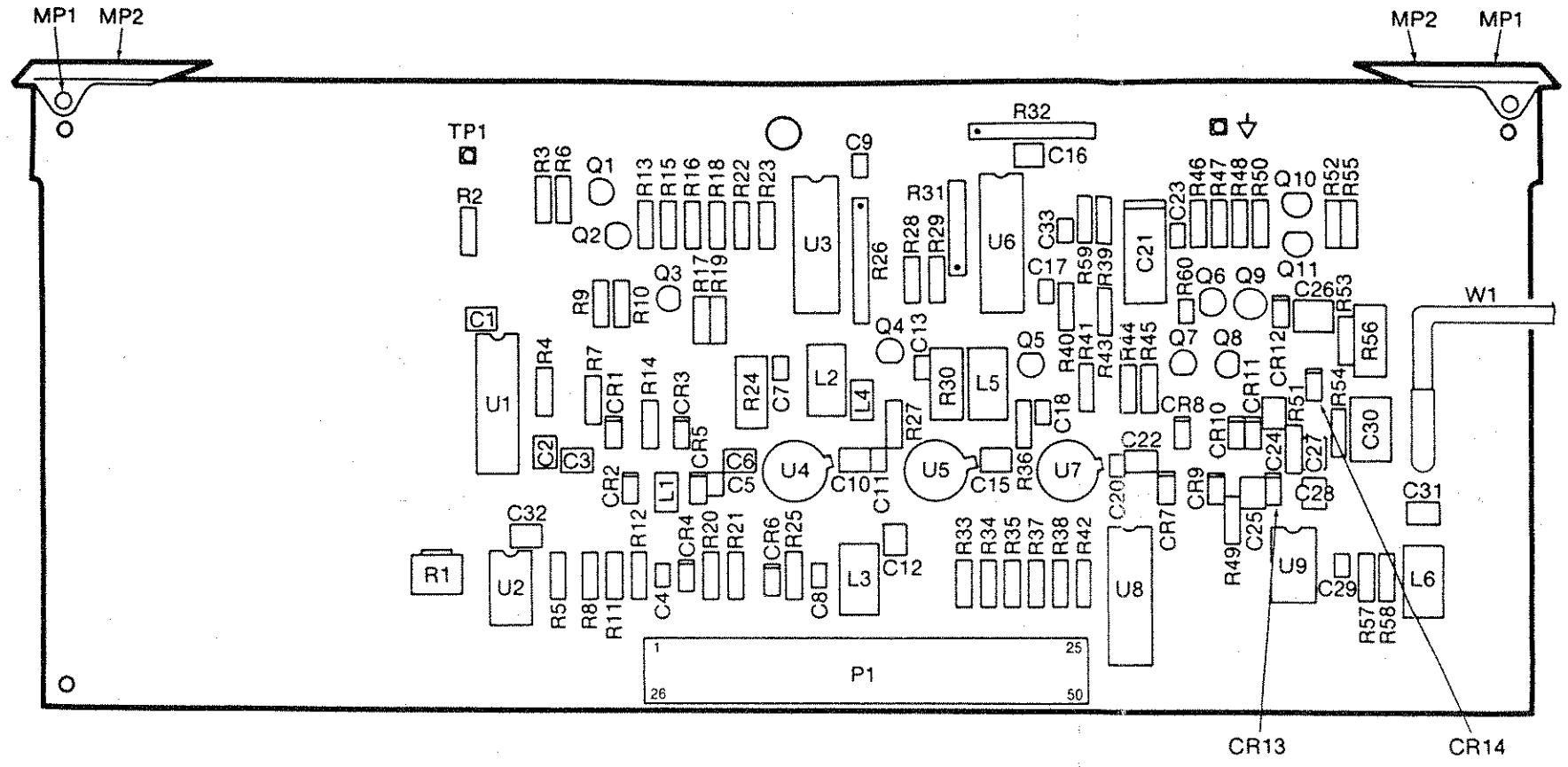
TEST POINT: A2U6(15)

COUNTER SETUP: INPUT 2, 1MΩ FREQUENCY MODE

COUNTER INPUT: 50 MHZ, 100 MV P-P AT A2U6(5)



P/O Figure 5-19. A2 Waveforms



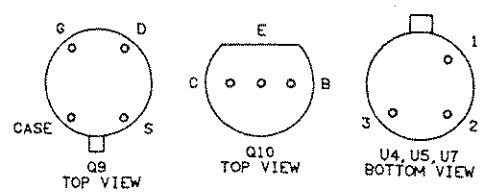
A2 SCHEMATIC DIAGRAM NOTES

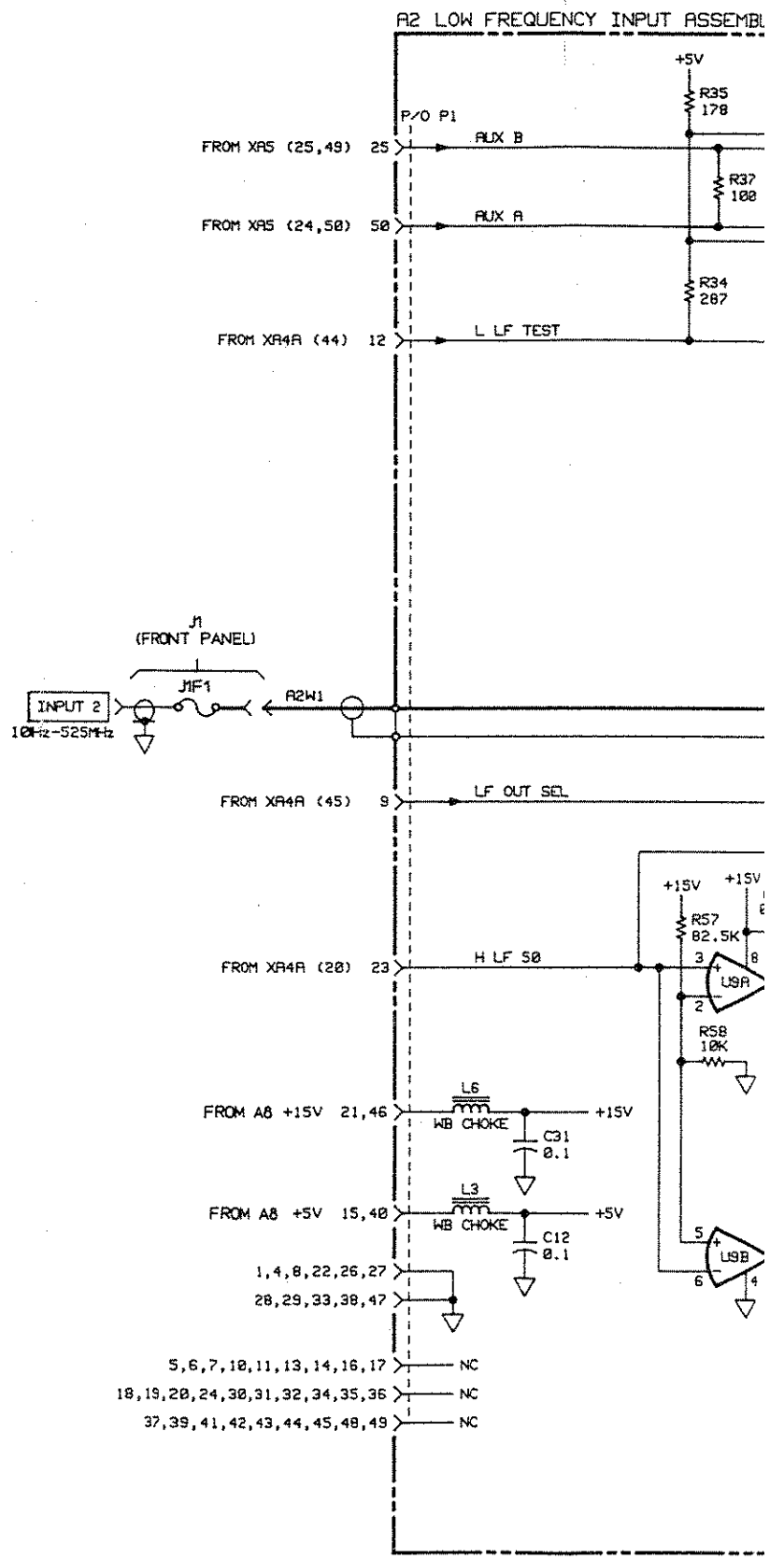
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A2 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

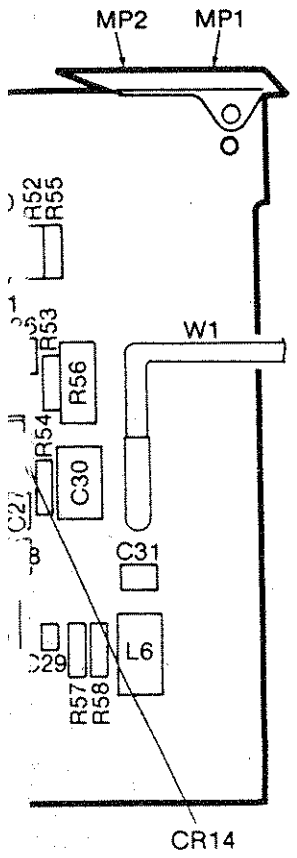
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN MICROFARADS, INDUCTANCE IN MICROHENRIES.

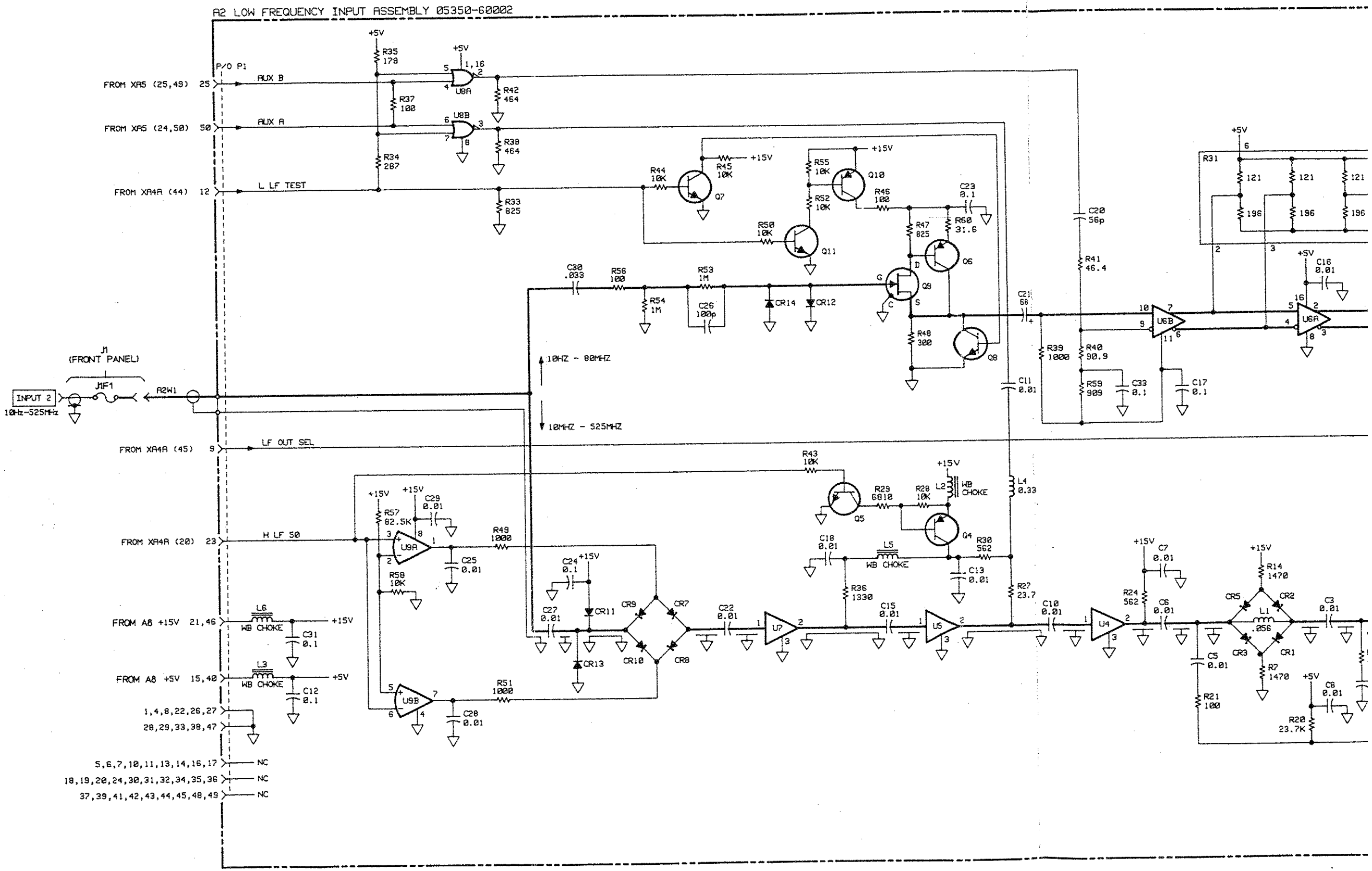
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.

4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.






MP2
MP1
R52
R55
R53
W1
R56
R54
C30
C31
L6
R57
R58
CR14


A2 LOW FREQUENCY INPUT ASSEMBLY 05350-60002
FROM XA5 (25,49) 25
AUX B
FROM XA5 (24,50) 50
AUX A
FROM XA4A (44) 12
L LF TEST
P/O P1
+5V
R35 178
R37 100
R34 287
R33 825
R42 464
R38 464
U8A
U8B
1,16
J1
(FRONT PANEL)
J1F1
INPUT 2
10Hz-525MHz
A2W1
10HZ - 80MHZ
10MHZ - 525MHZ
FROM XA4A (45) 9
LF OUT SEL
FROM XA4A (20) 23
H LF 50
FROM A8 +15V 21,46
FROM A8 +5V 15,40
1,4,8,22,26,27
28,29,33,38,47
5,6,7,10,11,13,14,16,17
18,19,20,24,30,31,32,34,35,36
37,39,41,42,43,44,45,48,49
NC
+15V
R44 10K
R45 10K
Q7
R55 10K
R52 10K
Q10
R46 100
R50 10K
Q11
R47 825
R60 31.6
C23 0.1
Q6
Q9
Q8
R48 300
C30 .033
R56 100
R53 1M
R54 1M
C26 100p
CR14
CR12
C20 56p
R41 46.4
C21 68
R39 1000
R40 90.9
C11 0.01
R59 909
C33 0.1
C17 0.1
U6B
U6A
R31
121
196
C16 0.01
R43 10K
Q5
R29 6810
R28 10K
L2 WB CHOKE
Q4
L4 0.33
R30 562
C18 0.01
L5 WB CHOKE
C13 0.01
R36 1330
R27 23.7
C29 0.01
R57 82.5K
U9A
C25 0.01
R49 1000
R58 10K
C24 0.1
C27 0.01
CR11
CR13
CR9
CR7
CR10
CR8
C22 0.01
U7
C15 0.01
U5
C10 0.01
U4
C7 0.01
R24 562
C6 0.01
R14 1470
CR5
CR2
L1 .056
CR3
CR1
C3 0.01
C5 0.01
R7 1470
R21 100
C8 0.01
R20 23.7K
L6 WB CHOKE
C31 0.1
L3 WB CHOKE
C12 0.1
U9B
R51 1000
C28 0.01

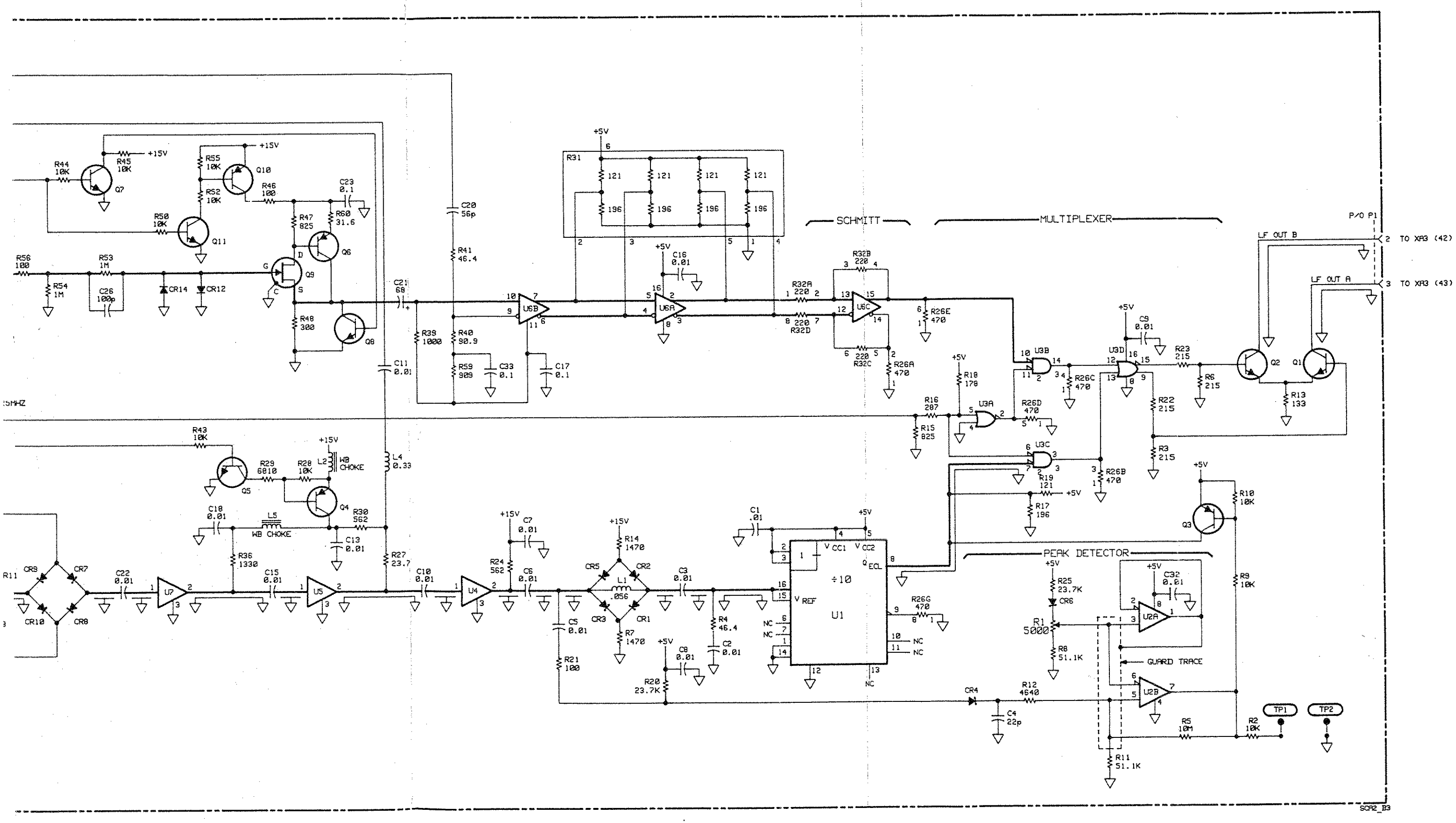


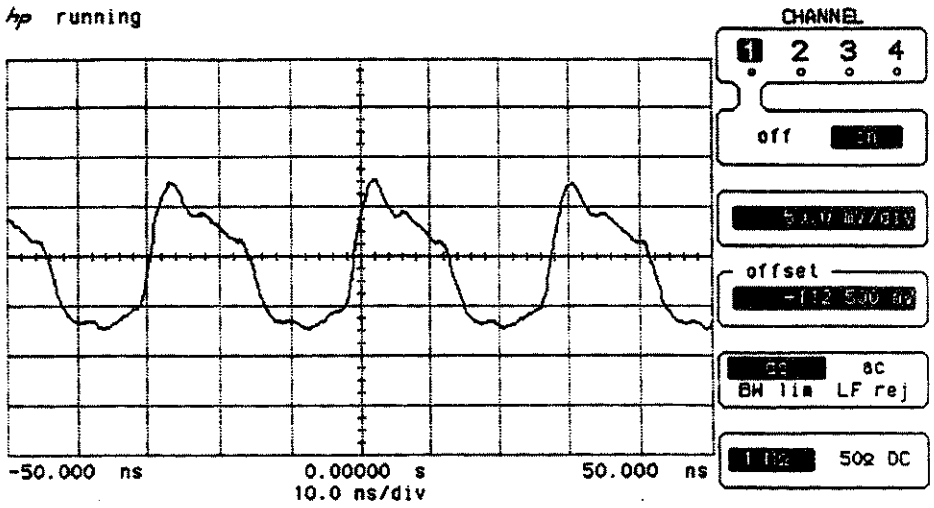
Figure 5-19. A2 Low Frequency Input Assembly Component Locator/Schematic Diagram

WAVEFORM A

TEST POINT: A3U12(7)

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 1 GHZ

COUNTER INPUT: 1 GHZ, –20 DBM

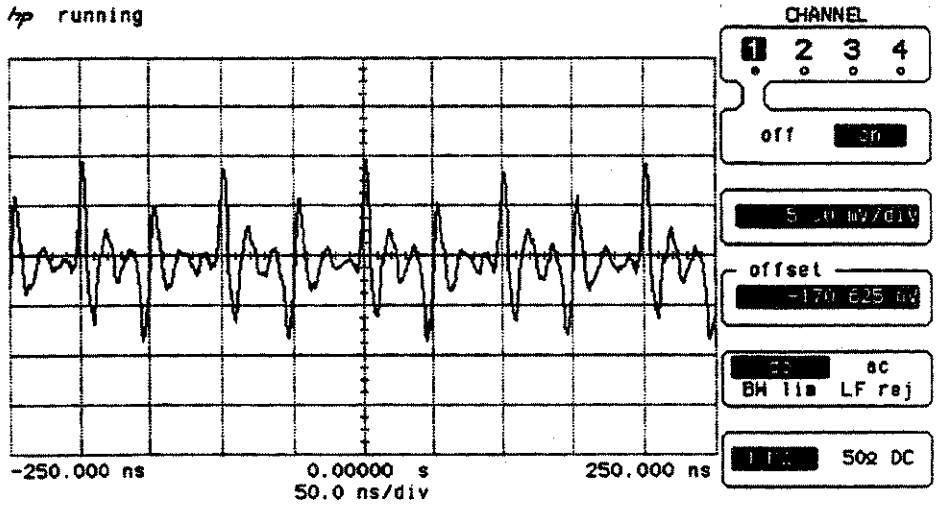


WAVEFORM B

TEST POINT: A3U12(10)

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 1 GHZ

COUNTER INPUT: 1 GHZ, –20 DBM

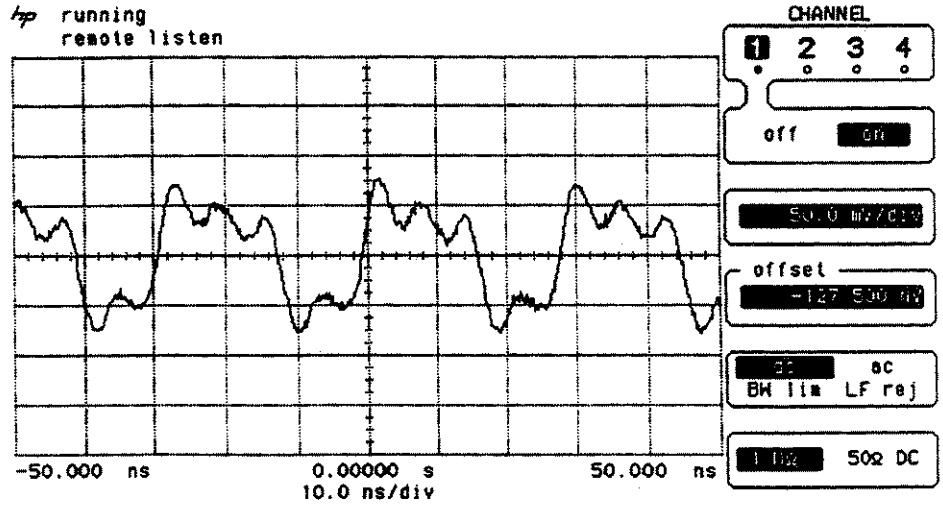


WAVEFORM C

TEST POINT: A3U12(2)

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 1 GHZ

COUNTER INPUT: 1 GHZ, –20 DBM



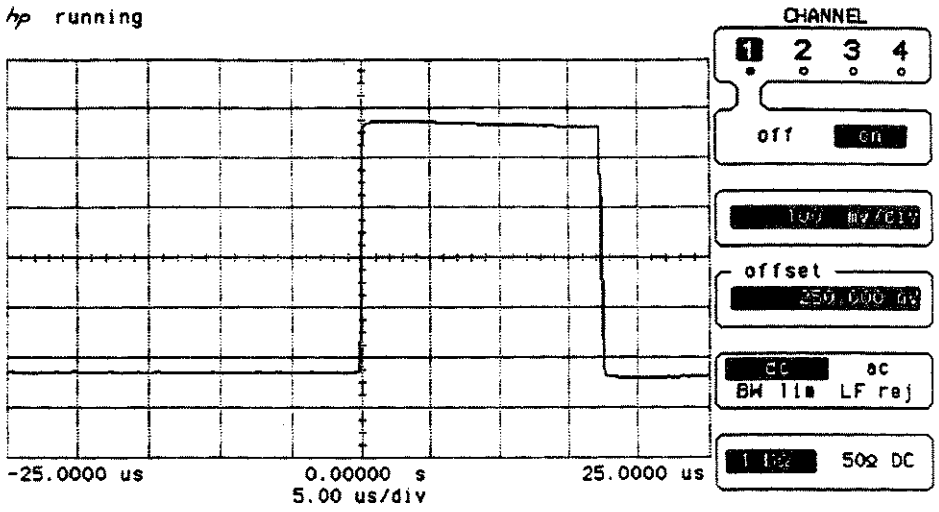
P/O Figure 5-20. A3 Waveforms

WAVEFORM D

TEST POINT: A3U10(7)

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 1 GHZ

COUNTER INPUT: 1 GHZ, −20 DBM

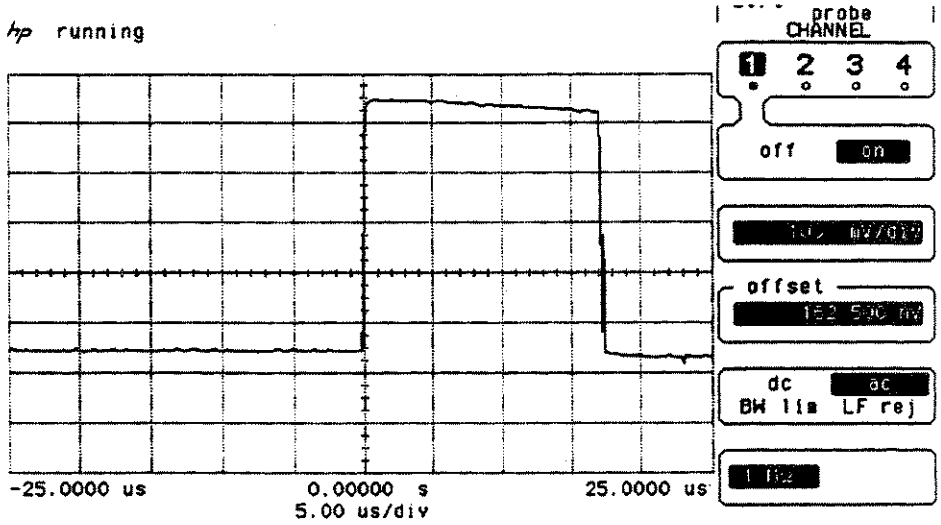


WAVEFORM E

TEST POINT: A3U3(7)

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 1 GHZ

COUNTER INPUT: 1 GHZ, −20 DBM

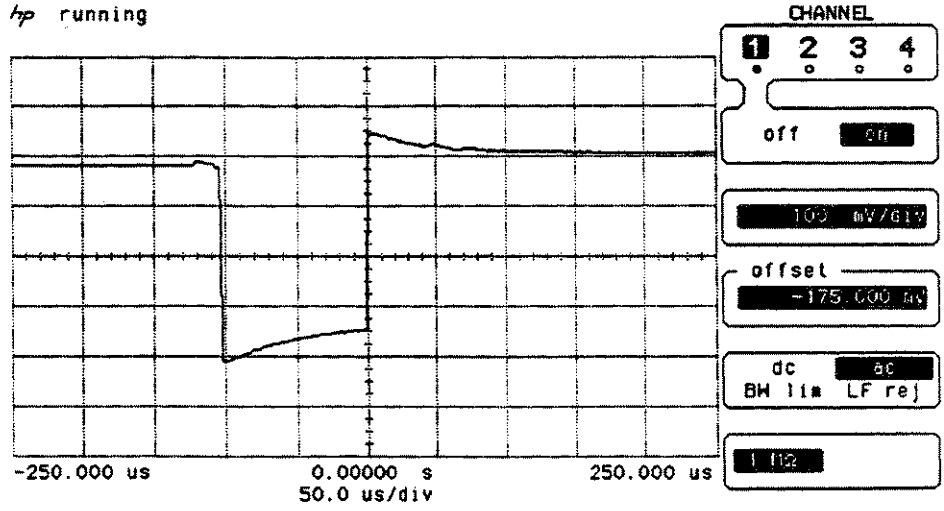


WAVEFORM F

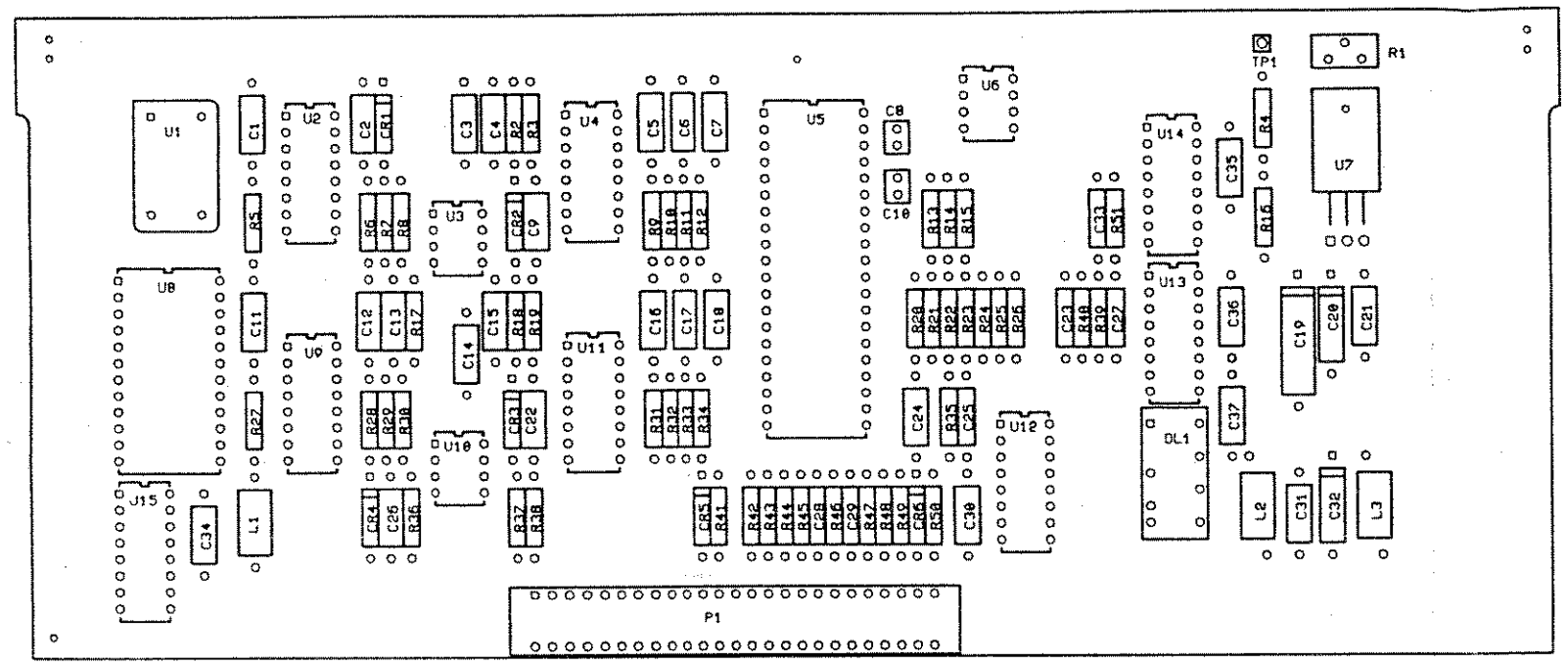
TEST POINT: A3U8(17)

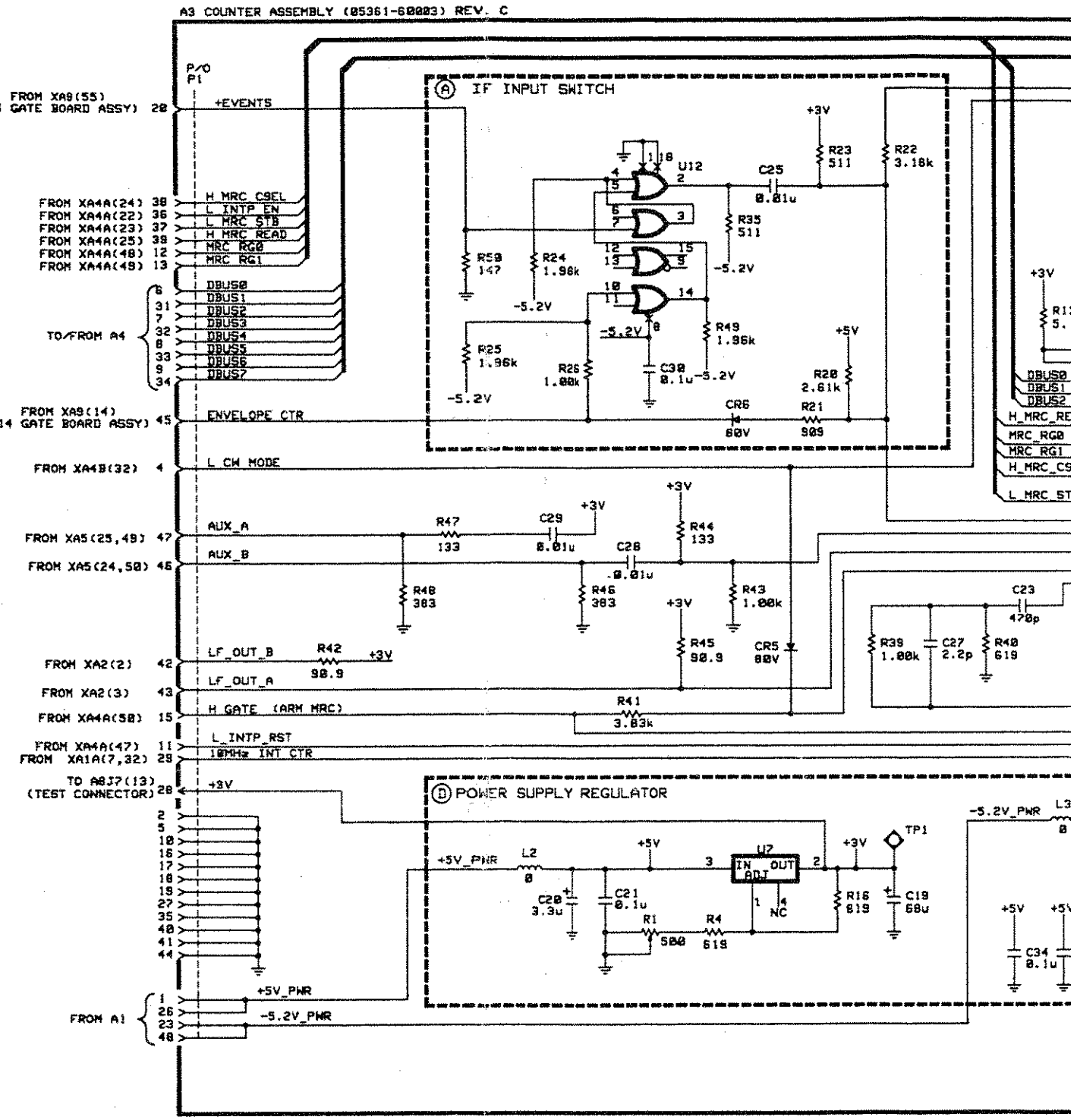
COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 1 GHZ

COUNTER INPUT: 1 GHZ, −20 DBM



P/O Figure 5-20. A3 Waveforms





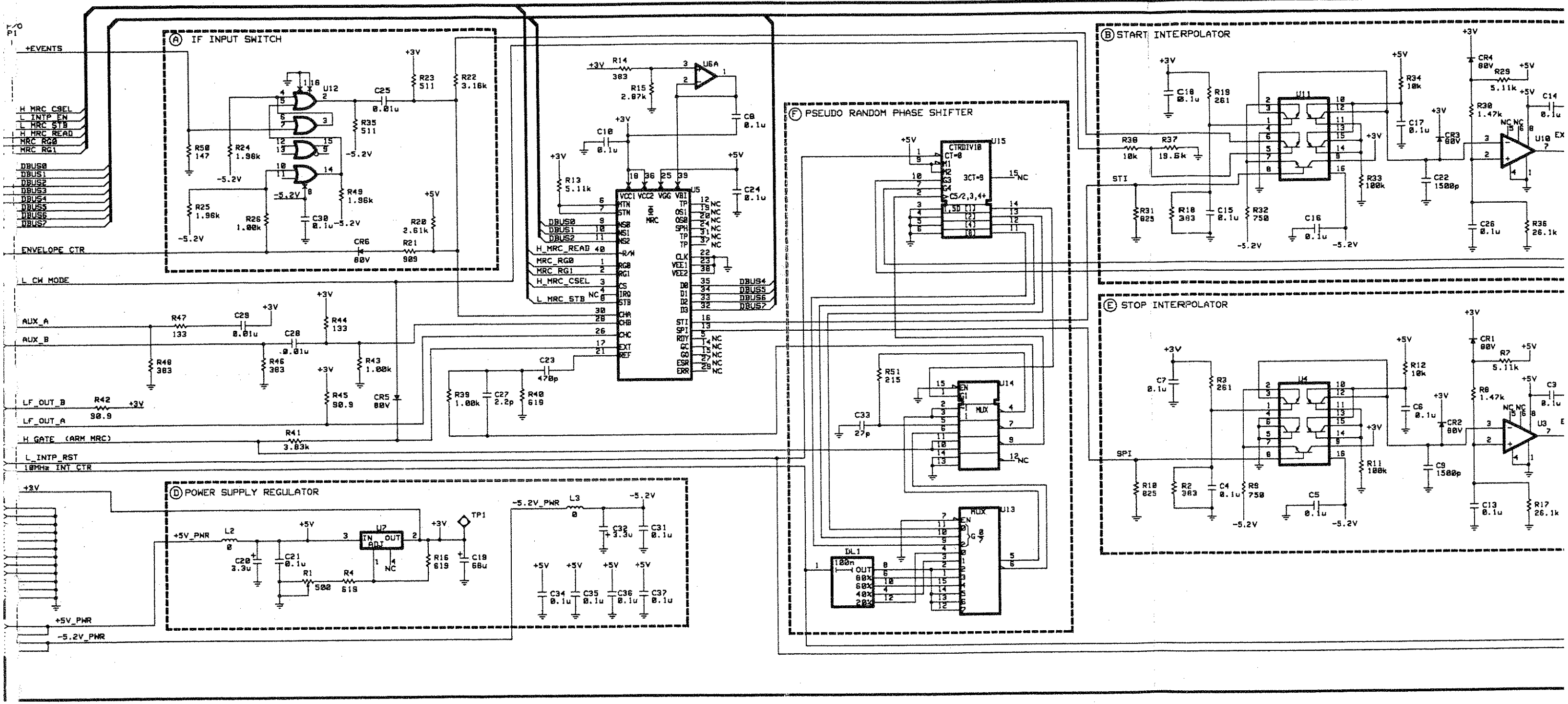
A3 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A3 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN MICROFARADS, INDUCTANCE IN MICROHENRIES.

3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.

4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.


A IF INPUT SWITCH
B START INTERPOLATOR
C STOP INTERPOLATOR
D POWER SUPPLY REGULATOR
E STOP INTERPOLATOR
F PSEUDO RANDOM PHASE SHIFTER
+EVENTS
H_MRC_CSEL
L_INTP_EN
L_MRC_STB
H_MRC_READ
MRC_RG0
MRC_RG1
DBUS0
DBUS1
DBUS2
DBUS3
DBUS4
DBUS5
DBUS6
DBUS7
ENVELOPE_CTR
L_CW_MODE
AUX_A
AUX_B
LF_OUT_B
LF_OUT_A
H_GATE (ARM_MRC)
L_INTP_RST
10MHz INT CTR
+5V_PWR
-5.2V_PWR
STI
SPI
U12
U6A
U5
U15
U14
U13
U11
U4
U2
U10
U3
DL1
TP1

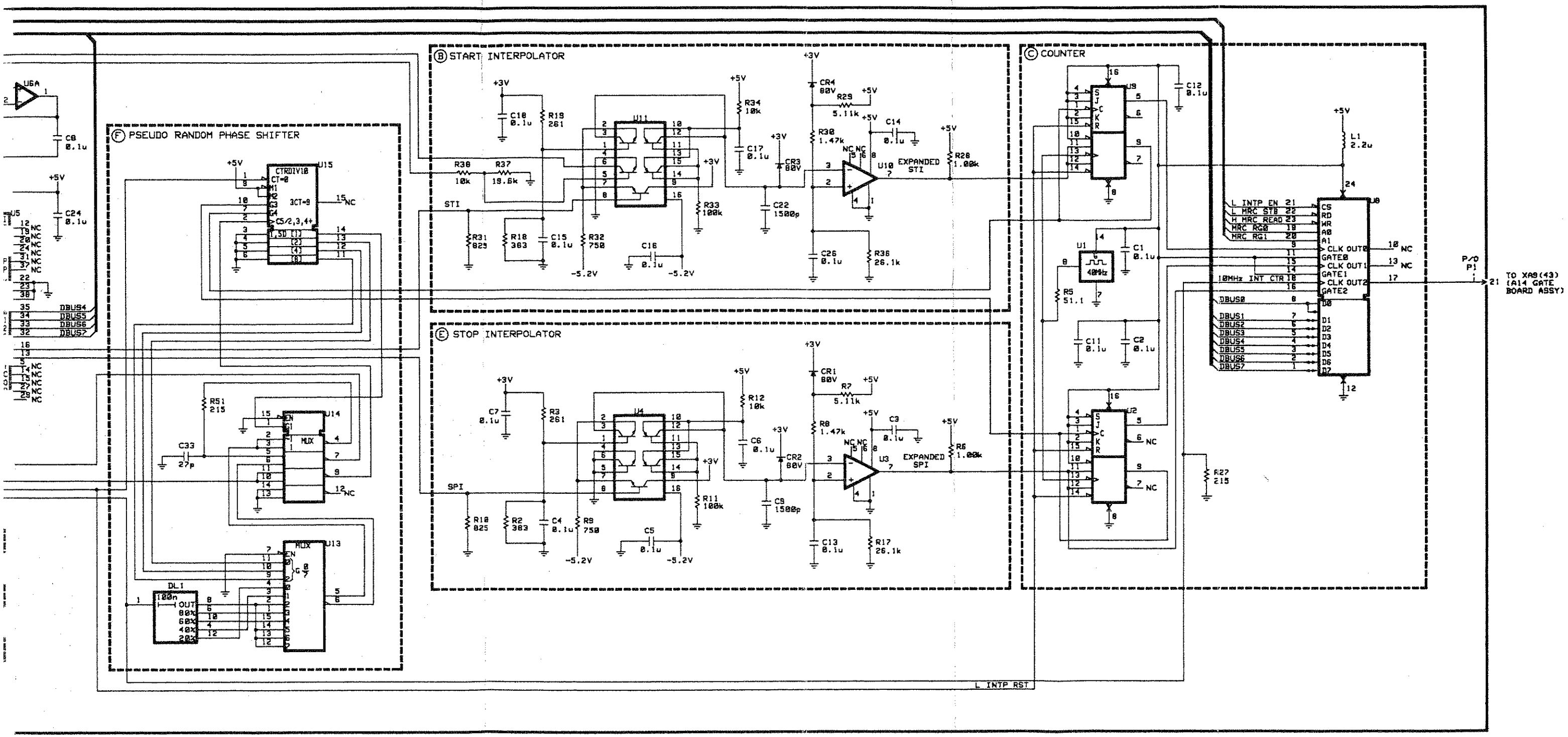
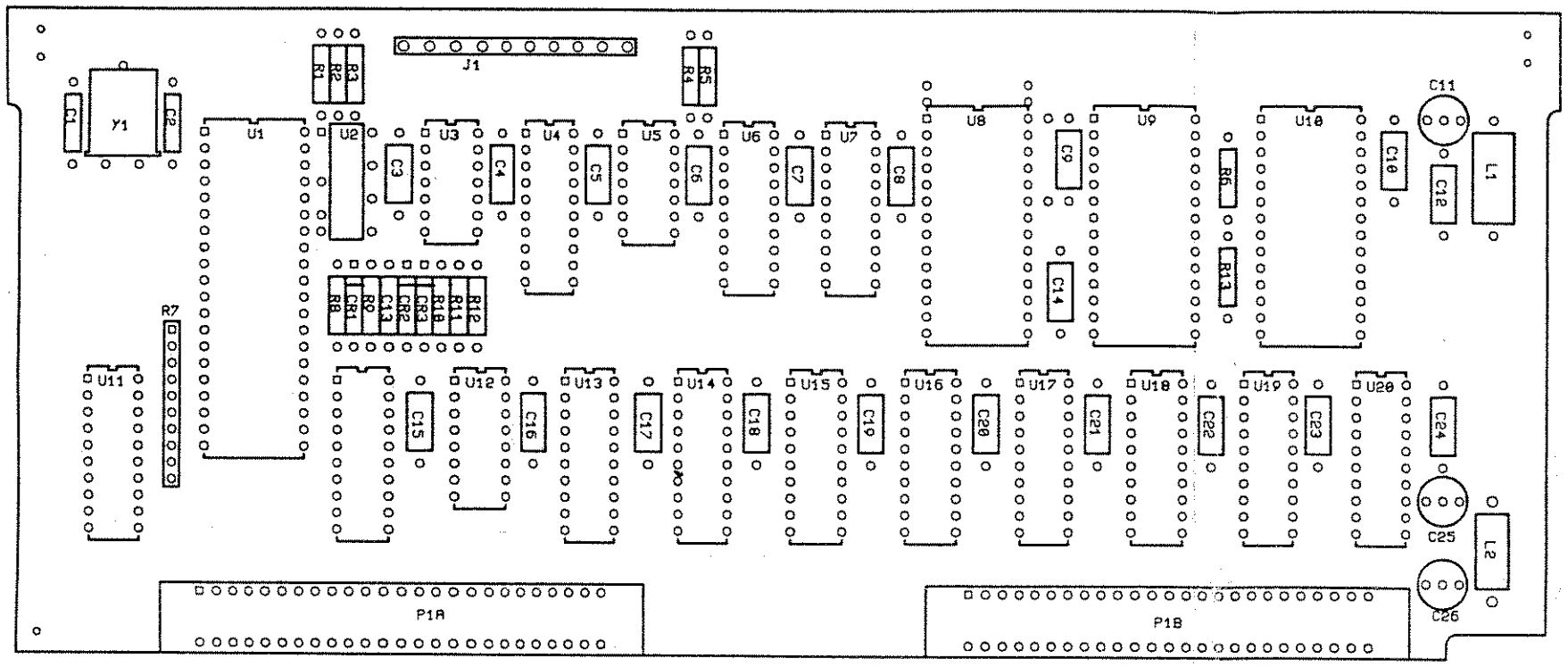


Figure 5-20. A3 Counter Assembly Component Locator/Schematic Diagram



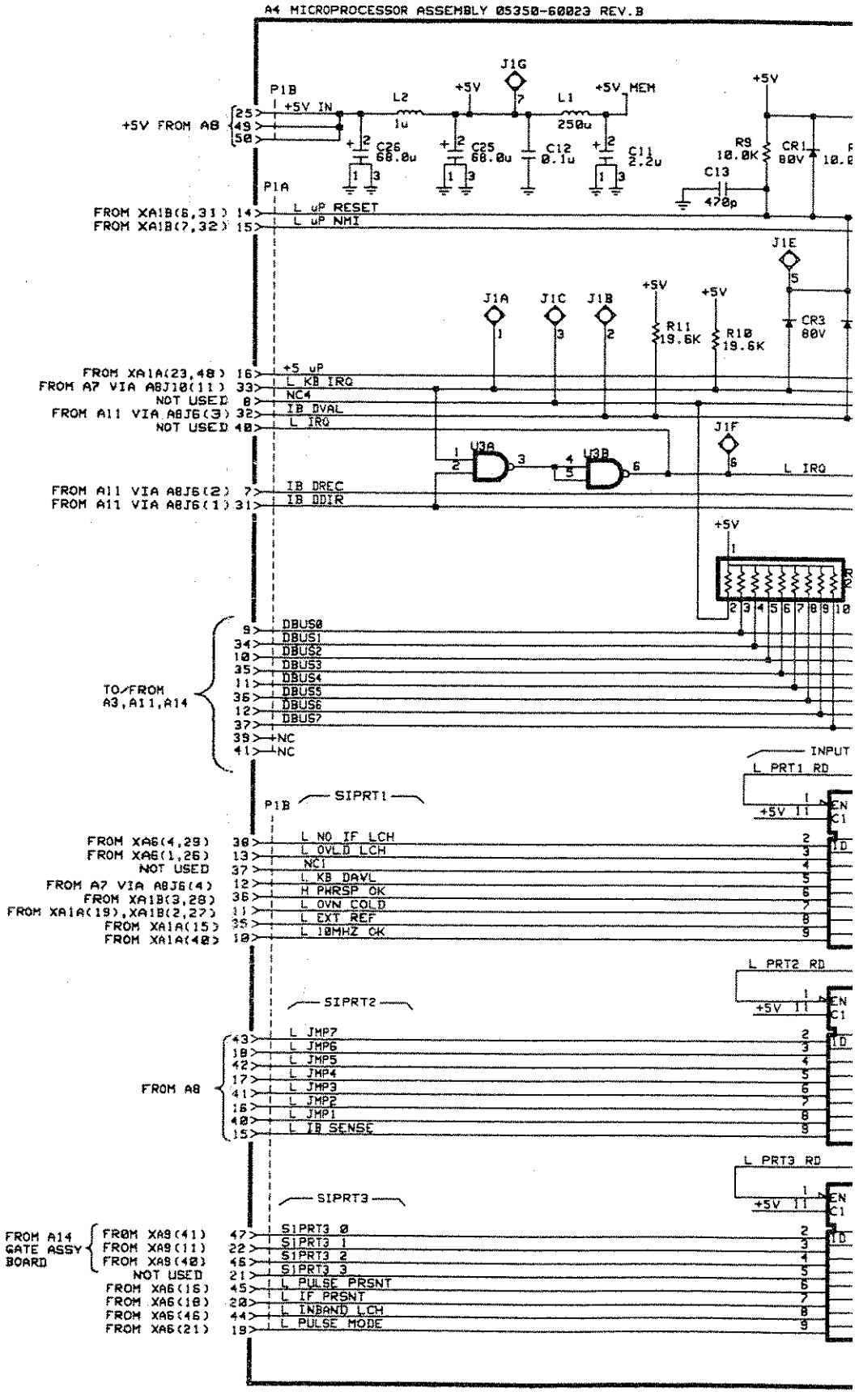
A4 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A4 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN FARADS, INDUCTANCE IN HENRIES.

3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.

4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.



A4 MICROPROCESSOR ASSEMBLY 05350-60023 REV.B

P1B +5V IN; +5V FROM A8; J1G; L2 1u; L1 250u; +5V_MEM; C26 68.0u; C25 68.0u; C12 0.1u; C11 2.2u; C13 470p; R9 10.0K; CR1 80V; R8 10.0K; +5V

P1A L uP RESET; FROM XA1B(6,31); L uP NMI; FROM XA1B(7,32)

J1A; J1C; J1B; J1E; J1F; J1H; CR3 80V; CR2 80V; R11 19.6K; R10 19.6K

FROM XA1A(23,48) +5 uP; L KB IRQ; FROM A7 VIA A8J10(11); NC4; NOT USED; IB DVAL; FROM A11 VIA A8J6(3); L IRQ; NOT USED

U3A; U3B; L IRQ

FROM A11 VIA A8J6(2) IB DREC; FROM A11 VIA A8J6(1) IB DDIR

R7 22K

TO/FROM A3,A11,A14: DBUS0; DBUS1; DBUS2; DBUS3; DBUS4; DBUS5; DBUS6; DBUS7; NC; NC

P1B SIPRT1

FROM XA6(4,29) L NO IF LCH; FROM XA6(1,25) L OVLD LCH; NOT USED NC1; FROM A7 VIA A8J6(4) L KB DAVL; FROM XA1B(3,28) H PWRSP OK; FROM XA1B(2,27) L OVN COLD; FROM XA1A(19),XA1B(2,27) L EXT REF; FROM XA1A(15) L 10MHZ OK; FROM XA1A(40)

SIPRT2

FROM A8: L JMP7; L JMP6; L JMP5; L JMP4; L JMP3; L JMP2; L JMP1; L IB SENSE

SIPRT3

FROM A14 GATE ASSY BOARD: FROM XA9(41) SIPRT3 0; FROM XA9(11) SIPRT3 1; FROM XA9(40) SIPRT3 2; SIPRT3 3; NOT USED; FROM XA6(15) L PULSE PRSNT; FROM XA6(18) L IF PRSNT; FROM XA6(46) L INBAND LCH; FROM XA6(21) L PULSE MODE

INPUT BUFFERS

L PRT1 RD: U18; L PRT2 RD: U19; L PRT3 RD: U20

MICROPROCESSOR

U1 MC68B09EL; L uP RESET; +5V; Y1 8MHz; C1 22p; C2 22p; R1 19.5K

DBUS0 DBUS1 DBUS2 DBUS3 DBUS4 DBUS5 DBUS6 DBUS7

ECLK; AS; H RD L WR; A D0; A D1; A D2; A D3; A D4; A D5; A D6; A D7; A8; A9; A10; A11; A12; A13; A14; A15

ADDRESS BUS BUFFER

U7; A D0 A D1 A D2 A D3 A D4 A D5 A D6 A D7; A0 A1 A2 A3 A4 A5 A6 A7

DELD H RD; INV EPLUS10

U6; D0 D1 D2 D3 D4 D5 D6 D7; A D0 A D1 A D2 A D3 A D4 A D5 A D6 A D7

EPLUS20; EPLUS30

DATA BUS BUFFER

U2 50n; 100% EPLUS30; 80% EPLUS20; 50% EPLUS10; 40%; 20%

P/O READ/WRITE DECODING

H RD L WR

A0-A15

P/O READ/WRITE DECODING

U12 BIN/OCT; EN; A2 A3; L PRT1 WR; L PRT2 WR; L PRT3 WR; L PRT4 WR; L PRT1 RD; L PRT2 RD; L PRT3 RD

EPLUS20; R2 0; R3 0

EPLUS10; H RD L WR; A15 A14 A13 A12 A11 A10 A9 A8

U4 PAL16L8; L PAGE EN; DELD INV E; DELD H RD; L MATE EN; H RAM WR; L RAM RD; L ROM EN; L IO EN

L uP RESET

P/O READ/WRITE DECODING

L IO EN; L ROM EN; L RAM RD; L MATE EN; L RAM WR; ECLK

D0-D7

BYPASS CAPS

C3 C4 C5 C6 C7 C8 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C14 C9 C10 0.1u; +5V; +5V_MEM

DBUS0-DBUS7

MATE TIMER

R13 10K; ECLK; L MATE EN; H RD L WR; A2 A1 A0; U9; CS1 CS0 R/~W RS2 RS1 RS0 RESET; ~IRQ; NC; G1 G2 G3 C1 C2 C3 O1 O2 O3; D0 D1 D2 D3 D4 D5 D6 D7

EPROM U8 (64Kx8); A 0 524,288; L ROM EN

R6 10K; R5 0

HM6264P-12 SRAM; A 0 8192; EPLUS30; L RAM RD; L RAM WR

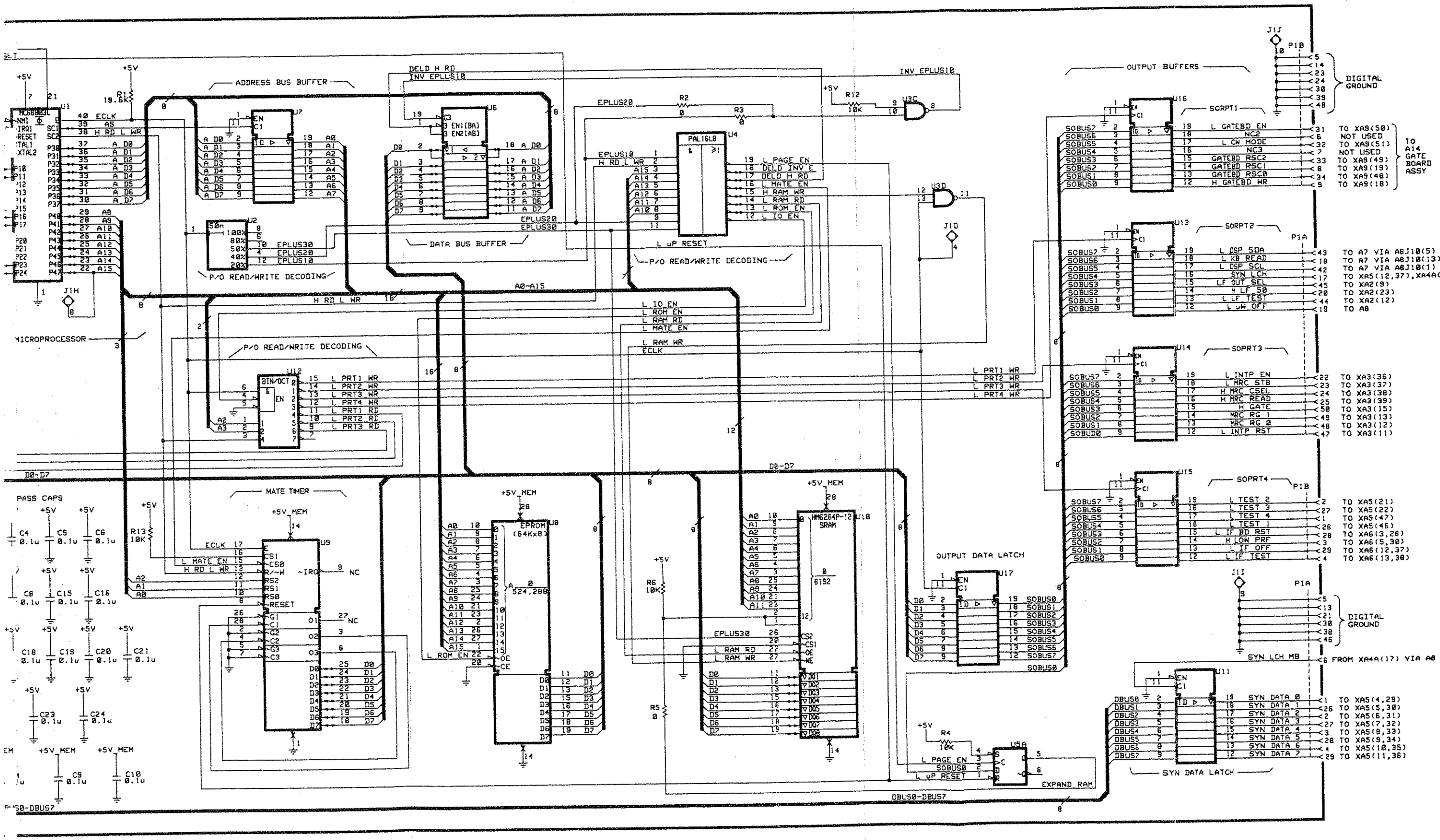


Figure 5-21. A4 Microprocessor Assembly (Standard and Option 700 HP 5361B) Component Locator/Schematic Diagram

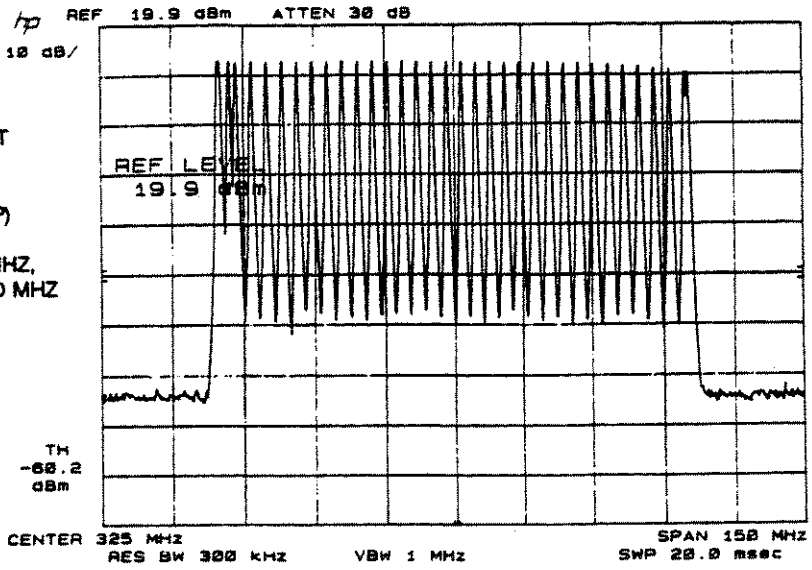
WAVEFORM A

TEST POINT: A5J2, LO OUTPUT

COUNTER SETUP: DIAG 52 (LO SWEEP)

SPECTRUM ANALYZER SETUP: CF = 325 MHZ, SPAN = 150 MHZ

COUNTER INPUT: NO INPUT

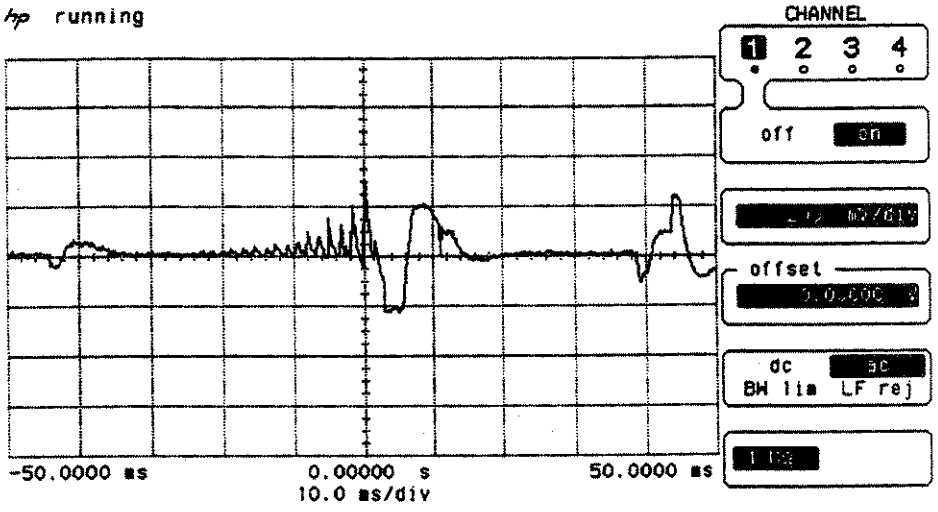


WAVEFORM B

TEST POINT: A5U1 (6)

COUNTER SETUP: AUTO MODE

COUNTER INPUT: NO INPUT

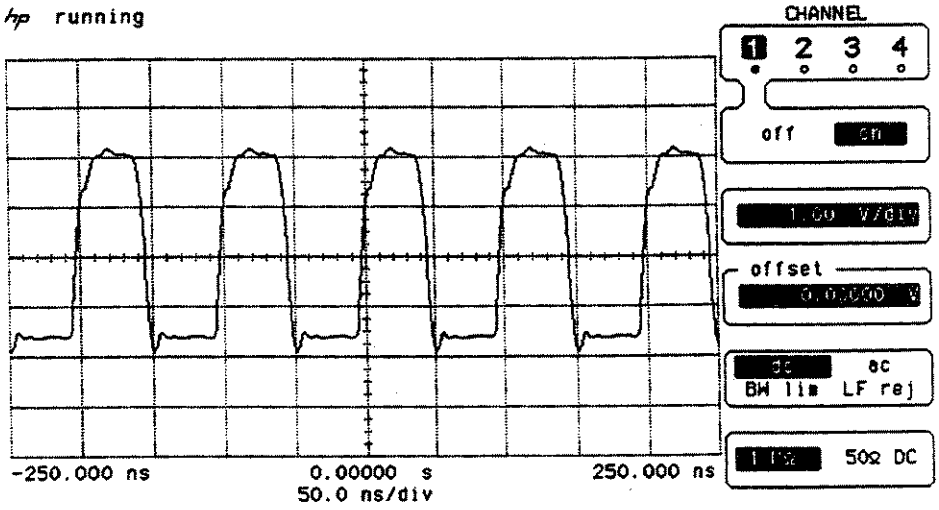


WAVEFORM C

TEST POINT: A5P1 (1)

COUNTER SETUP: AUTO MODE

COUNTER INPUT: NO INPUT



P/O Figure 5-22. A5 Waveforms

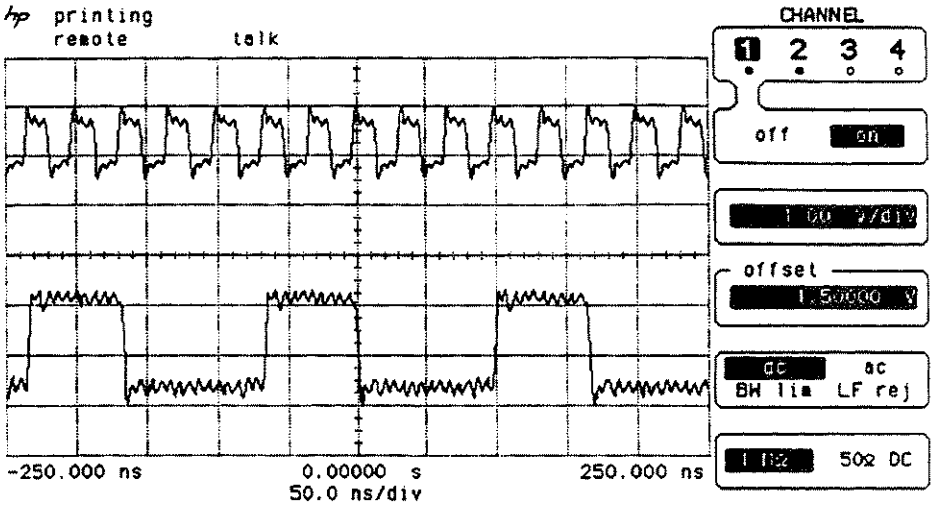
WAVEFORM D

TEST POINT: CH 1: A5U10(2)
CH 2: A5U7(11)

TRIGGER SOURCE: CH 2, -SLOPE

COUNTER SETUP: DIAG 51,
LO = 300.0 MHZ

COUNTER INPUT: NO INPUT



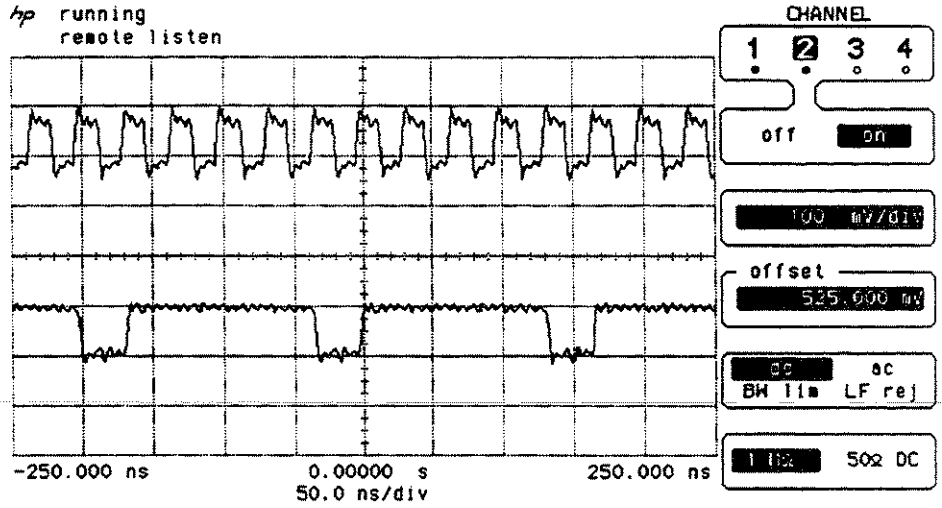
WAVEFORM E

TEST POINT: CH 1: A5U10(2)
CH 2: A5U7(3)

TRIGGER SOURCE: CH 2, -SLOPE

COUNTER SETUP: DIAG 51,
LO = 300.0 MHZ

COUNTER INPUT: NO INPUT



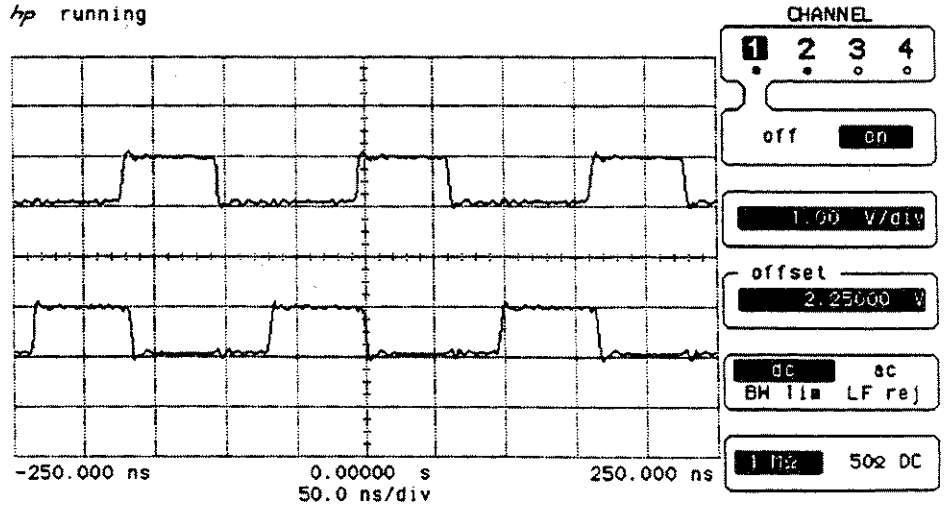
WAVEFORM F

TEST POINT: CH 1: A5U7(4)
CH 2: A5U7(14)

TRIGGER SOURCE: CH 2, -SLOPE

COUNTER SETUP: DIAG 51,
LO = 300.0 MHZ

COUNTER INPUT: NO INPUTI



P/O Figure 5-22. A5 Waveforms

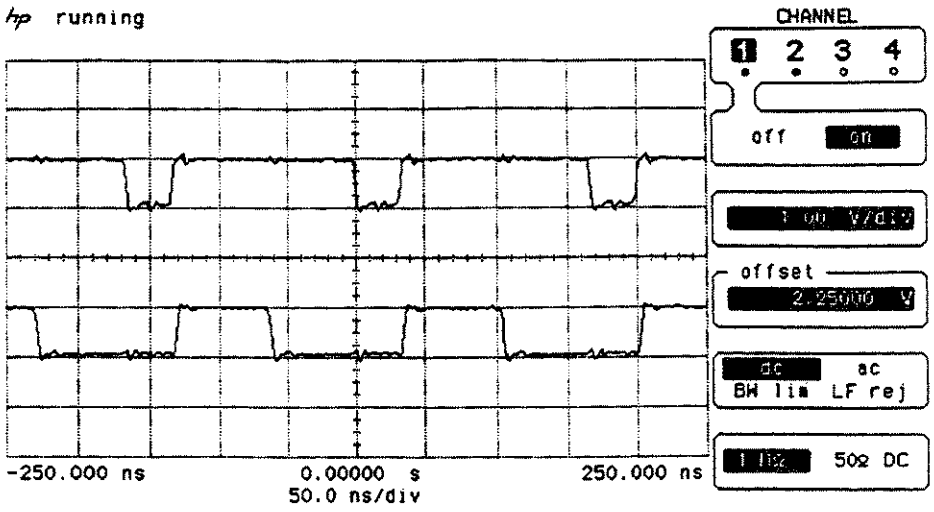
WAVEFORM G

TEST POINT: CH 1: A5U7(3)
CH 2: A5U7(14)

TRIGGER SOURCE: CH 1, -SLOPE

COUNTER SETUP: DIAG 51,
LO = 300.0 MHZ

COUNTER INPUT: NO INPUT



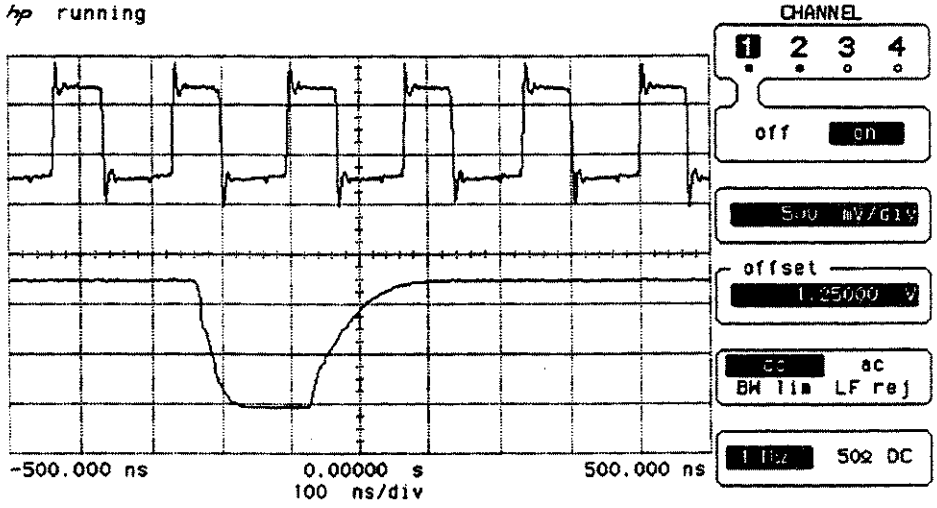
WAVEFORM H

TEST POINT: CH 1: A5U3(3)
CH 2: A5U3(14)

TRIGGER SOURCE: CH 2, -SLOPE

COUNTER SETUP: DIAG 51,
LO = 300.1 MHZ

COUNTER INPUT: NO INPUT



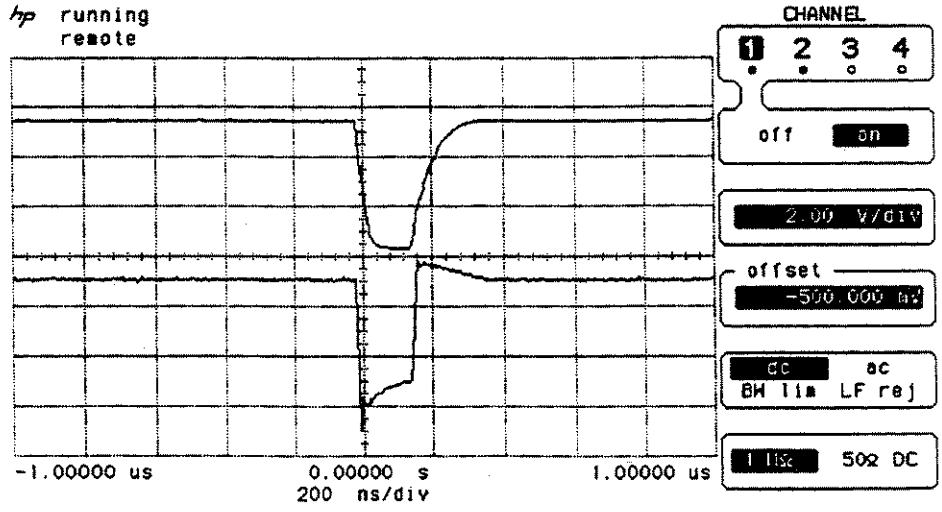
WAVEFORM I

TEST POINT: CH 1: A5U3(14)
CH 2: A5U10(13)

TRIGGER SOURCE: CH 1, -SLOPE

COUNTER SETUP: DIAG 51,
LO = 300.1 MHZ

COUNTER NPUT: NO INPUTI



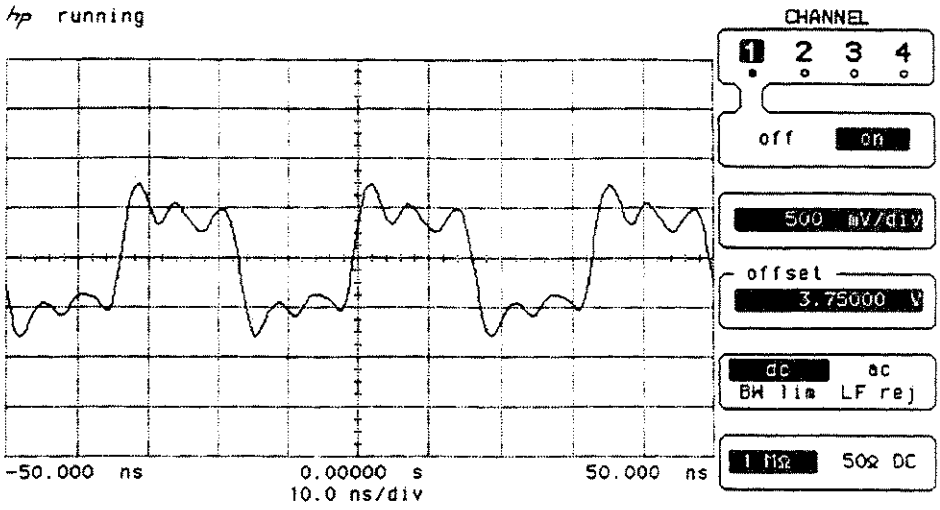
P/O Figure 5-22. A5 Waveforms

WAVEFORM J

TEST POINT: A5U10(2)

COUNTER SETUP: DIAG 51, LO = 300.0 MHZ

COUNTER INPUT: NO INPUT

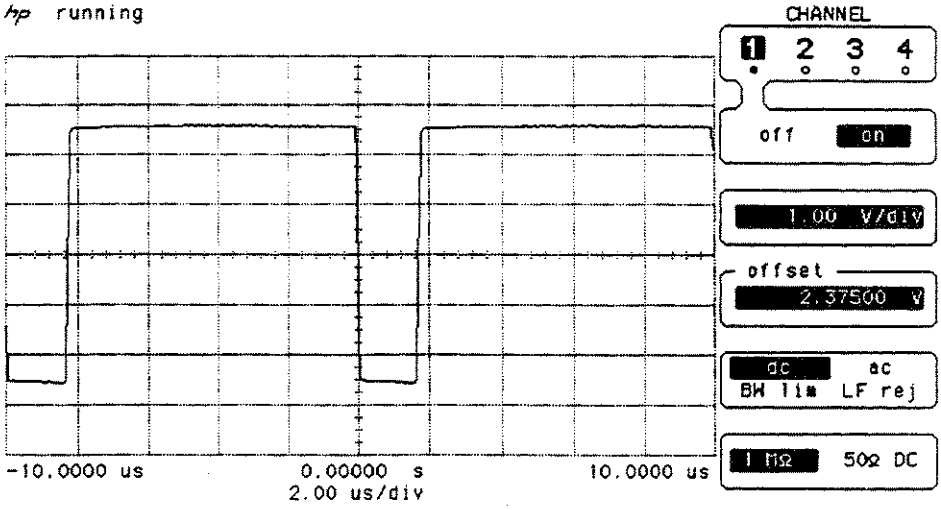


WAVEFORM K

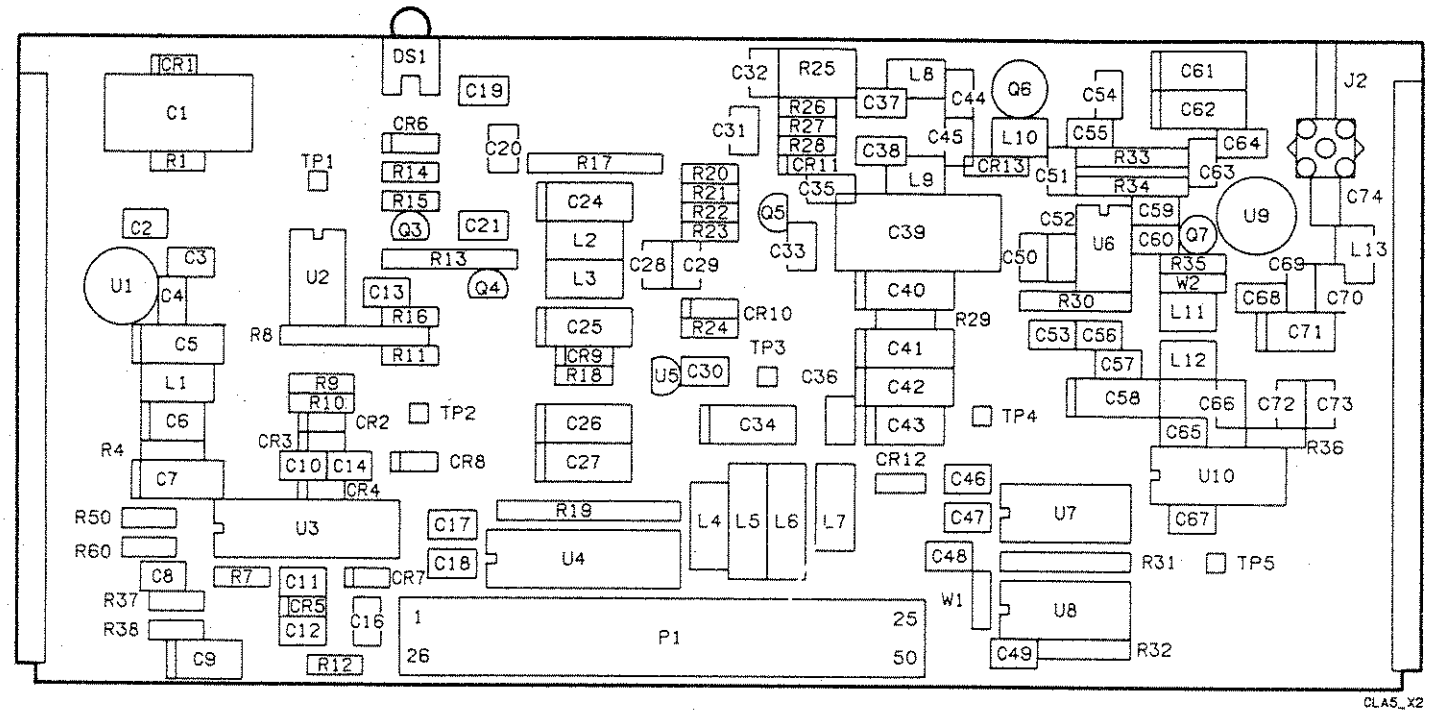
TEST POINT: A5U3(14)

COUNTER SETUP: DIAG 51, LO = 301.0 MHZ

COUNTER INPUT: NO INPUT



P/O Figure 5-22. A5 Waveforms



NOTES

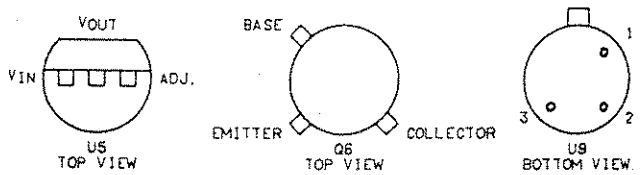
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN MICROFARADS;
   INDUCTANCE IN MICROHENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.
5. PC TRACE INDUCTANCE.
6. TOLERANCE FOR ALL DC VOLTAGES ON SCHEMATIC IS ±Ø.1 VOLT UNLESS OTHERWISE NOTED.

REFERENCE DESIGNATORS

A5 ASSEMBLY	A5 ASSEMBLY
C1 -C11, C13, C14,	P1
C16 -C20, C24 -C74	Q3-Q7
CR1-CR13	R4-R11, R13-
DS1	R24, R26-R38
J2	TP1-TP5
L1-L3	U1-U10
	W1, W2

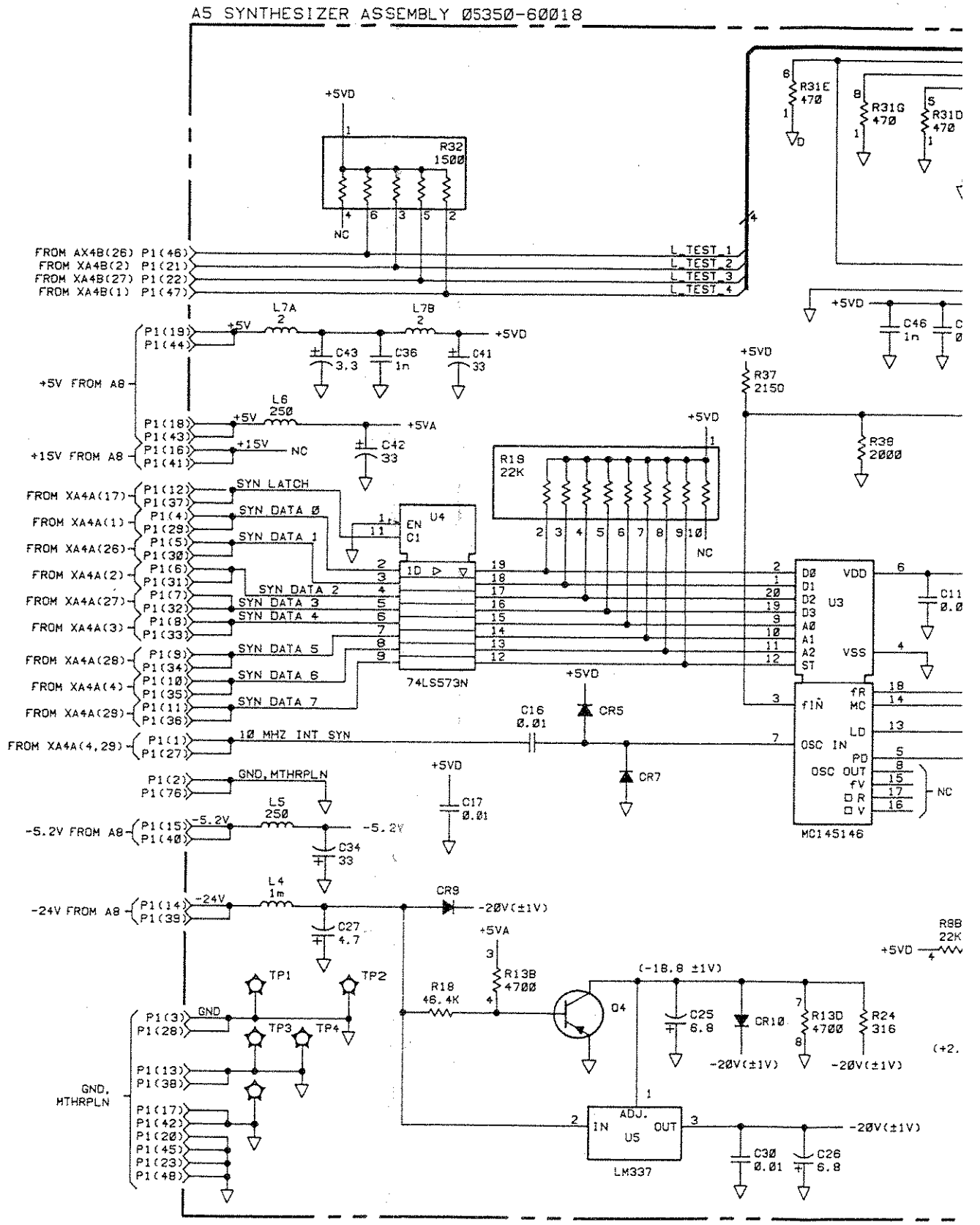
TABLE OF ACTIVE ELEMENTS

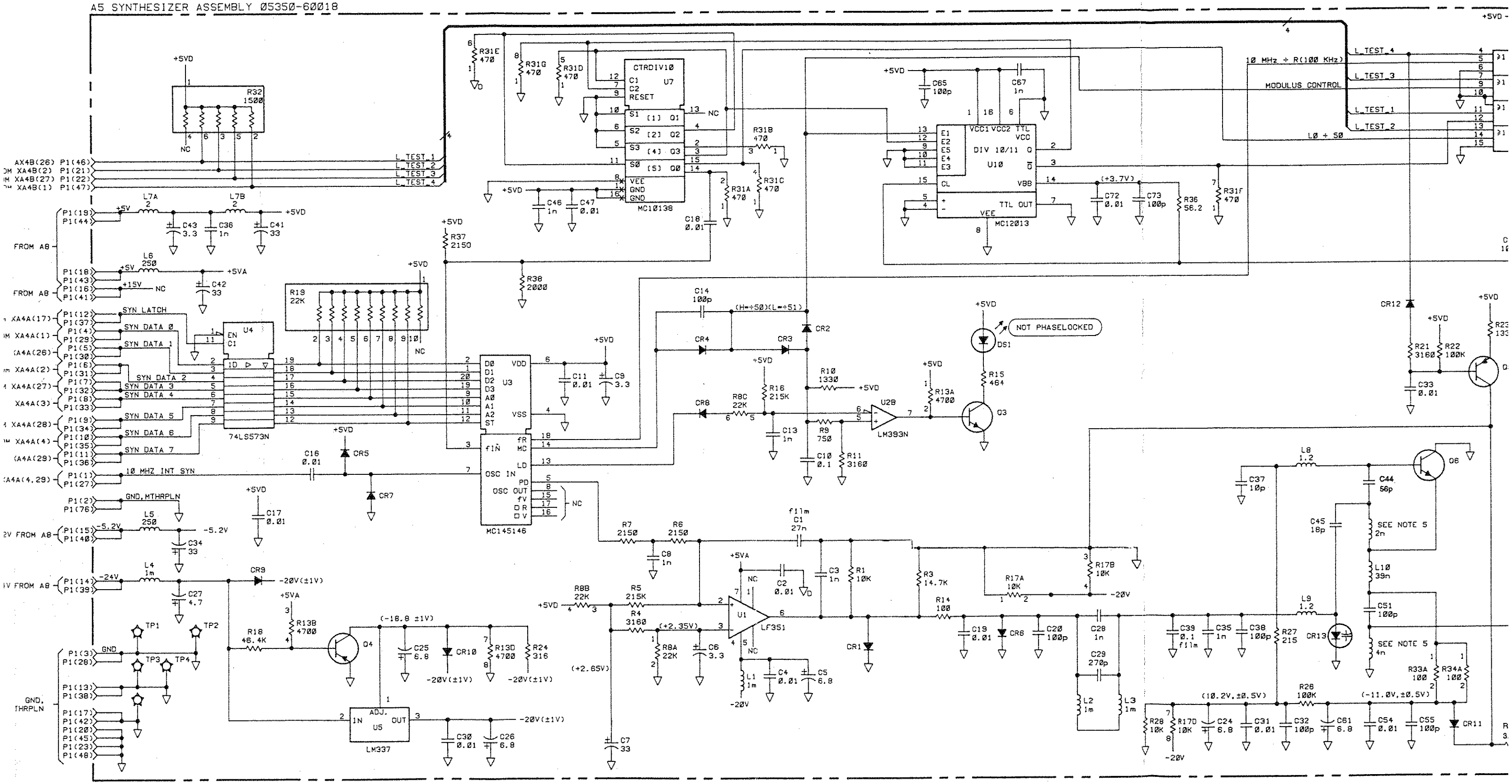
REFERENCE DESIGNATOR	HP PART NUMBER	MFG PART NUMBER
CR1-CR5, CR7-CR12	1901-0050	1N4150
CR6	1901-0734	1N5818
CR13	0122-0161	BB405B
DS1	1990-1022	HLMP-5030
Q3	1854-0215	2N3904
Q4,Q5	1853-0036	2N3906
Q6	1854-0591	BFR90
Q7	1854-0345	2N5179
U1	1826-0685	LF351H
U2	1826-0412	LM393N
U3	1820-3405	MC145146P
U4	1820-2724	SN74ALS573BN
U5	1826-1099	LM337LZ
U6	1826-0372	A251-0100
U7	1820-1383	MC10138L
U8	1820-3340	MC10H121P
U9	1813-0213	MWA130
U10	1820-1888	MC12013L



XA5
CONNECTOR PINOUT
CIRCUIT SIDE OF MOTHERBOARD

GND, MTHRPLN	26	1	1Ø MHz INT SYN
1Ø MHz INT SYN	27	2	GND, MTHRPLN
	28	3	GND, MTHRPLN
	29	4	SYN DATA Ø
	3Ø	5	SYN DATA 1
	31	6	SYN DATA 2
	32	7	SYN DATA 3
	33	8	SYN DATA 4
	34	9	SYN DATA 5
	35	1Ø	SYN DATA 6
	36	11	SYN DATA 7
	37	12	SYN LCH
	38	13	GND, MTHRPLN
	39	14	-24V
	4Ø	15	-5.2V
	41	16	+15V (NOT USED)
	42	17	GND, MTHRPLN
	43	18	+5V
	44	19	+5V
	45	2Ø	GND, MTHRPLN
L TEST 1	46	21	L TEST 2
L TEST 4	47	22	L TEST 3
	48	23	GND, MTHRPLN
AUX B	49	24	AUX A
AUX B	5Ø	25	AUX B




+5VD
R32 1500
NC
L_TEST_1
L_TEST_2
L_TEST_3
L_TEST_4
AX4B(26) P1(46)
XA4B(2) P1(21)
XA4B(27) P1(22)
XA4B(1) P1(47)
R31E 470
R31G 470
R31D 470
CTRDIV10
C1 C2 RESET
U7
S1 (1) Q1
S2 (2) Q2
S3 (4) Q3
S0 (5) Q0
VEE GND GND
MC10138
NC
R31B 470
R31A 470
R31C 470
C46 1n
C47 0.01
C18 0.01
C65 100p
C67 1n
VCC1 VCC2 TTL VCC
DIV 10/11
U10
CL
VBB
TTL OUT
VEE
MC12013
(+3.7V)
C72 0.01
C73 100p
R36 56.2
R31F 470
10 MHz ÷ R(100 KHz)
MODULUS CONTROL
LØ ÷ SØ
L7A 2
L7B 2
C43 3.3
C36 1n
C41 33
FROM A8
L6 250
+5V
+5VA
+15V
C42 33
R37 2150
R38 2000
R19 22K
SYN LATCH
SYN DATA Ø
SYN DATA 1
SYN DATA 2
SYN DATA 3
SYN DATA 4
SYN DATA 5
SYN DATA 6
SYN DATA 7
U4
EN C1 1D
74LS573N
D0 D1 D2 D3 A0 A1 A2 ST
VDD VSS
U3
C11 0.01
C9 3.3
C14 100p
(H=÷5Ø)(L=÷51)
CR4
CR3
CR2
R16 215K
R8C 22K
CR8
R10 133Ø
R9 75Ø
C13 1n
C10 0.1
R11 3160
U2B
LM393N
R13A 4700
DS1
NOT PHASELOCKED
R15 464
Q3
CR12
R21 3160
R22 100K
C33 0.01
R23 133
Q5
1Ø MHZ INT SYN
C16 0.01
CR5
CR7
C17 0.01
fIN
OSC IN
OSC OUT
fR MC LD PD fV ØR ØV
MC145146
NC
GND, MTHRPLN
L5 250
-5.2V
C34 33
L4 1m
-24V
CR9
-20V(±1V)
C27 4.7
TP1 TP2 TP3 TP4
GND
GND, THRPLN
R18 46.4K
R13B 4700
+5VA
(-18.8 ±1V)
Q4
C25 6.8
CR10
R13D 4700
R24 316
-20V(±1V)
ADJ.
U5
IN OUT
LM337
C30 0.01
C26 6.8
R7 2150
R6 2150
C8 1n
film C1 27n
R8B 22K
R5 215K
R4 3160
(+2.35V)
(+2.65V)
R8A 22K
C6 3.3
C7 33
U1
LF351
C2 0.01
C3 1n
R1 10K
R3 14.7K
R14 100
R17A 10K
R17B 10K
C19 0.01
CR6
C20 100p
C28 1n
C29 270p
L2 1m
L3 1m
C4 0.01
C5 6.8
L1 1m
CR1
C39 0.1 film
C35 1n
C38 100p
R27 215
CR13
L8 1.2
C37 10p
C44 56p
C45 18p
SEE NOTE 5
2n
L10 39n
C51 100p
4n
L9 1.2
R33A 100
R34A 100
R26 100K
(10.2V, ±0.5V)
(-11.0V, ±0.5V)
R28 10K
R17D 10K
C24 6.8
C31 0.01
C32 100p
C61 6.8
C54 0.01
C55 100p
CR11
Q6

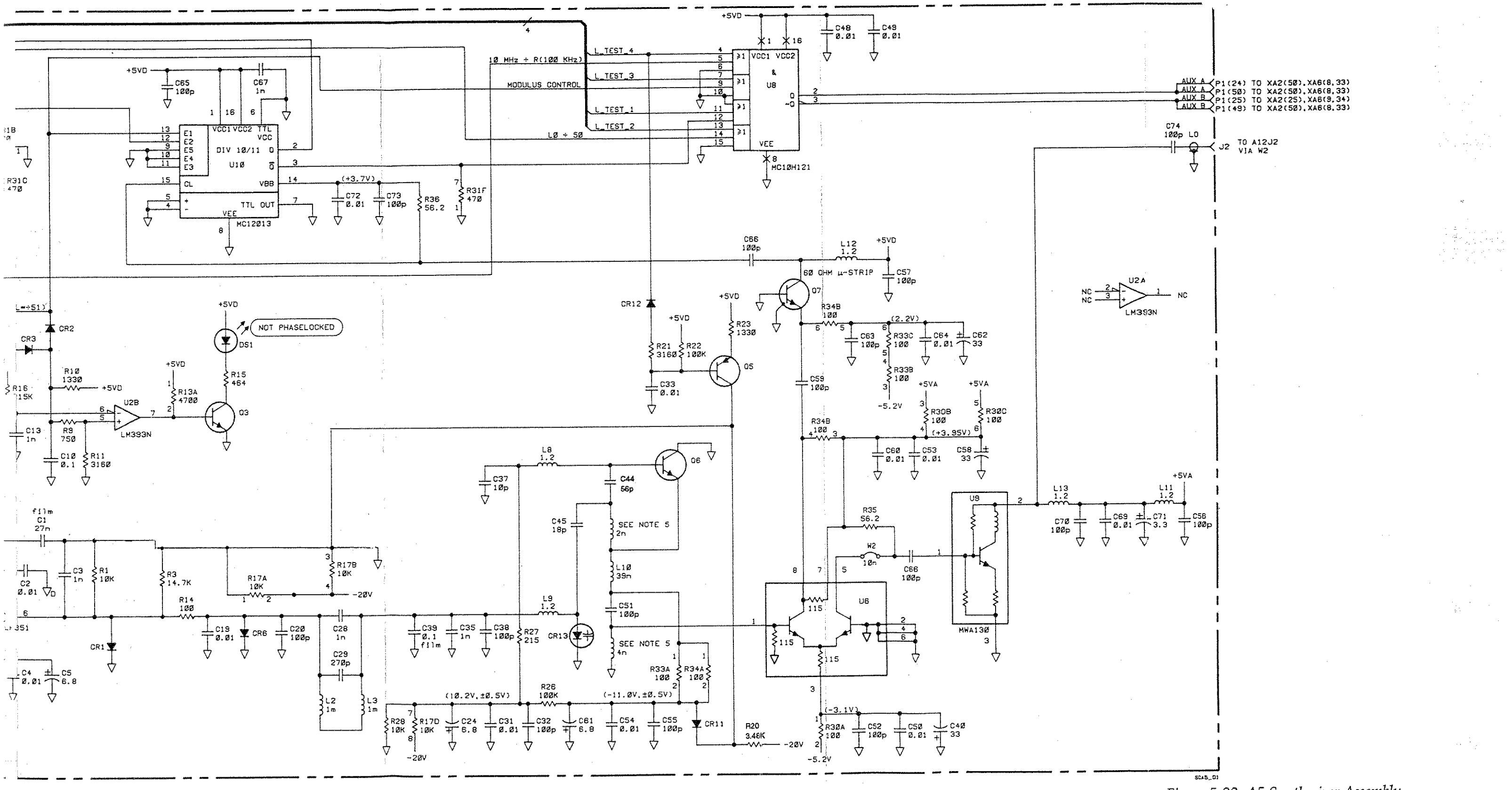


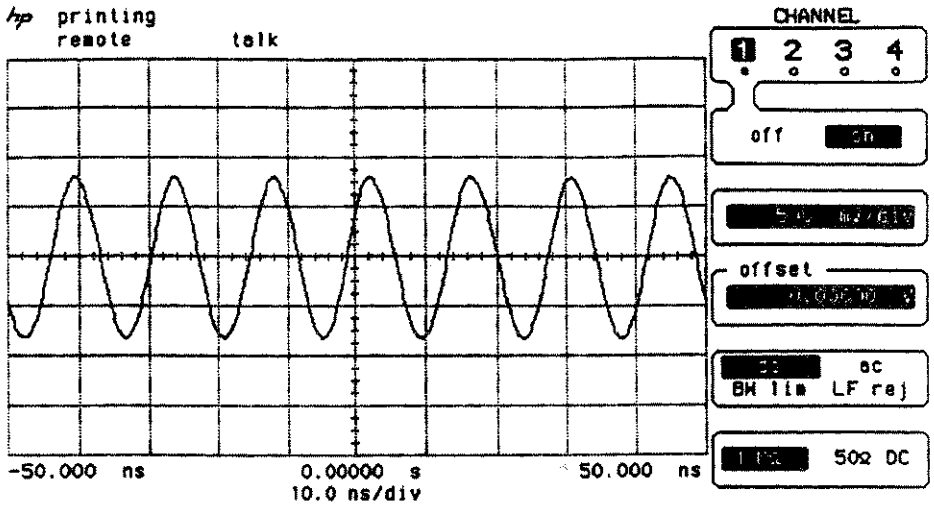
Figure 5-22. A5 Synthesizer Assembly Component Locator/Schematic Diagram

WAVEFORM A

TEST POINT: A12J1, IF OUTPUT OF MICROWAVE MODULE

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 770 MHZ

COUNTER INPUT: 770 MHZ, –10 DBM

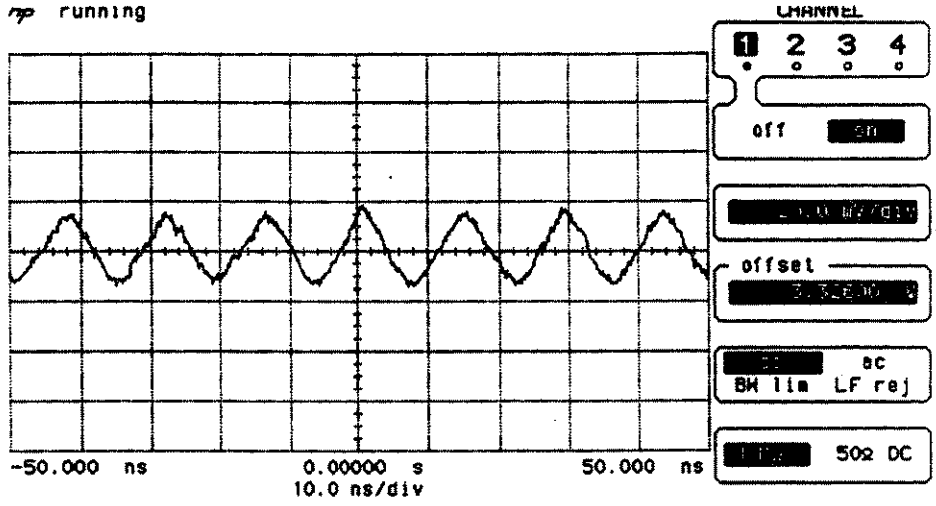


WAVEFORM B

TEST POINT: A6L11(2), LOW_PASS_ FILTER_1

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 770 MHZ

COUNTER INPUT: 770 MHZ, –10 DBM

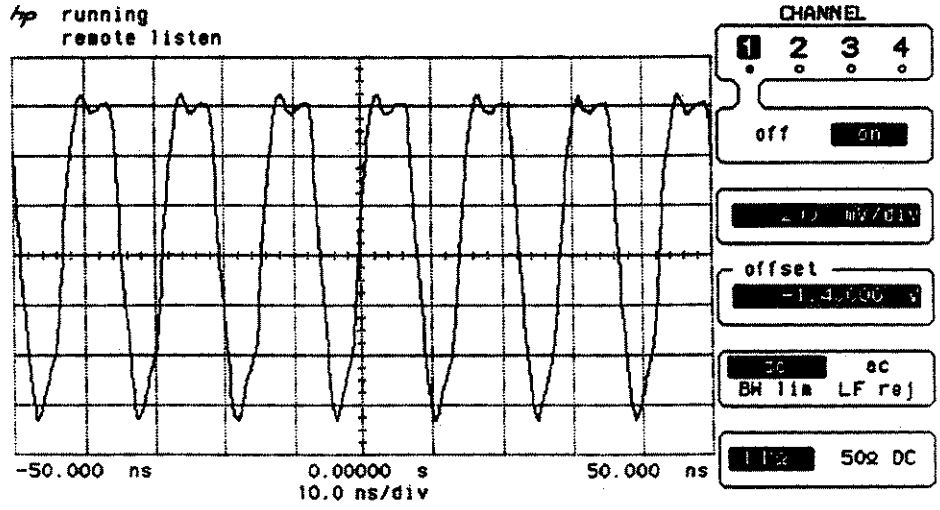


WAVEFORM C

TEST POINT: A6U2(15), +IF_NEW

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 770 MHZ

COUNTER INPUT: 770 MHZ, –10 DBM



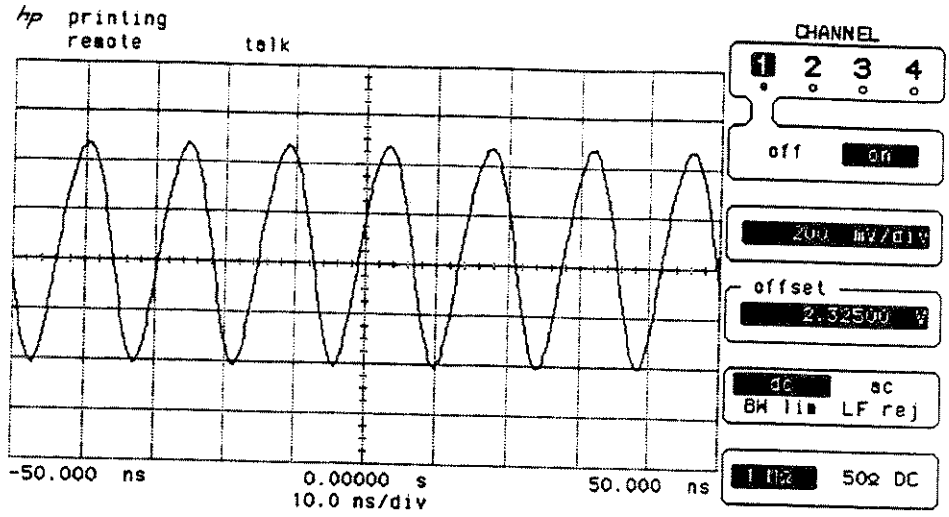
P/O Figure 5-23. A6 Waveforms

WAVEFORM D

TEST POINT: A6U5(16), +NEW_IF_MON

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 770 MHZ

COUNTER INPUT: 770 MHZ, −10 DBM

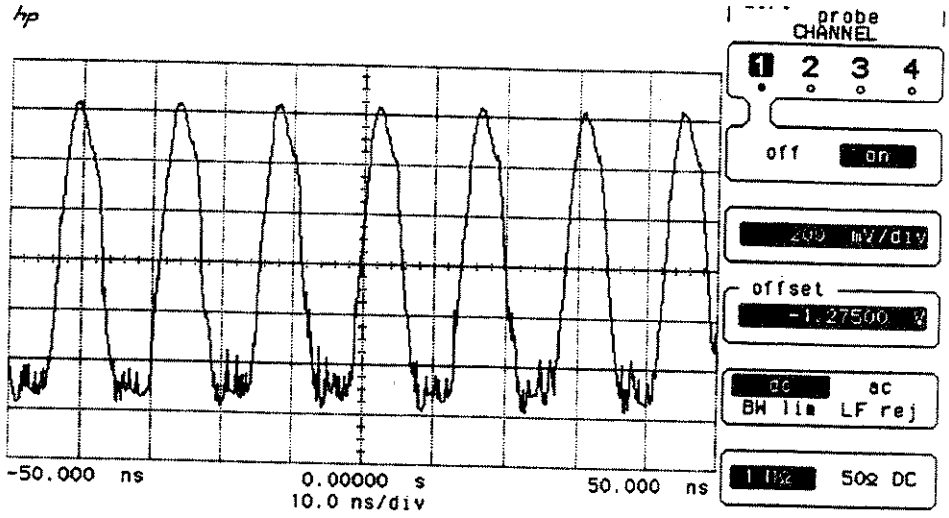


WAVEFORM E

TEST POINT: A6U2(14), −IF_NEW

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 770 MHZ

COUNTER INPUT: 770 MHZ, −10 DBM

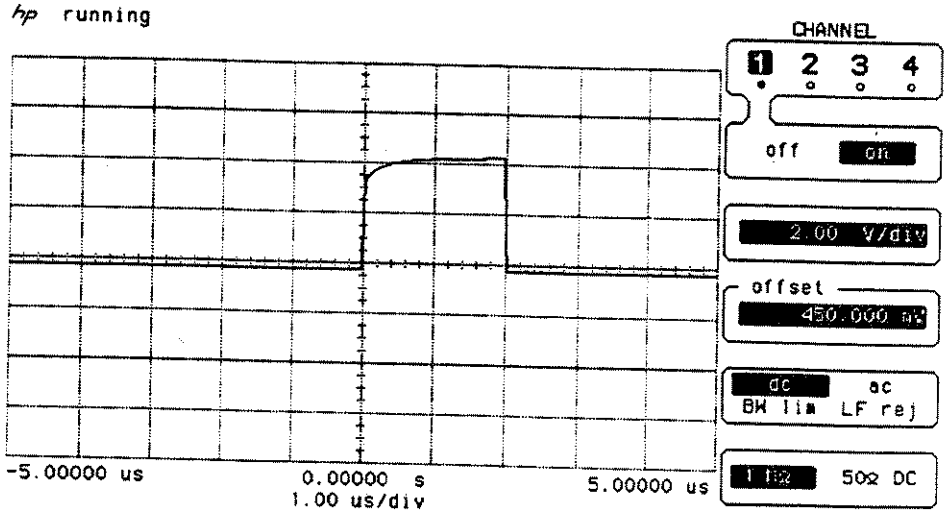


WAVEFORM F

TEST POINT: A6U19(13), L_MODE_LCH

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 770 MHZ

COUNTER INPUT: 770 MHZ, −10 DBM



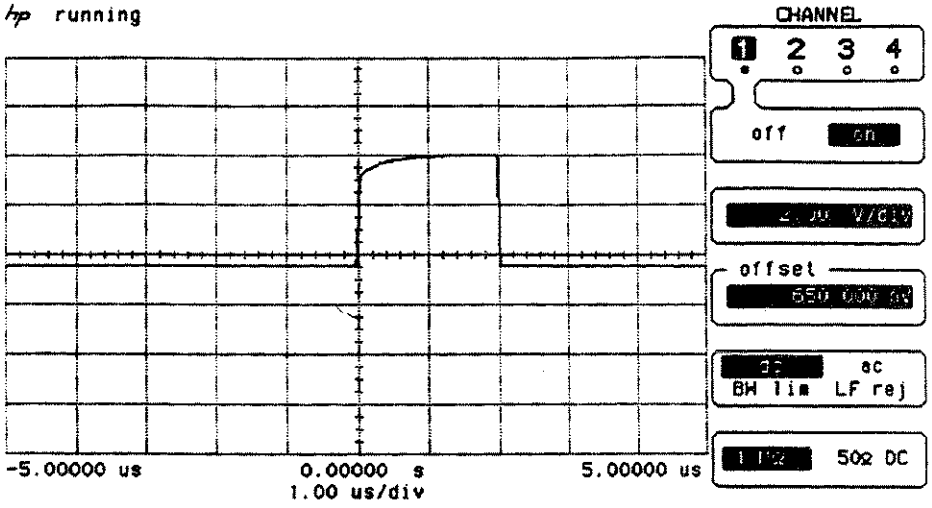
P/O Figure 5-23. A6 Waveforms

WAVEFORM G

TEST POINT: A6U19(7), L_INBAND_LCH

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 770 MHZ

COUNTER INPUT: 770 MHZ, −10 DBM

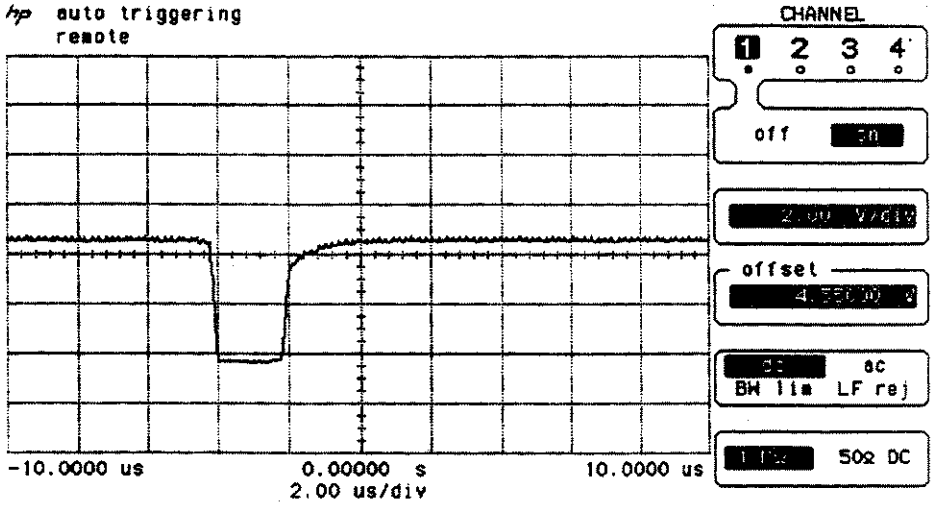


WAVEFORM H

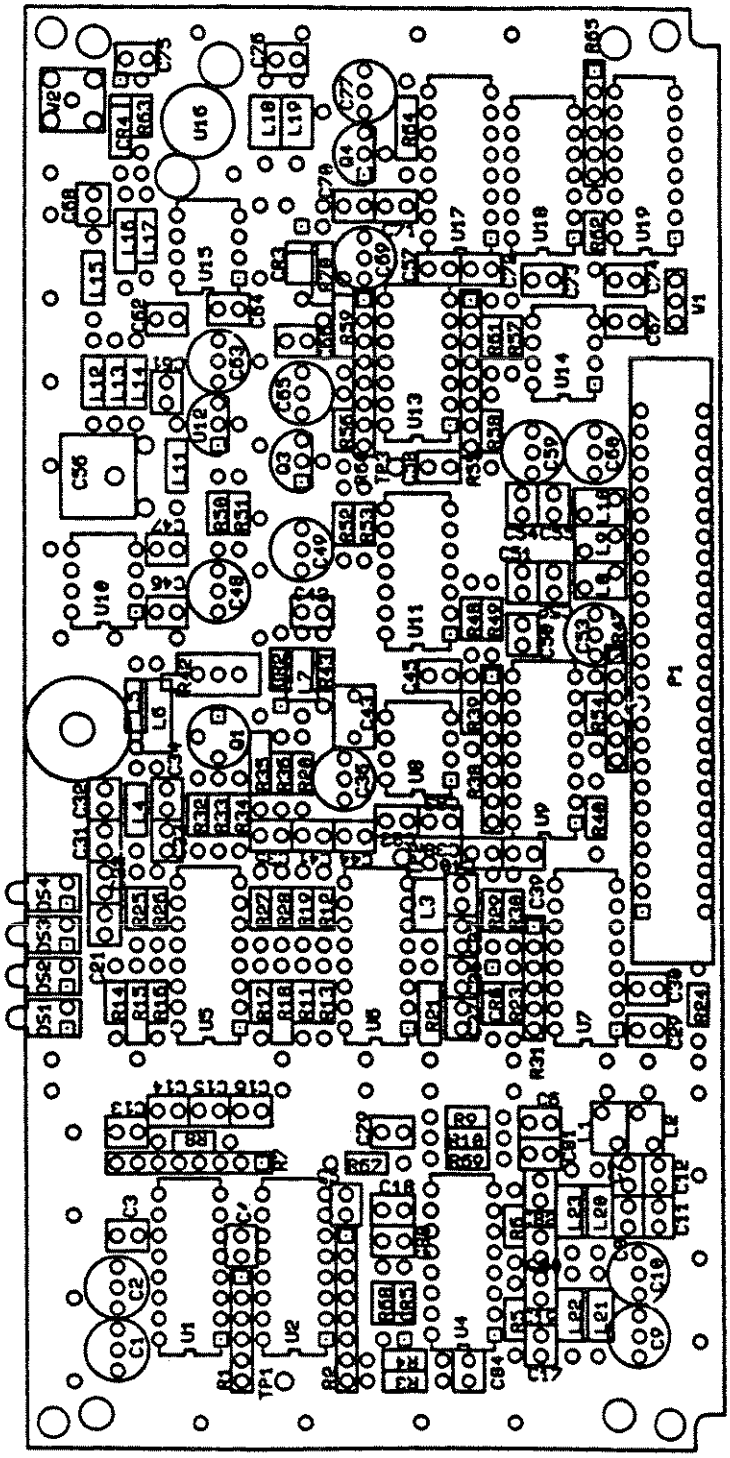
TEST POINT: A6U19(15), L_IF_BD_RST

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 770 MHZ

COUNTER INPUT: 770 MHZ, −10 DBM



P/O Figure 5-23. A6 Waveforms



P/O Figure 5-23. A6 Component Locator

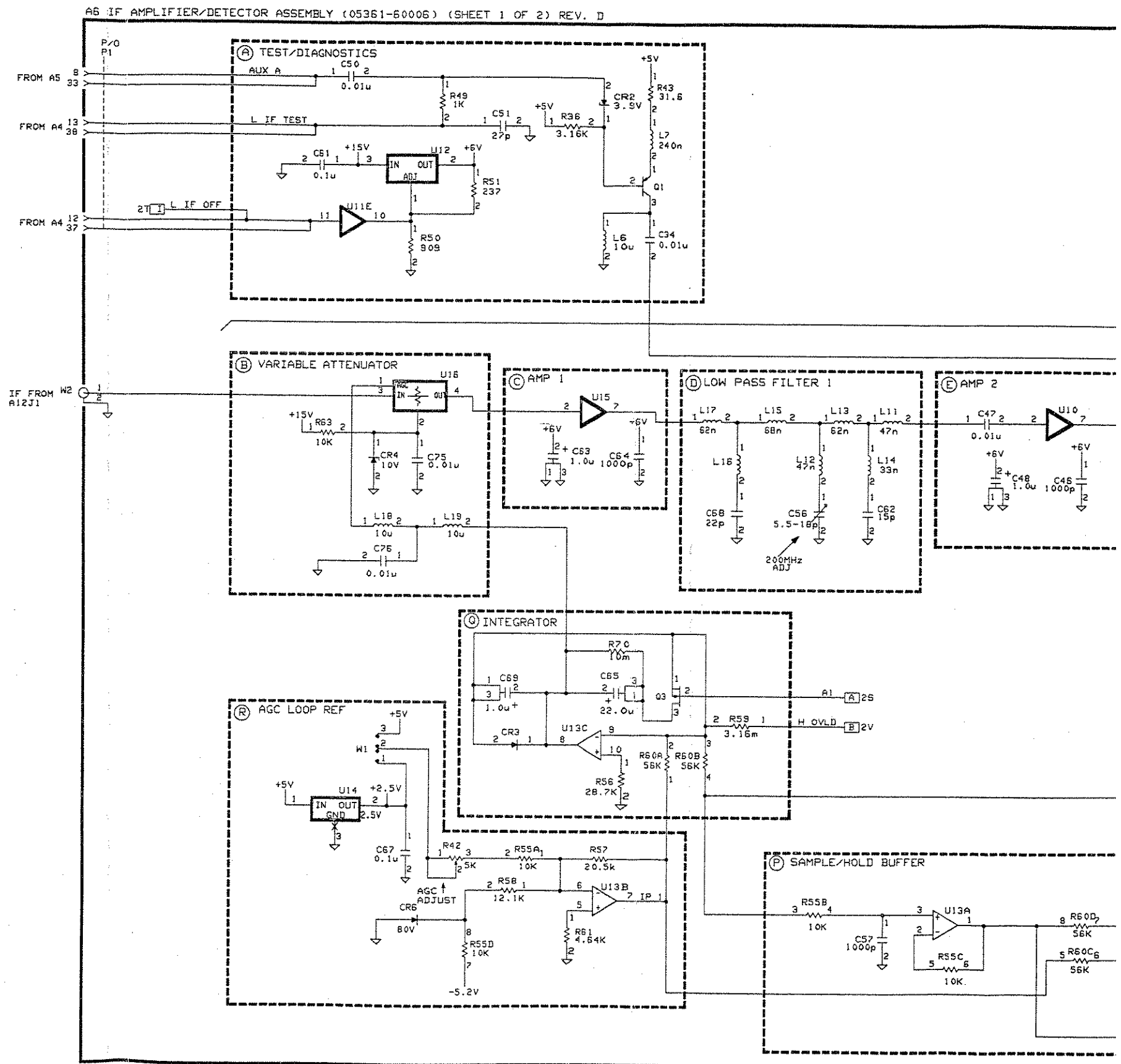
A6 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A6 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN FARADS, INDUCTANCE IN HENRIES.

3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.

4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.



EST/DIAGNOSTICS
AUX A
C50 0.01u
R49 1K
F TEST
C51 22p
+5V
R36 3.16K
CR2 3.9V
+5V
R43 31.6
L7 240n
Q1
C61 0.1u
+15V
U12
IN OUT ADJ
+6V
R51 237
U11E
R50 909
L6 10u
C34 0.01u

AGC LOOP

ARIABLE ATTENUATOR
U16
AGC IN OUT
+15V
R63 10K
CR4 10V
C75 0.01u
L18 10u
L18 10u
C76 0.01u

C AMP 1
U15
+6V
C63 1.0u
C64 1000p

D LOW PASS FILTER 1
L17 82n
L15 68n
L13 82n
L11 47n
L16
C68 22p
L12 47n
C56 5.5-18p
200MHz ADJ
L14 33n
C62 15p

E AMP 2
C47 0.01u
U10
+6V
C48 1.0u
C46 1000p

F LOW PASS FILTER 2
L5 56n
L4 82n
C32 22p
C31 12p

G AMP 3 +5V
C36 1.0u
C22 1000p
R25 75
R28 75
C41 1000p
C33 0.01u
U5E
U5C
R26 68.1
R33 10
C35 39p
R27 68.1
R32 14.7
R34 14.7
R35 147
C42 1000p
C49 1.0u
-5.2V

H BUFFER AMPS
R16 26.1
U5D
C14 0.01u
R15 215
U5B
R17 26.1
R18 215
C15 0.01u

J SCHMITT TRIGGER
R7C 68
R7A 68
C16 0.01u
+2.5V
R8 1.33K
R7D 68
C13 0.01u

I INBAND DRIVER
+5V
R11 261
U6A
R13 42.2
R12 196

K INBAND 35
CR5
80V
L20 120n
C7 39p
C8 68p

GC LOOP REF
+5V
W1
U14
IN OUT GND
+2.5V
2.5V
C67 0.1u
R42 5K
R55A 10K
R57 20.5k
R58 12.1K
AGC ADJUST
CR6
8.0V
R55D 10K
R61 4.64K
-5.2V

Q INTEGRATOR
R70 10m
C69 1.0u
C65 22.0u
Q3
A1 2S
CR3
U13C
R59 3.16m
H OVLD B 2V
R60A 56K
R60B 56K
R56 28.7K

P SAMPLE/HOLD BUFFER
2V C RV 1
R55B 10K
C57 1000p
U13A
R55C 10K
R60D 56K
R60C 56K
R52 215K
U13D
R53 23.7K

O SAMPLE/HOLD
+15V
C45 0.01u
-5.2V
C83 0.01u
U8
C43 2200p
SH 1 D 2S

N ENVELOPE & AGC DETECTORS
+5V
U6B
U6D
U6E
U6C
C38 0.01u
C37 0.01u
R21 4.64M
C26 56p
C27 56p
L3 11u
C40 2.2p
R29 1.47K

M ENVELOPE COMPARA
C29 0.01u
+2.5V
R30 1.62K
R23 17.8K
C39 100p

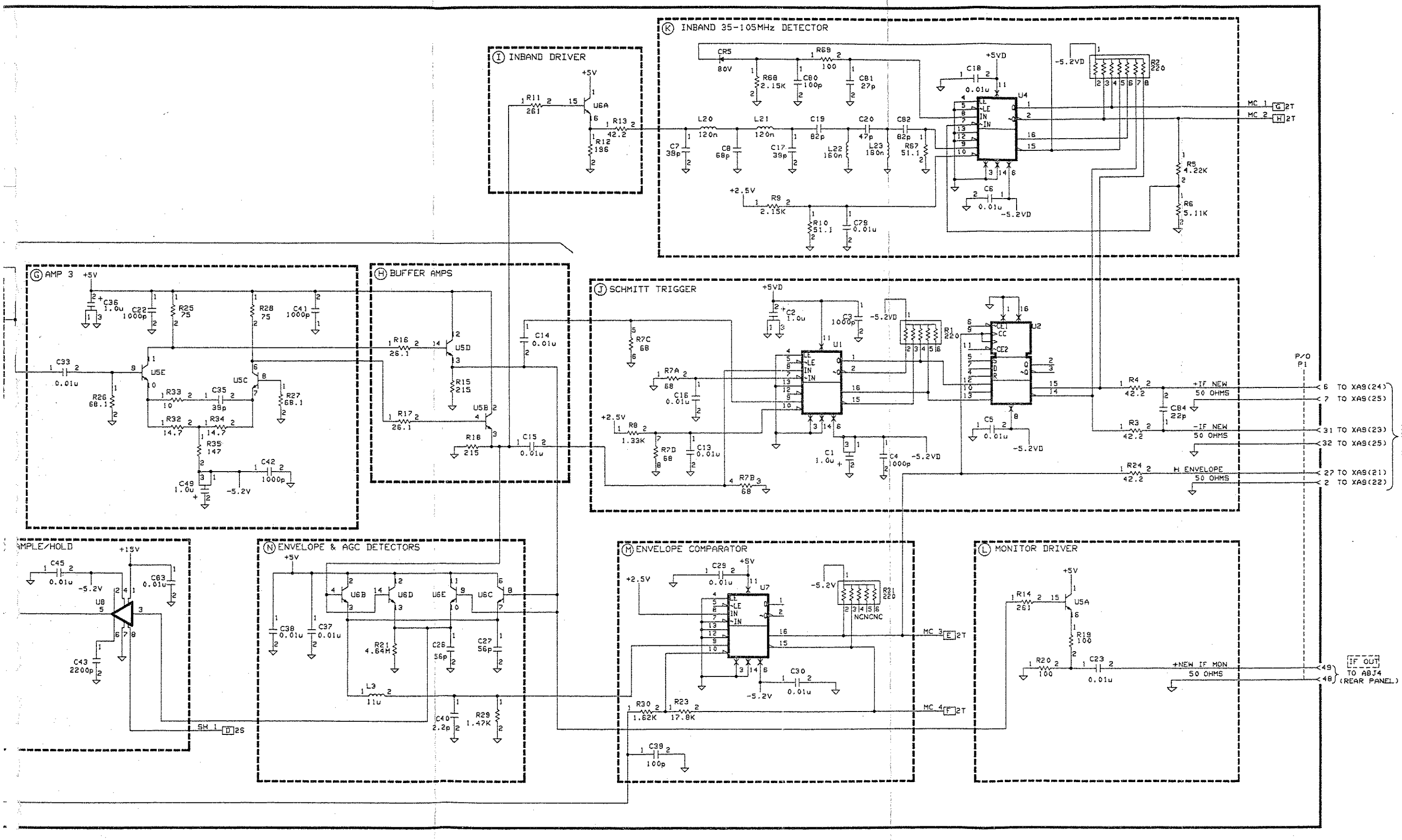


Figure 5-23. A6 Amplifier/Detector Assembly Schematic Diagram (Sheet 1 of 2)

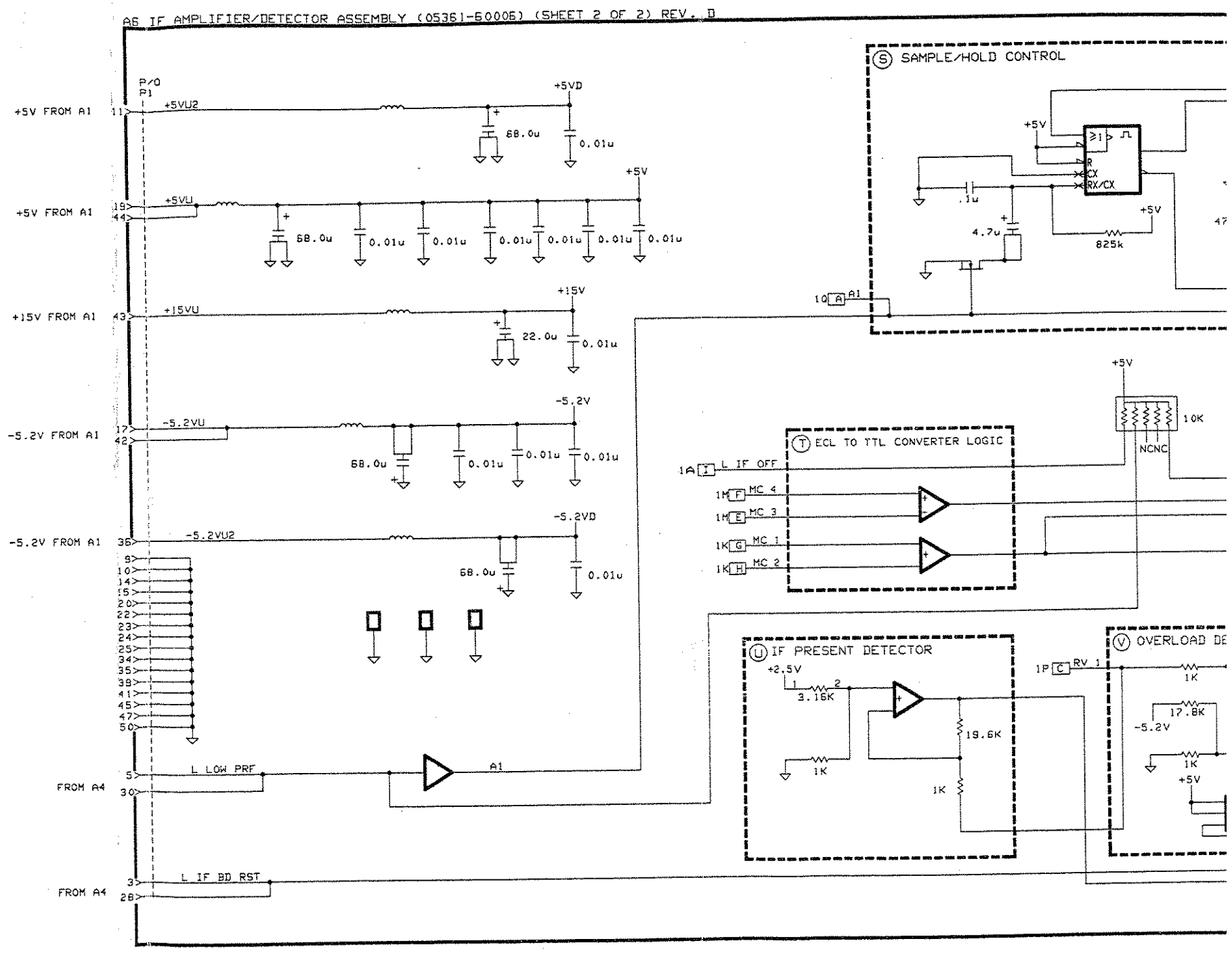
A6 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A6 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN FARADS, INDUCTANCE IN HENRIES.

3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.

4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.



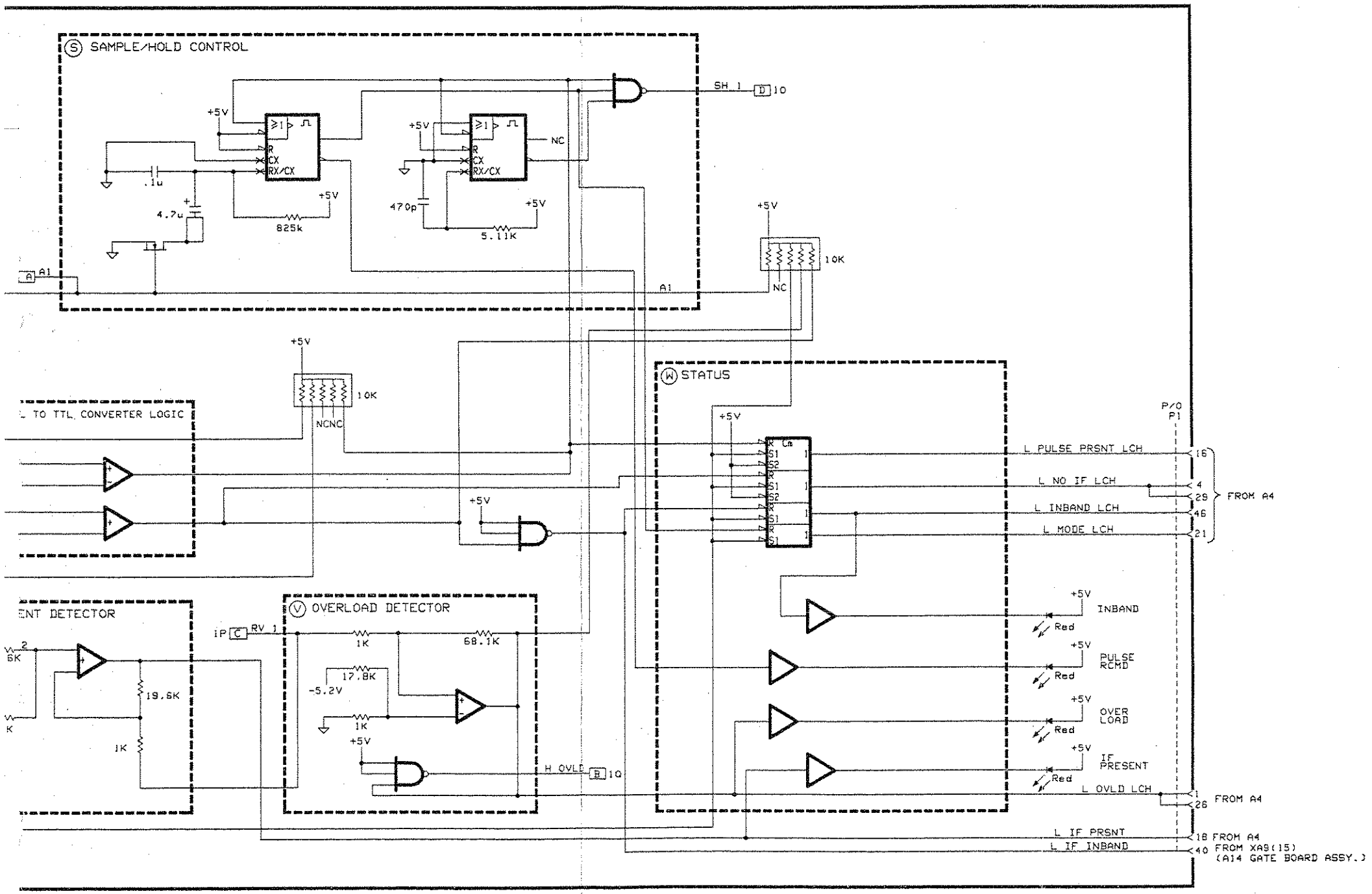


Figure 5-23. A6 Amplifier/Detector Assembly Schematic Diagram (Sheet 2 of 2)

A7 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A7 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN MICROFARADS, INDUCTANCE IN MICROHENRIES.

3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.

4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.

A7J3
CONNECTOR PINOUT
CIRCUIT SIDE OF A7 BOARD

DSP SDA	16	1	GND, DIGITAL
+5V	15	2	NC
+15V	14	3	L KB IRQ
L KB DAVL	13	4	L STBY
DSP SCL	12	5	L KB READ
STBY LED	11	6	DBS 3
DBUS 4	10	7	DBS 5
DBUS 6	9	8	DBS 7

A8J10
CONNECTOR PINOUT
CIRCUIT SIDE OF MOTHERBOARD

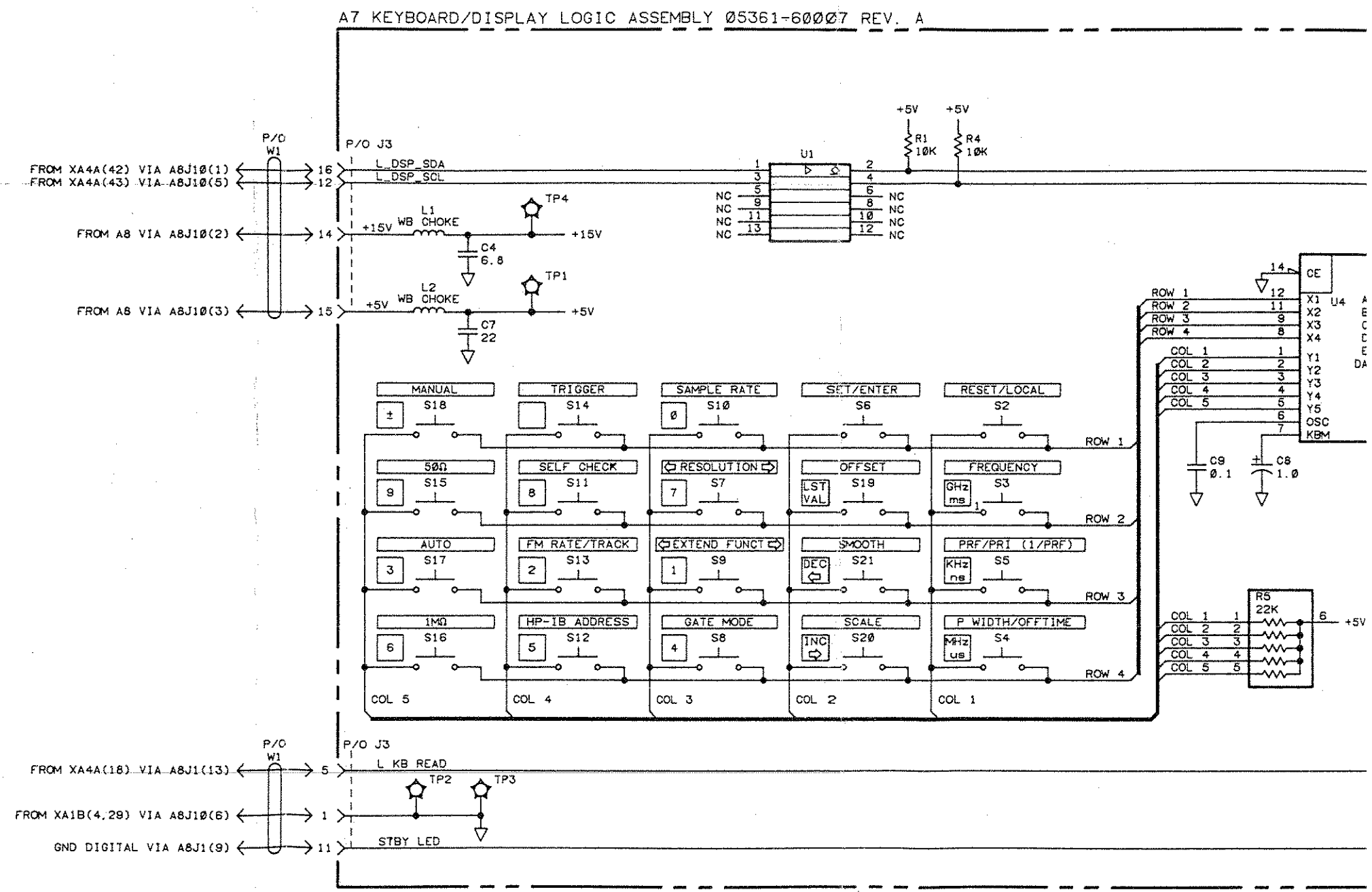
GND, DIGITAL	9	1	DSP SDA
NC	10	2	+5V
L KB IRQ	11	3	+15V
L STBY	12	4	L KB DAVL
L KB READ	13	5	DSP SCL
DBUS 3	3	6	STBY LED
DBUS 5	5	7	DBUS 4
DBUS 7	7	8	DBUS 6

A7 TEST POINTS
CIRCUIT SIDE OF A7 BOARD

TP1	+5V
TP2	GND
TP3	GND
TP4	+15V
TP5	NC
TP6	NC
TP7	DA
TP8	~L KB IRQ
TP9	NC
TP10	NC

A7J4
CIRCUIT SIDE OF A7 BOARD

DSP SDA(VIA A7U1)	1
DSP SCL(VIA A7U1)	2
+5V	3
GND	4



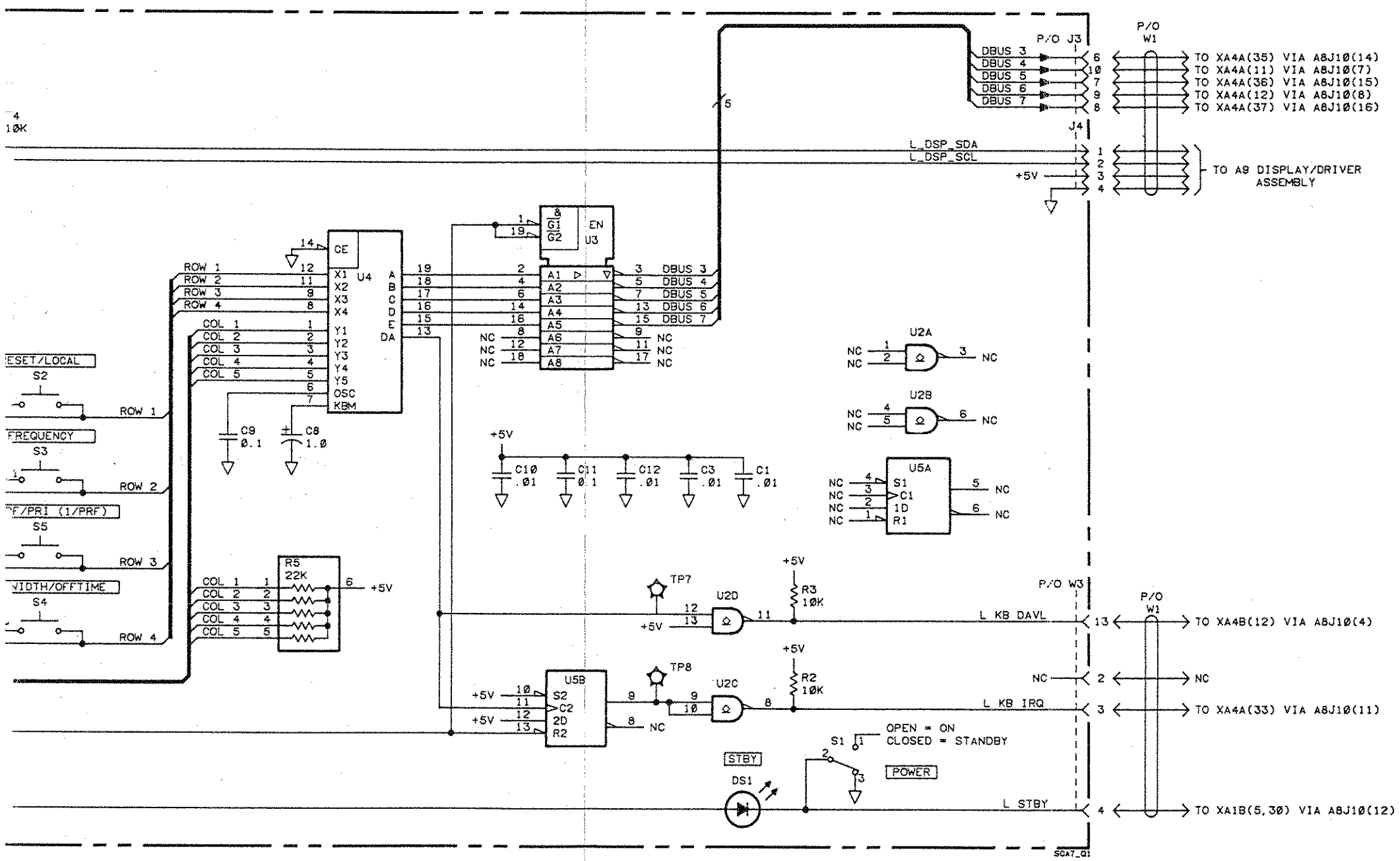
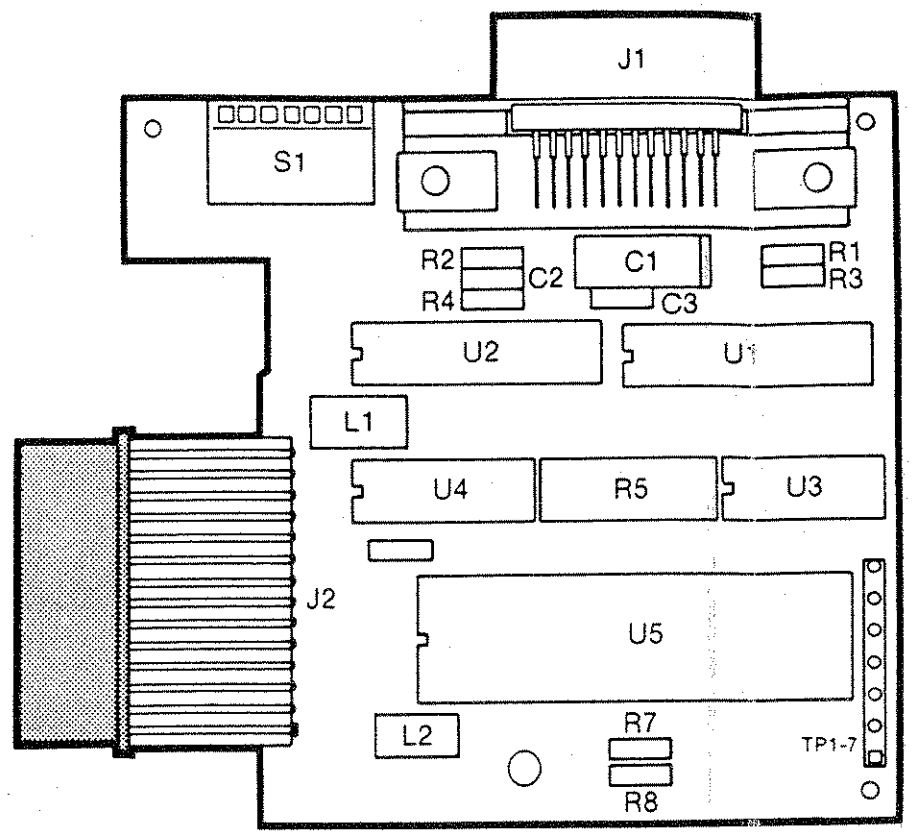


Figure 5-24. A7 Keyboard/Display Logic Assembly Schematic Diagram



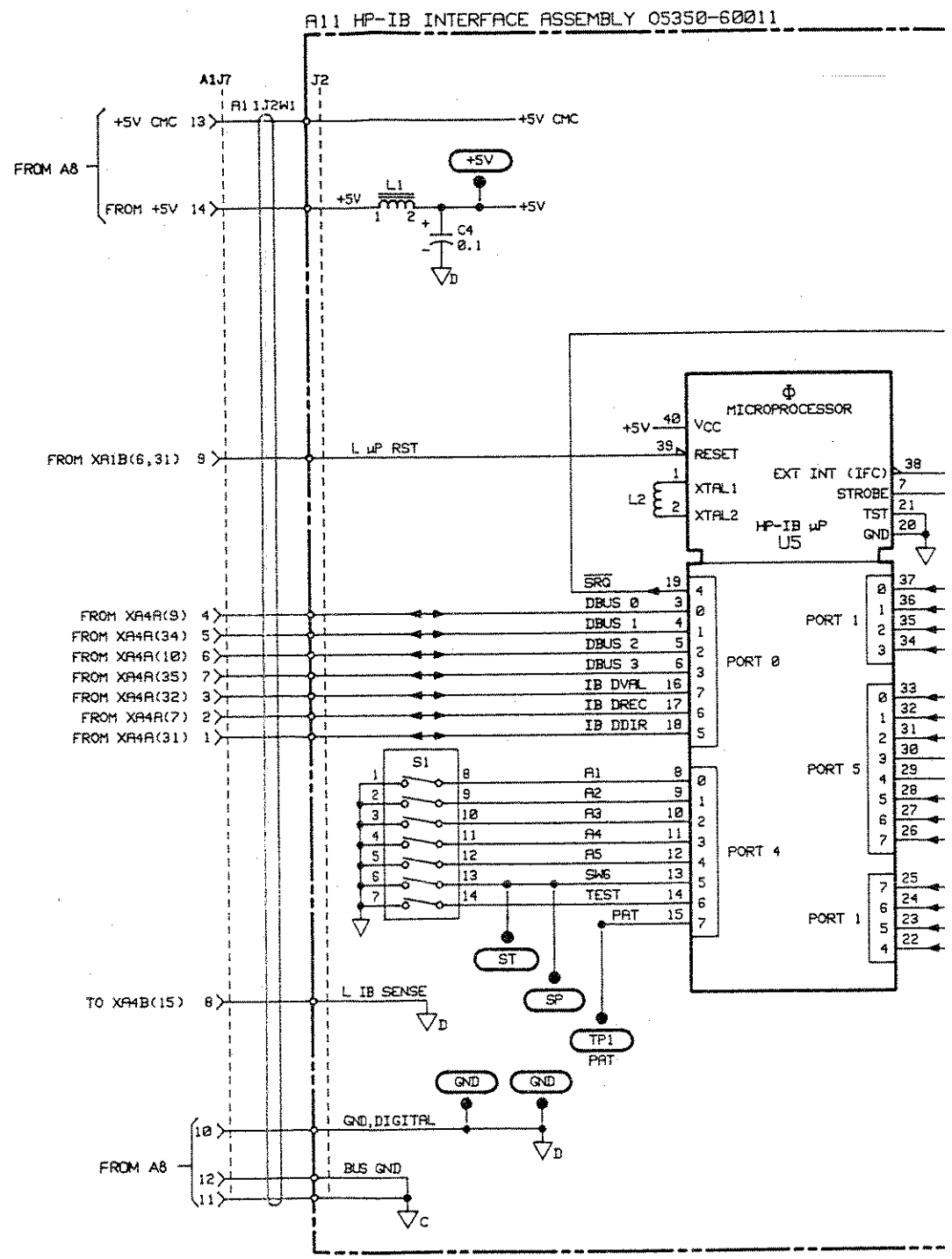
A11 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A11 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN MICROFARADS, INDUCTANCE IN MICROHENRIES.

3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.

4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.



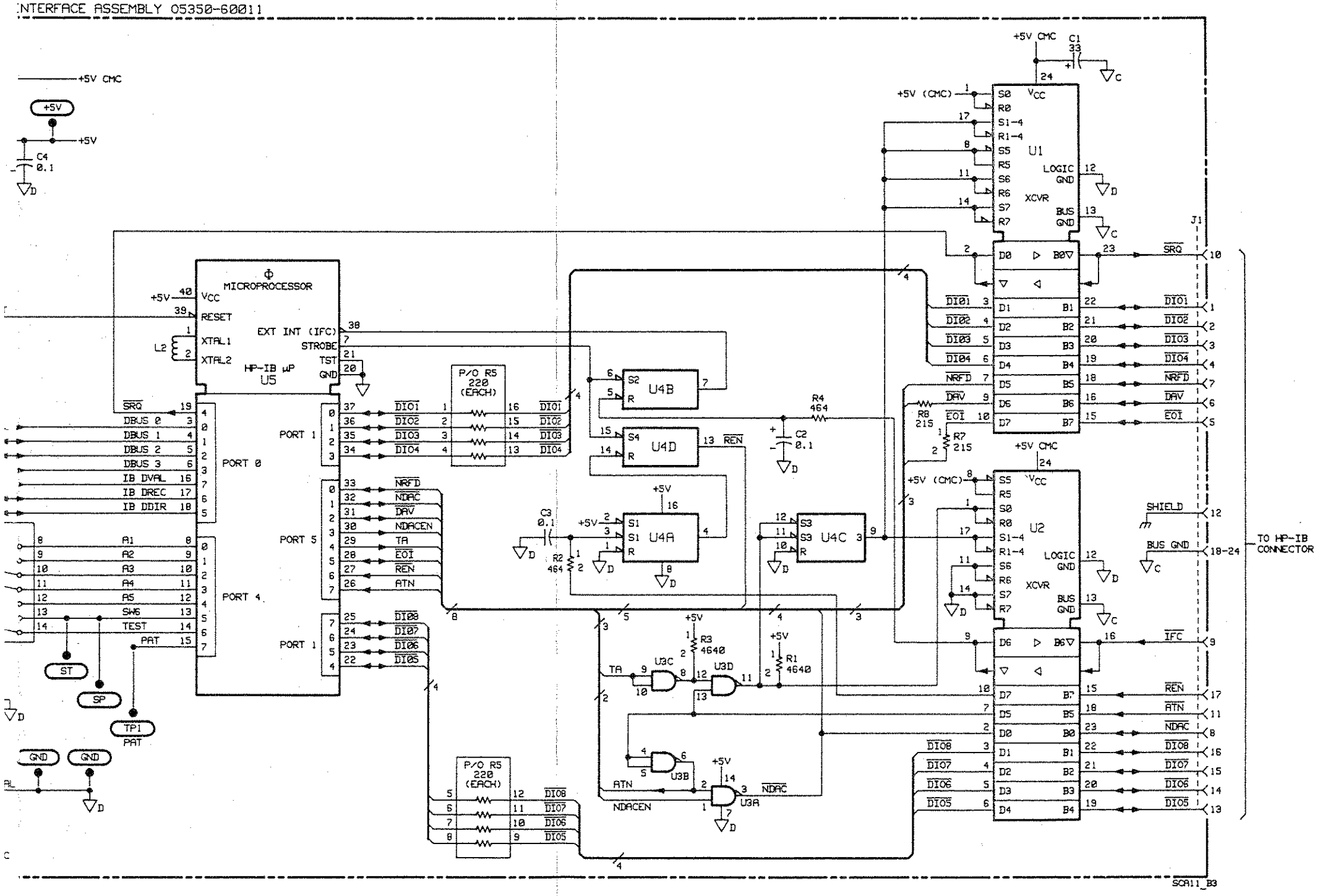


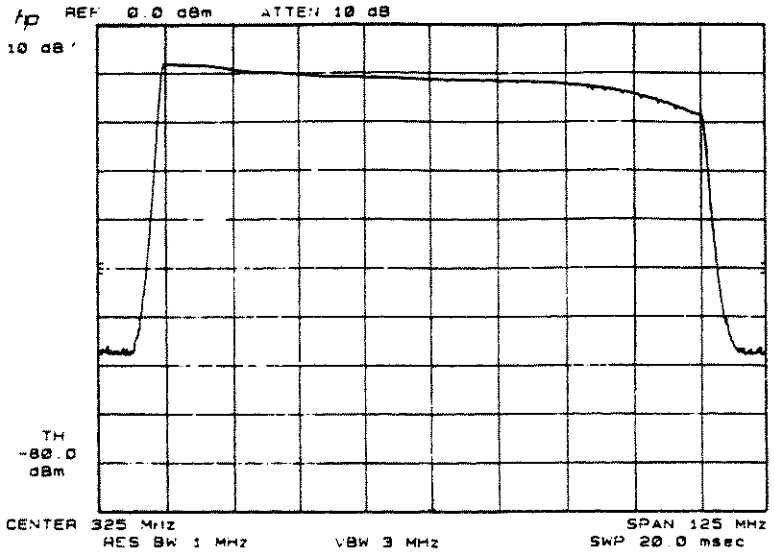
Figure 5-25. A11 HP-IB Interface Assembly Component Locator/Schematic Diagram

WAVEFORM A

TEST POINT:
A12Q2 COLLECTOR,
(USE HP 1124A ACTIVE PROBE WITH 100:1 DIVIDER TIP WITH THE SPECTRUM ANALYZER; SET PROBE TO AC COUPLED, NO OFFSET)

COUNTER SETUP:
INPUT 1, DIAG 52 (LO SWEEP), WAVEFORM SHOWN WAS OBTAINED AFTER 5 OR 6 SWEEPS IN "MAX HOLD" MODE.

COUNTER INPUT: 770 MHZ, –20 DBM

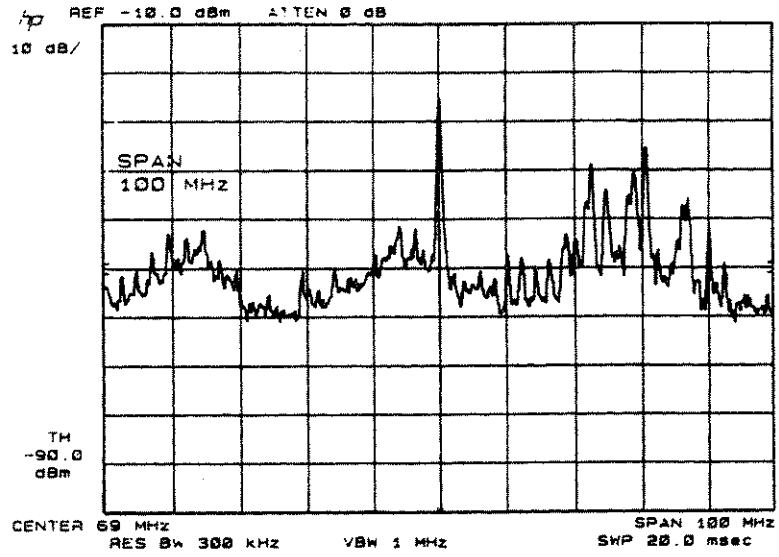


WAVEFORM B

TEST POINT:
A12Q1 EMITTER, (USE HP 1124A ACTIVE PROBE WITH NO DIVIDER TIP TO THE SPECTRUM ANALYZER; SET PROBE TO AC COUPLED, NO OFFSET)

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 1 GHZ

COUNTER INPUT: 1 GHZ, 0 DBM

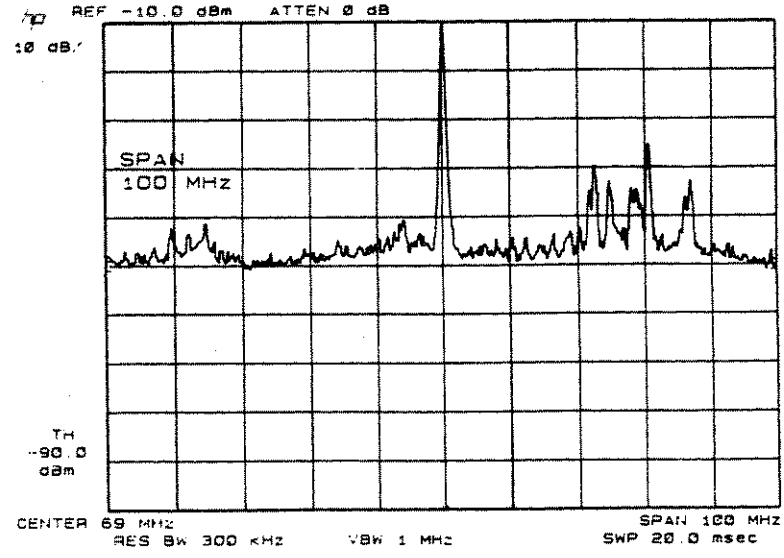


WAVEFORM C

TEST POINT:
A12U1(2), (USE HP 1124A ACTIVE PROBE WITH NO DIVIDER TIP TO THE SPECTRUM ANALYZER; SET PROBE TO AC COUPLED, NO OFFSET)

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 1 GHZ

COUNTER INPUT: 1 GHZ, 0 DBM



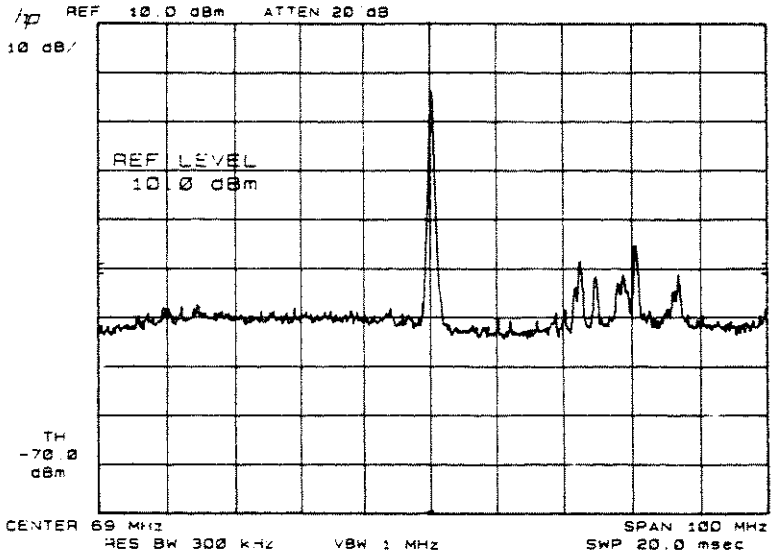
P/O Figure 5-26. A12 Waveforms

WAVEFORM D

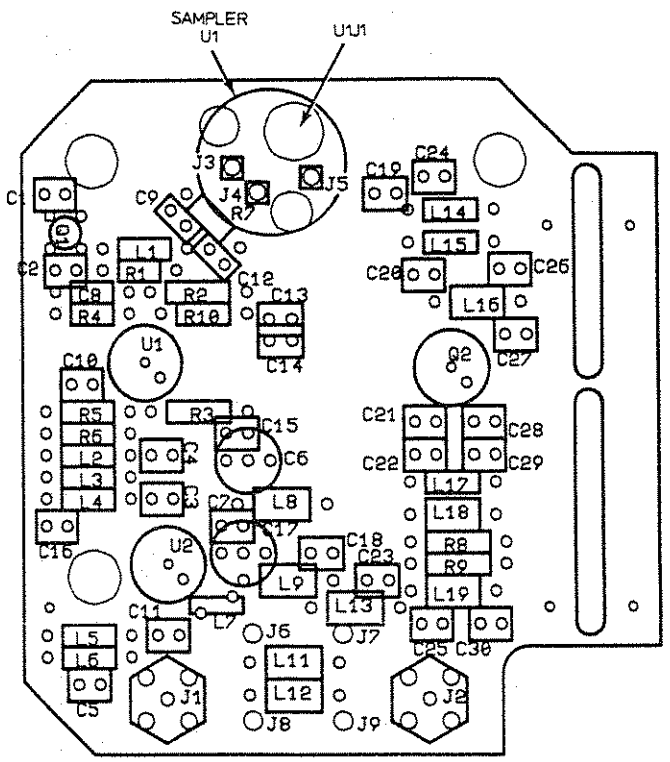
TEST POINT:
A12U2(2), (USE HP 1124A ACTIVE PROBE WITH NO DIVIDER TIP TO THE SPECTRUM ANALYZER; SET PROBE TO AC COUPLED, NO OFFSET)

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 1 GHZ

COUNTER INPUT: 1 GHZ, 0 DBM



P/O Figure 5-26. A12 Waveforms



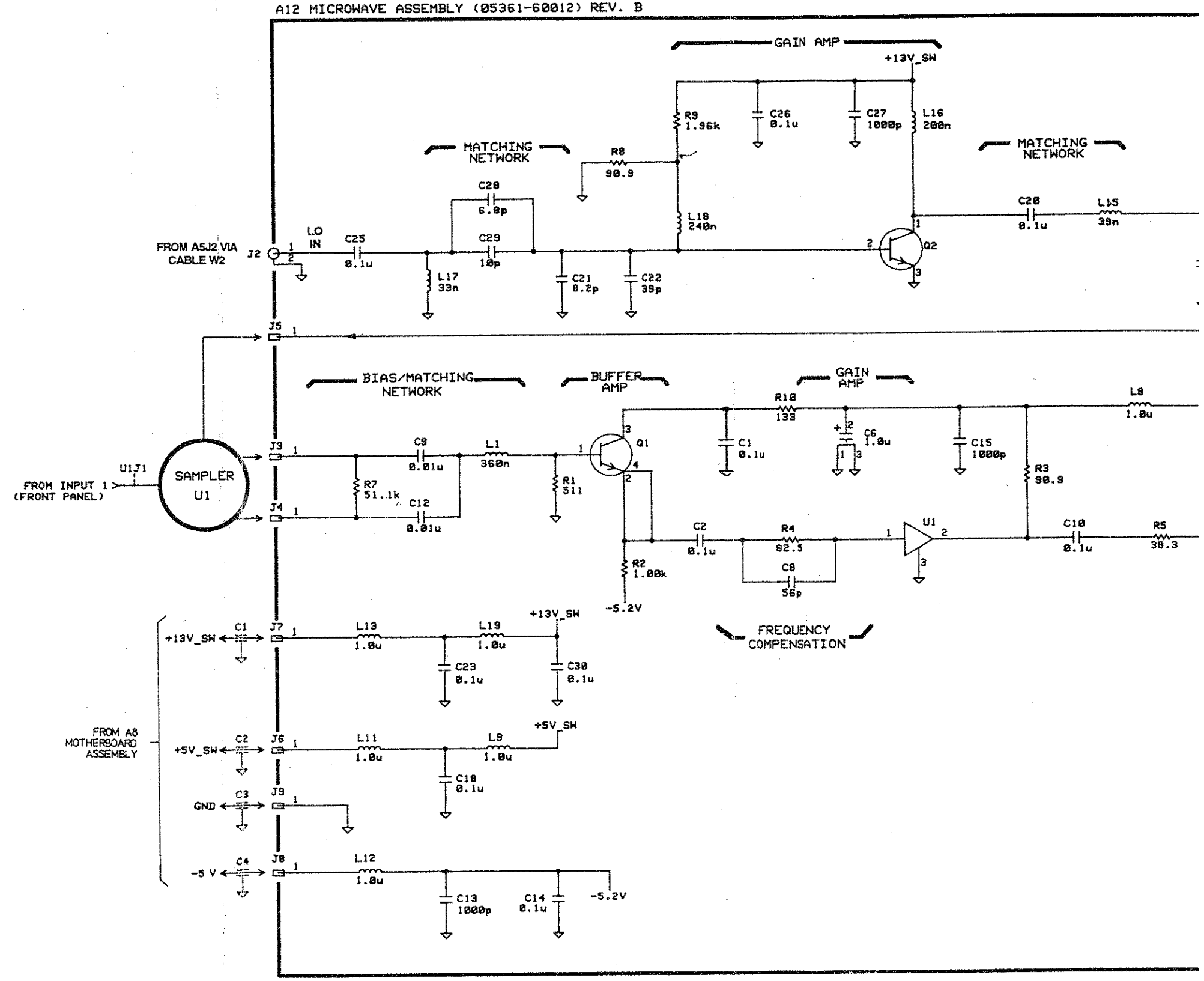
NOTE

This A12 schematic diagram and accompanying information apply only to the 05361-60012 assembly installed in the HP5361A and standard HP5361B. Refer to Figure 5-26A for the 5361B/option 026/040 A12 schematic diagram and component information.

A12 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A12 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN FARADS, INDUCTANCE IN HENRIES.
3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.

A12 MICROWAVE ASSEMBLY (05361-60012) REV. B



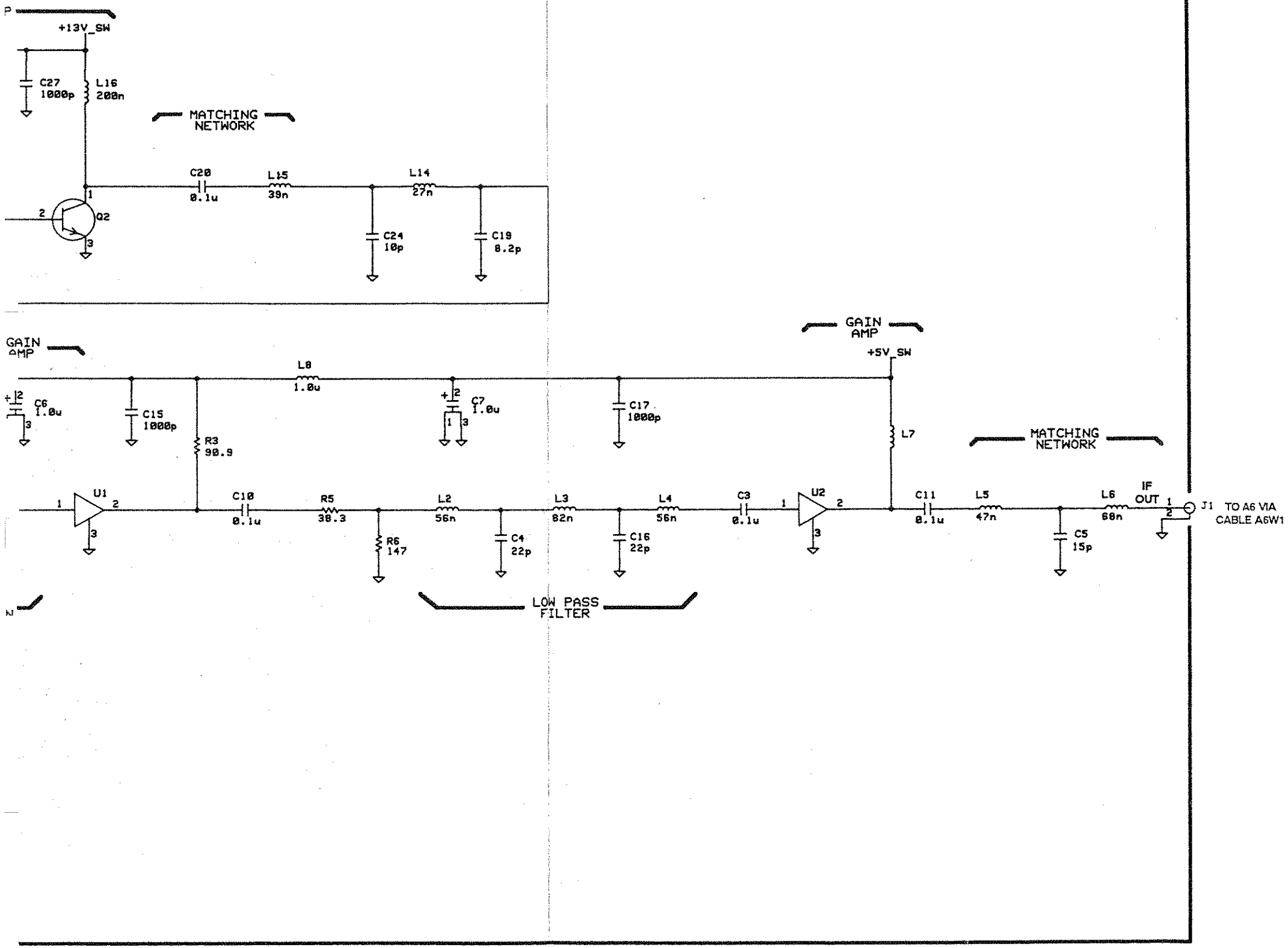


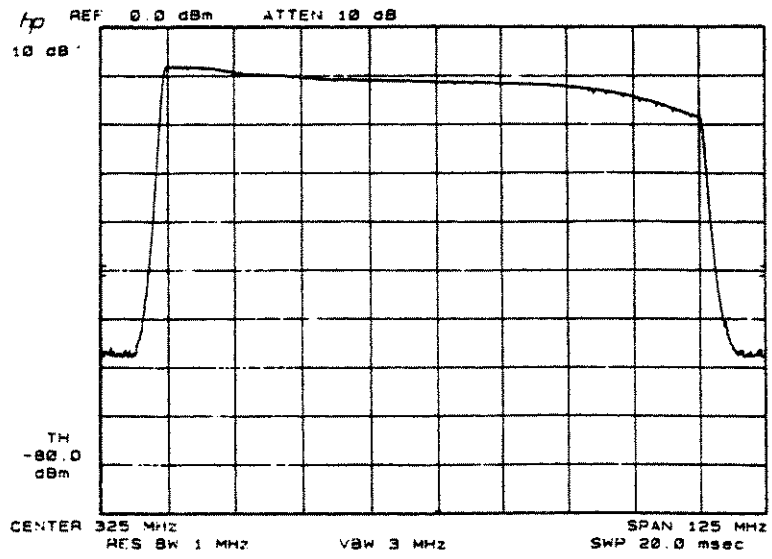
Figure 5-26. A12 Microwave Module (A12 Assembly/U1 Sampler) Component Locator/Schematic Diagram

WAVEFORM A

TEST POINT:
A12Q2 COLLECTOR,
(USE HP 1124A ACTIVE PROBE WITH 100:1 DIVIDER TIP WITH THE SPECTRUM ANALYZER; SET PROBE TO AC COUPLED, NO OFFSET)

COUNTER SETUP:
INPUT 1, DIAG 52 (LO SWEEP), WAVEFORM SHOWN WAS OBTAINED AFTER 5 OR 6 SWEEPS IN "MAX HOLD" MODE.

COUNTER INPUT: 770 MHZ, –20 DBM

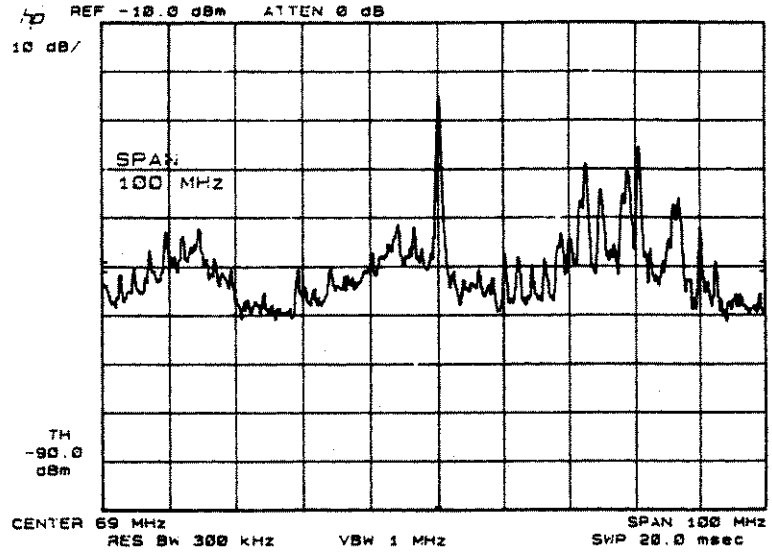


WAVEFORM B

TEST POINT:
A12Q1 EMITTER, (USE HP 1124A ACTIVE PROBE WITH NO DIVIDER TIP TO THE SPECTRUM ANALYZER; SET PROBE TO AC COUPLED, NO OFFSET)

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 1 GHZ

COUNTER INPUT: 1 GHZ, 0 DBM

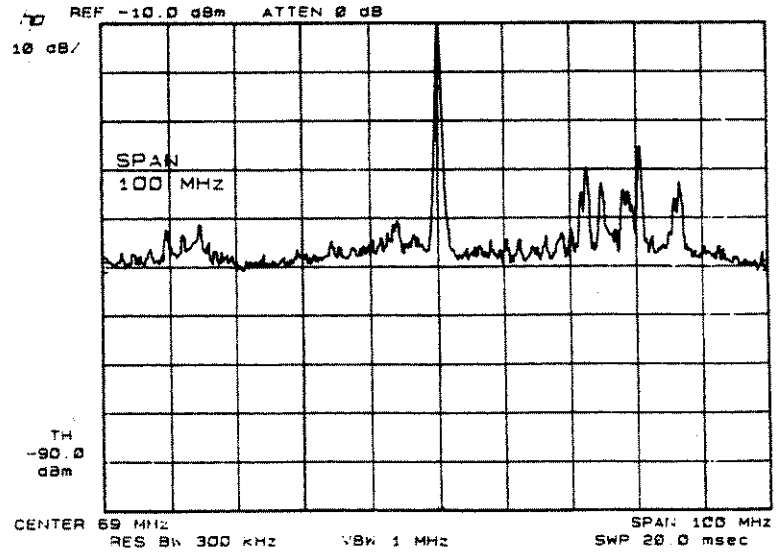


WAVEFORM C

TEST POINT:
A12U1(2), (USE HP 1124A ACTIVE PROBE WITH NO DIVIDER TIP TO THE SPECTRUM ANALYZER; SET PROBE TO AC COUPLED, NO OFFSET)

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 1 GHZ

COUNTER INPUT: 1 GHZ, 0 DBM



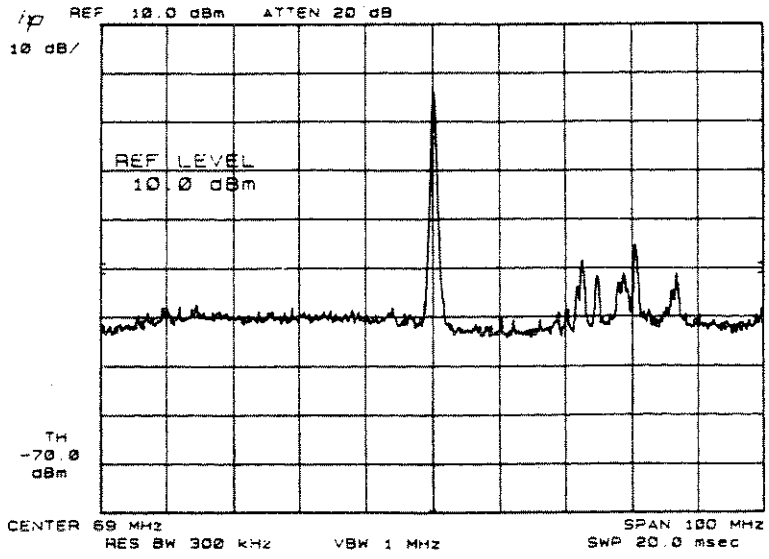
P/O Figure 5-26A. Option 026/040, A12 Waveforms (40 GHz 5361B)

WAVEFORM D

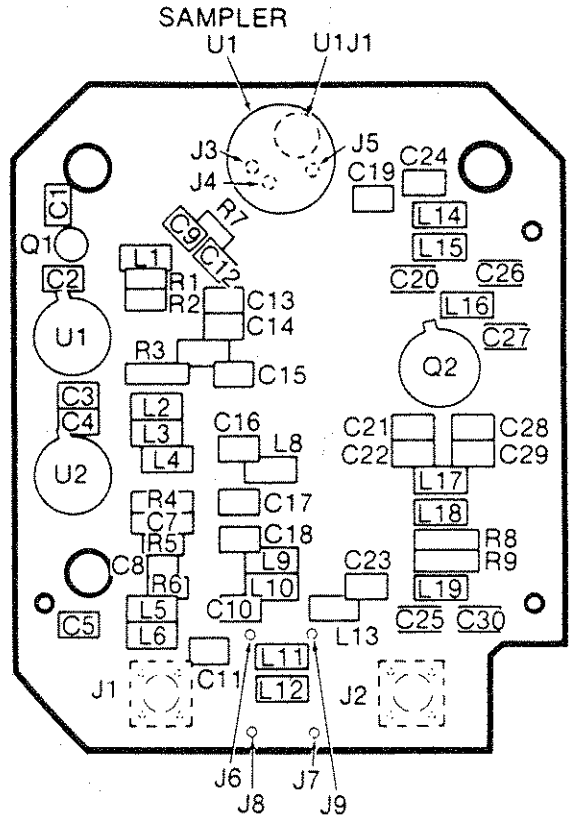
TEST POINT:
A12U2(2), (USE HP 1124A ACTIVE PROBE WITH NO DIVIDER TIP TO THE SPECTRUM ANALYZER; SET PROBE TO AC COUPLED, NO OFFSET)

COUNTER SETUP: INPUT 1, MANUAL MODE, CF = 1 GHZ

COUNTER INPUT: 1 GHZ, 0 DBM



P/O Figure 5-26A. Option 026/040, A12 Waveforms (40 GHz 5361B)

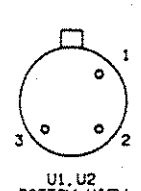


NOTES

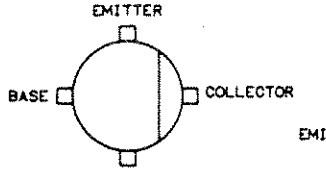
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN MICROFARADS;
   INDUCTANCE IN MICROHENRIES.
3. SAMPLER U1 IS NOT PART OF THE A12 ASSEMBLY. REFER TO REPLACEABLE PARTS LIST IN SECTION VI FOR SAMPLER PART NUMBER.

A8J11
CIRCUIT SIDE OF MOTHERBOARD

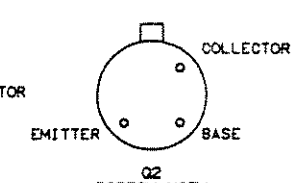
NOT CONNECTED TO MICROWAVE MODULE			TO MICROWAVE MODULE VIA W5
GND, MTHRPLN	6	1	NC
+15V	7	2	+13V SW
-5.2V	8	3	GND, MTHRPLN
-5.2V	9	4	+5V SW
+5V	10	5	-5.2V



U1, U2
BOTTOM VIEW

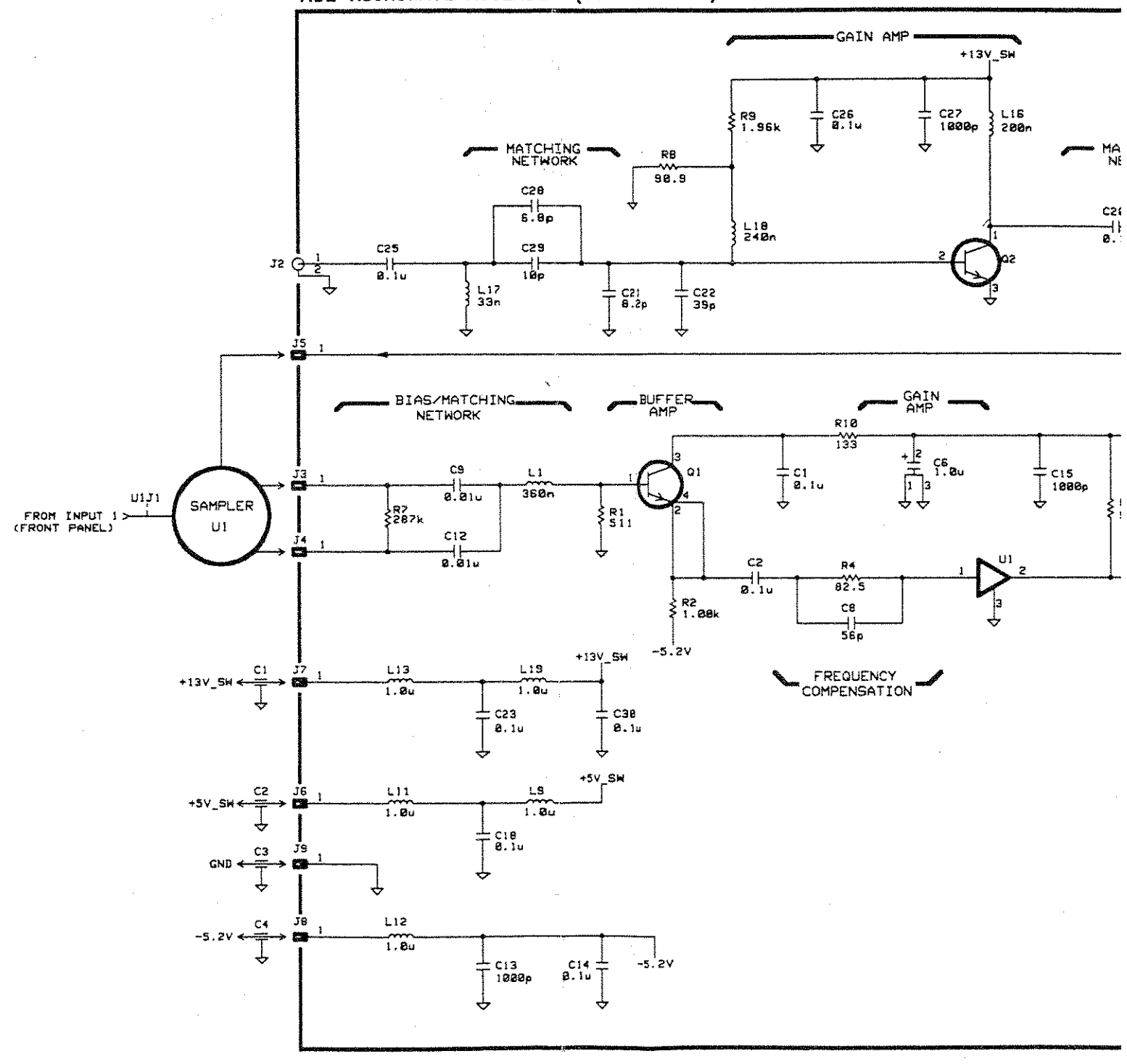


Q1
TOP VIEW



Q2
BOTTOM VIEW

A12 MICROWAVE ASSEMBLY (05361-60013)



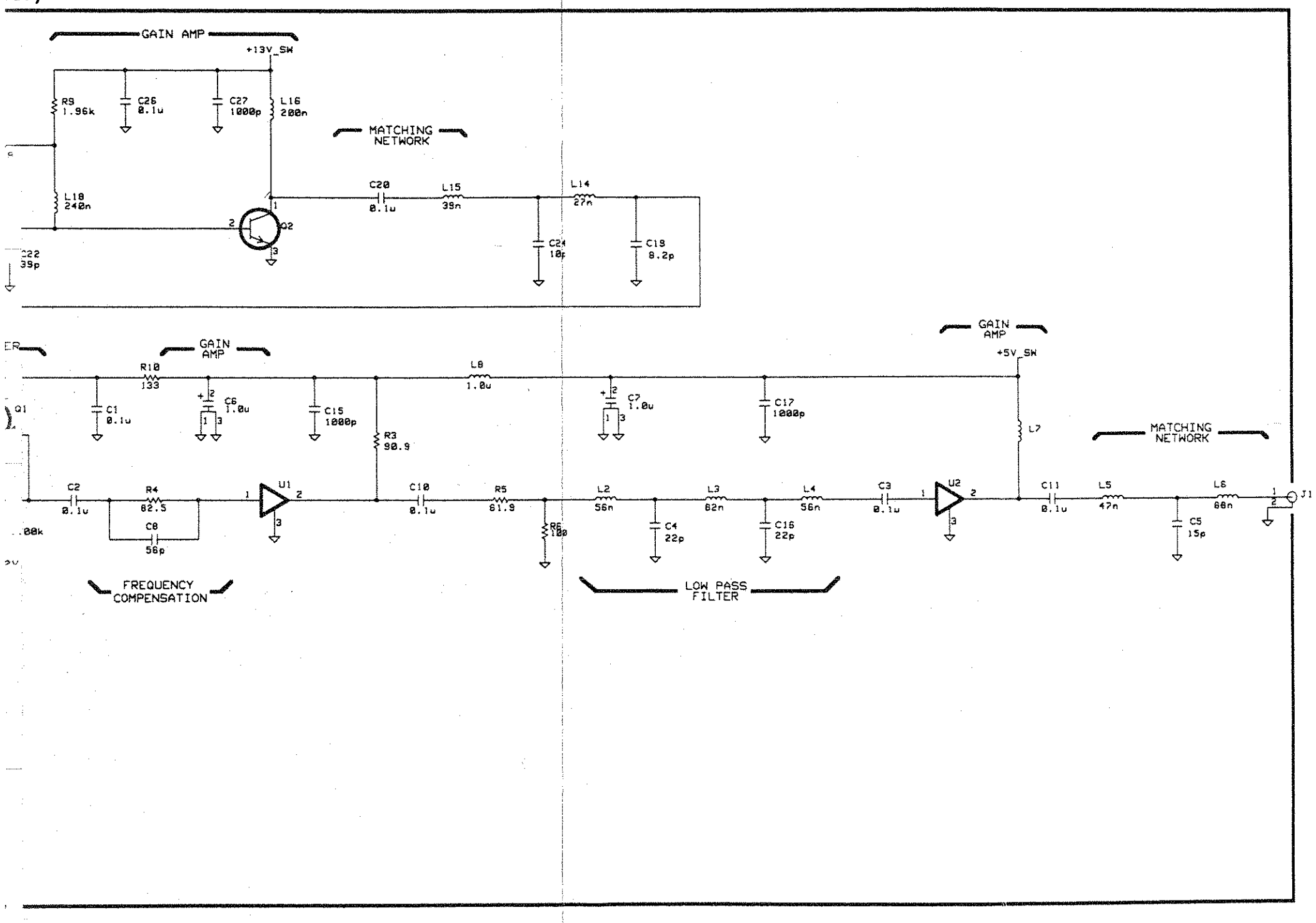


Figure 5-26A. Option 026/040, A12 Microwave Module (A12 Assembly/U1 Sampler) Component Locator/Schematic Diagram

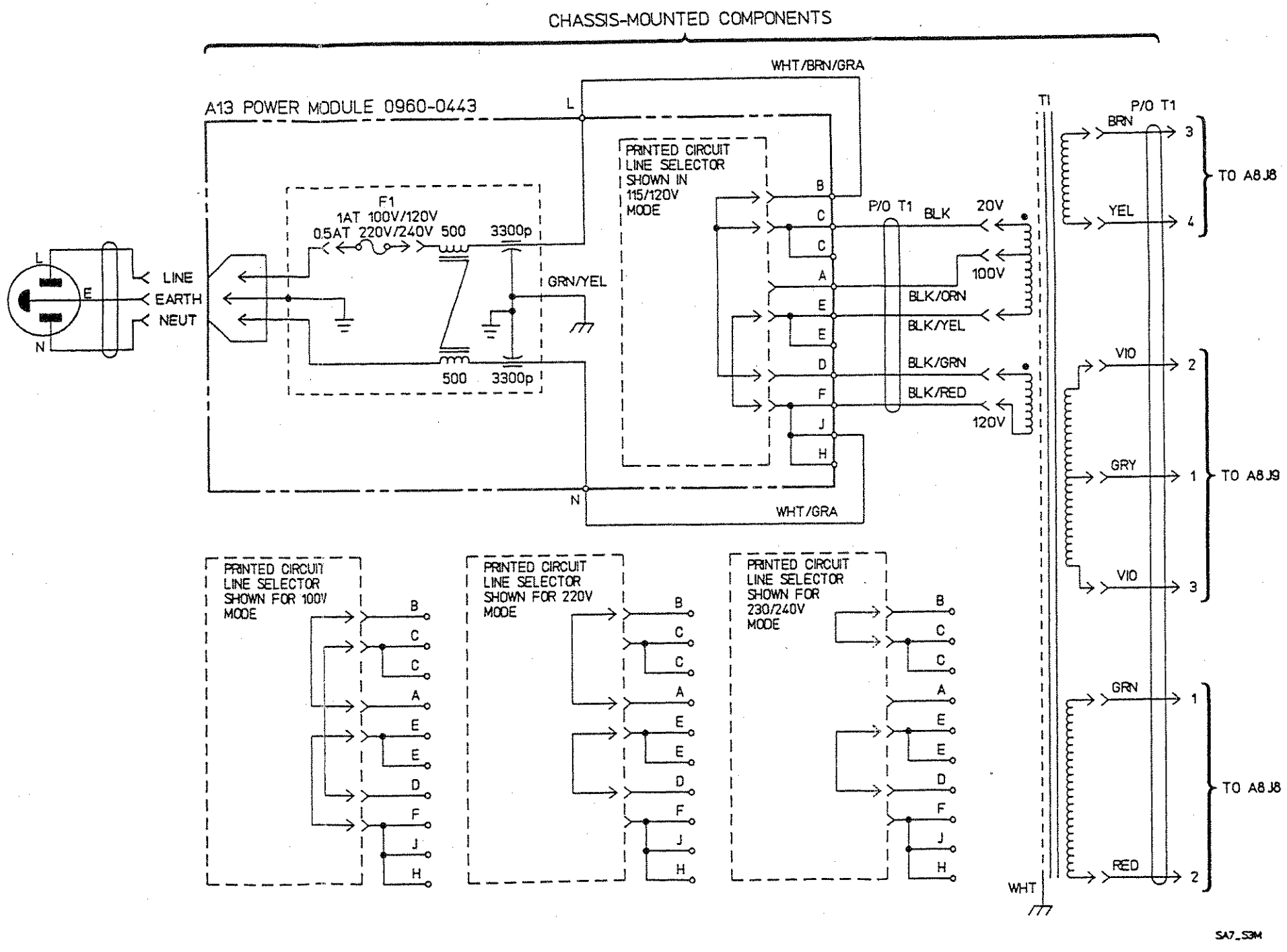


Figure 5-27. A13 Power Input Module and Transformer Assembly Schematic Diagram

Figure 5-27.
A13 POWER INPUT MODULE AND
TRANSFORMER ASSEMBLY
SCHEMATIC DIAGRAM

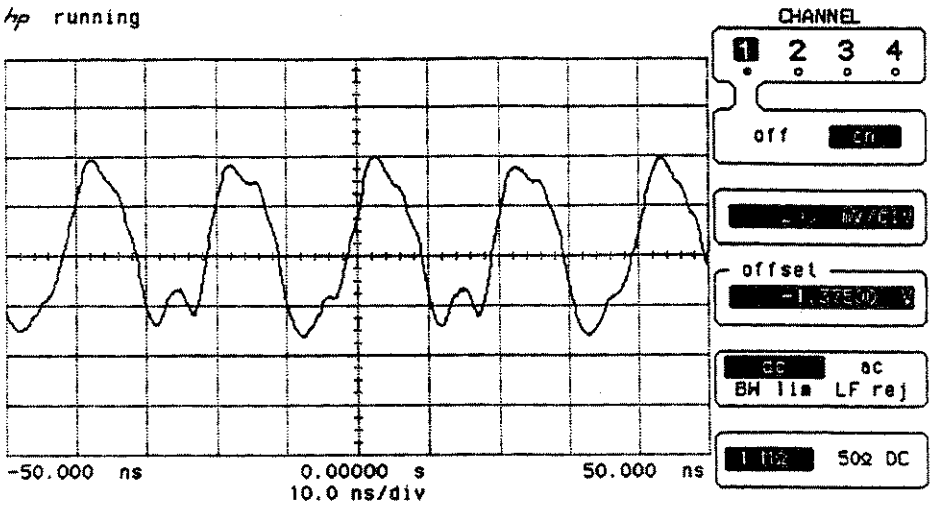
(See Page 5-233)

WAVEFORM A

TEST POINT: A14U32(4), +IF_NEW

COUNTER SETUP: INPUT 1, AUTO MODE, CW MODE

COUNTER INPUT: 1 GHZ, 10 DBM SINE WAVE

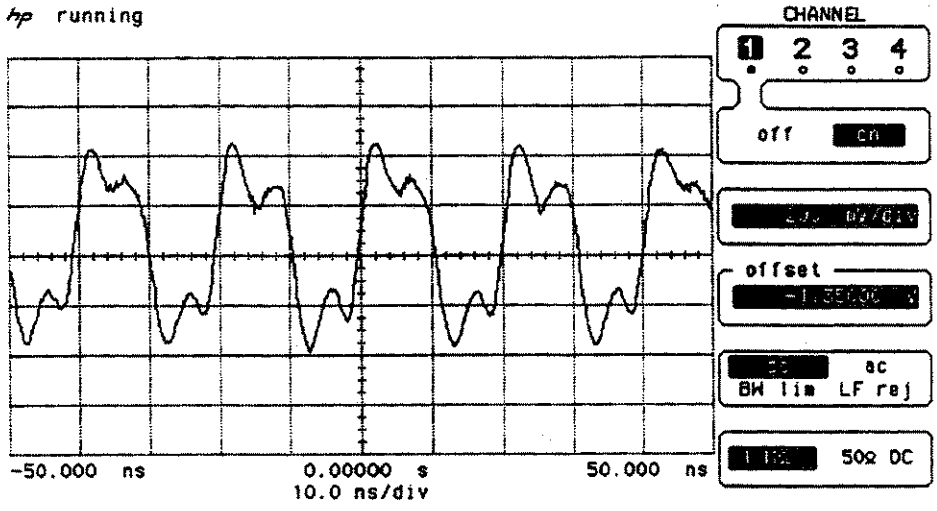


WAVEFORM B

TEST POINT: A14U32(5), -IF_NEW

COUNTER SETUP: INPUT 1, AUTO MODE, CW MODE

COUNTER INPUT: 1 GHZ, –10 DBM SINE WAVE

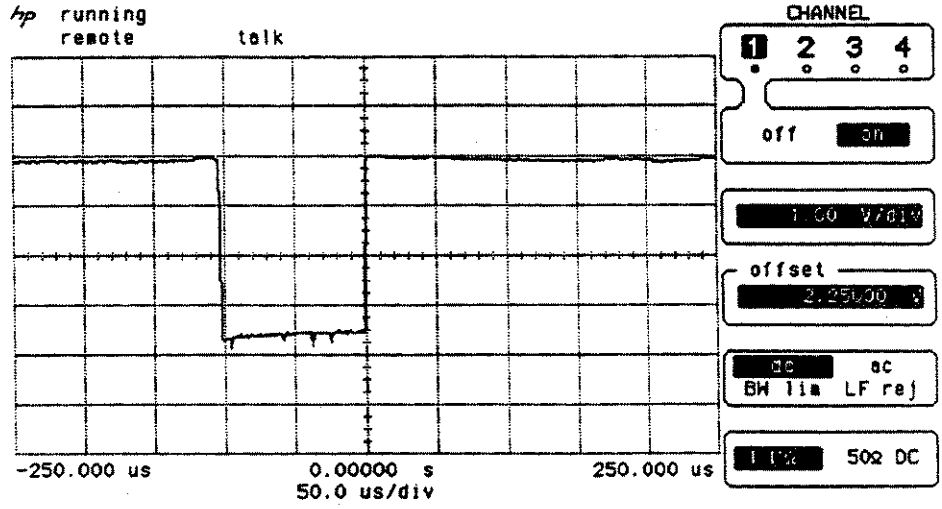


WAVEFORM C

TEST POINT: A14U28(2), L_HOLD_OFF

COUNTER SETUP: INPUT 1, AUTO MODE, CW MODE

COUNTER INPUT: 1 GHZ, –10 DBM SINE WAVE



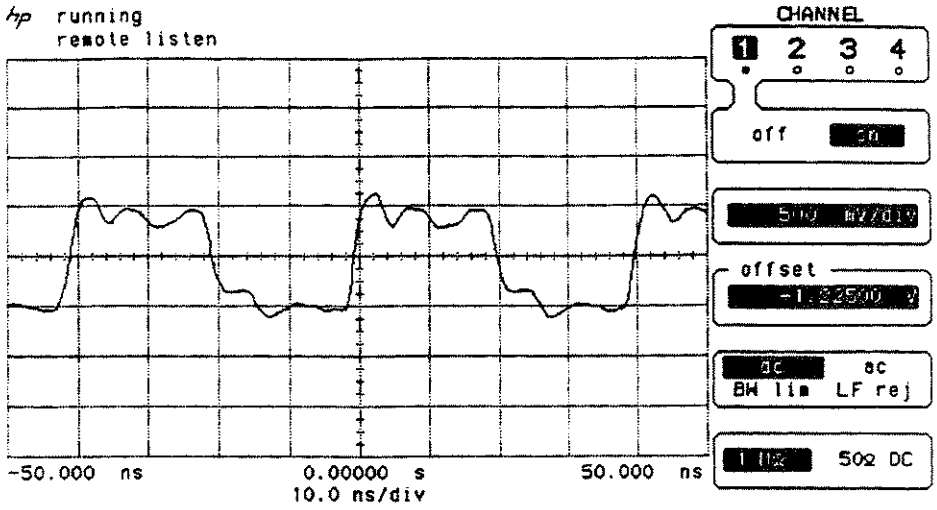
P/O Figure 5-28. A14 Waveforms

WAVEFORM D

TEST POINT: A14U33(2), EVENTS

COUNTER SETUP: INPUT 1, AUTO MODE, CW MODE

COUNTER INPUT: 1 GHZ, 10 DBM SINE WAVE

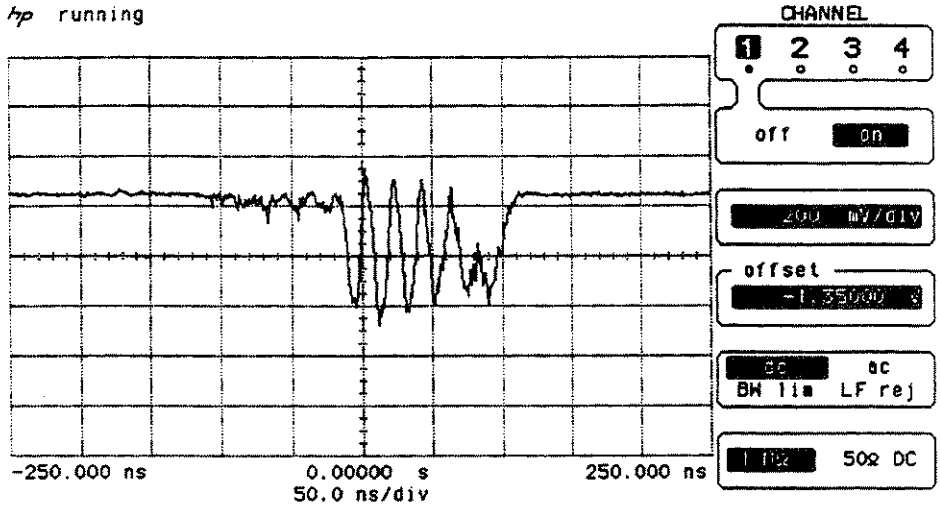


WAVEFORM E

TEST POINT: A14U32(4), +IF_NEW

COUNTER SETUP: INPUT 1, AUTO MODE, PULSED MODE

COUNTER INPUT: 1 GHZ, -10 DBM PULSED SIGNAL

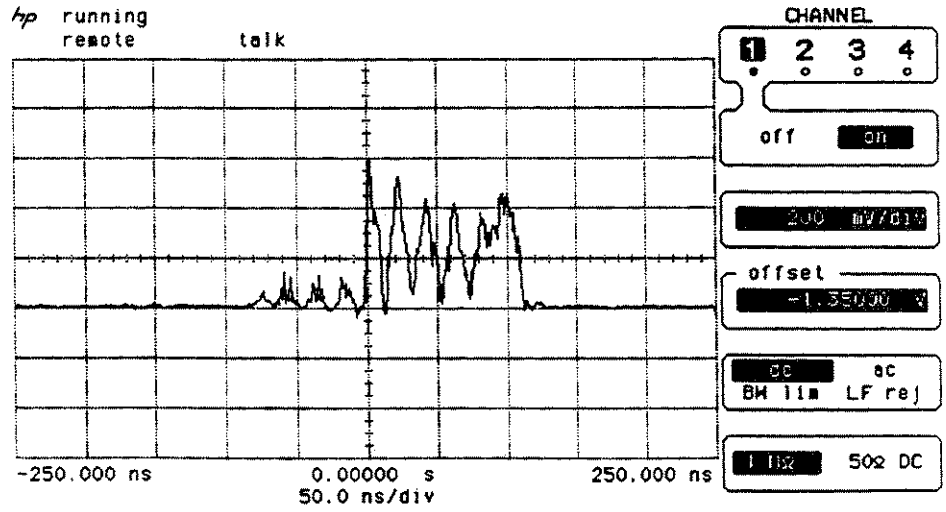


WAVEFORM F

TEST POINT: A14U32(5), -IF_NEW

COUNTER SETUP: INPUT 1, AUTO MODE, PULSED MODE

COUNTER INPUT: 1 GHZ, -10 DBM PULSED SIGNAL



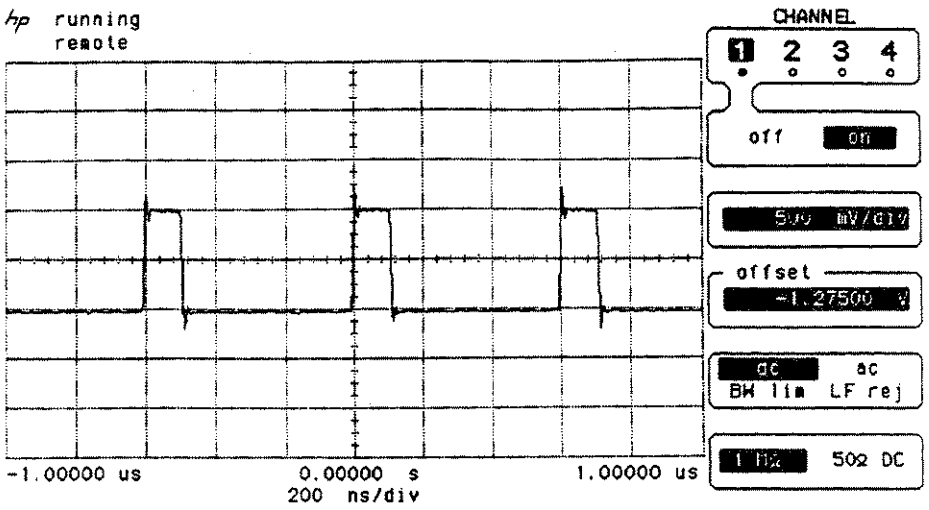
P/O Figure 5-28. A14 Waveforms

WAVEFORM G

TEST POINT: A14U31(4), H_ENV_IF

COUNTER SETUP: INPUT 1, AUTO MODE, PULSED MODE

COUNTER INPUT: 1 GHZ, –10 DBM PULSED SIGNAL

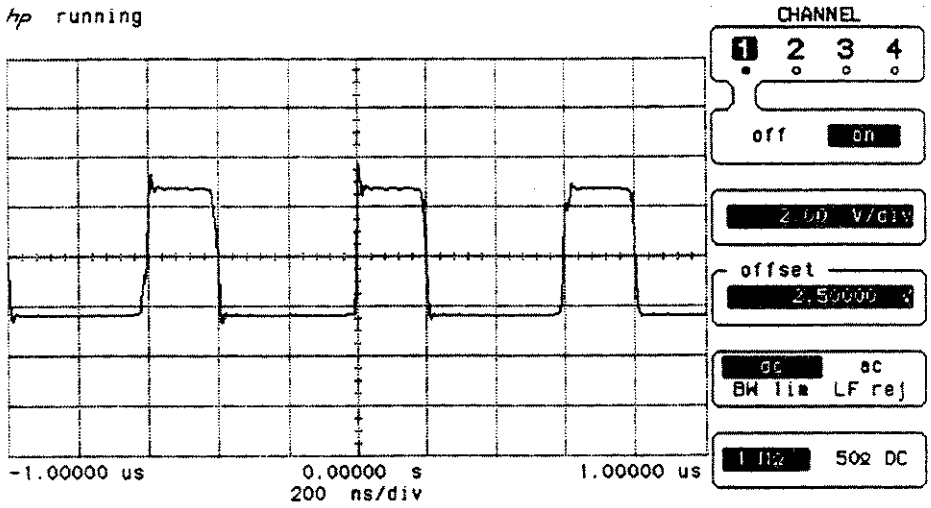


WAVEFORM H

TEST POINT: A14U11(1), L_IF_INBAND

COUNTER SETUP: INPUT 1, AUTO MODE, PULSED MODE

COUNTER INPUT: 1 GHZ, –10 DBM PULSED SIGNAL

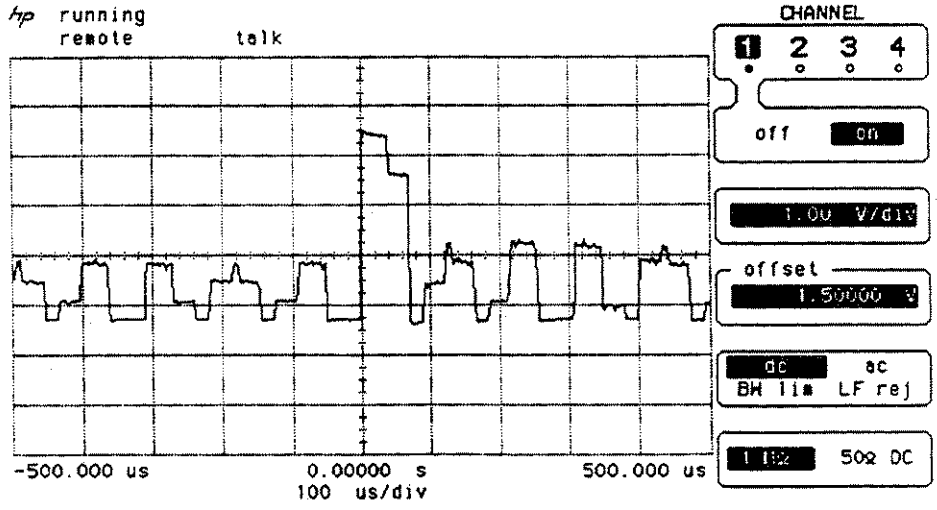


WAVEFORM I

TEST POINT: A14U28(1), H_GATE

COUNTER SETUP: INPUT 1, AUTO MODE, PULSED MODE

COUNTER INPUT: 1 GHZ, –10 DBM PULSED SIGNAL



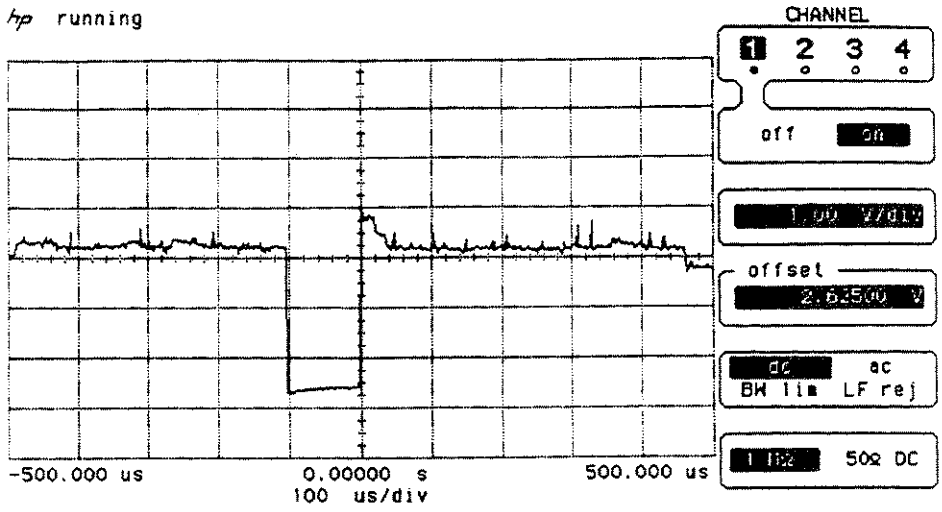
P/O Figure 5-28. A14 Waveforms

WAVEFORM J

TEST POINT: A14U28(2), L_HOLD_OFF

COUNTER SETUP: INPUT 1, AUTO MODE, PULSED MODE

COUNTER INPUT: 1 GHZ, –10 DBM PULSED SIGNAL

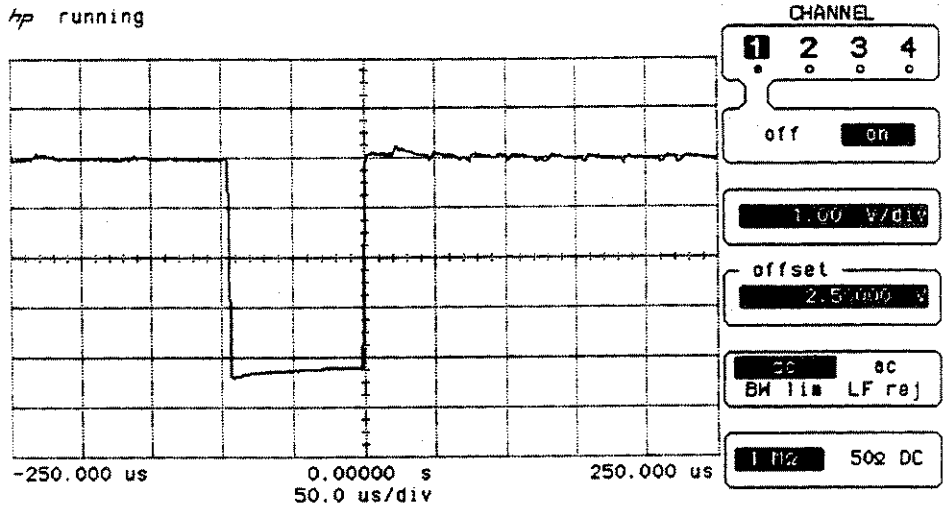


WAVEFORM K

TEST POINT: A14U30(5), L_INP_RST

COUNTER SETUP: INPUT 1, AUTO MODE, PULSED MODE

COUNTER INPUT: 1 GHZ, –10 DBM PULSED SIGNAL

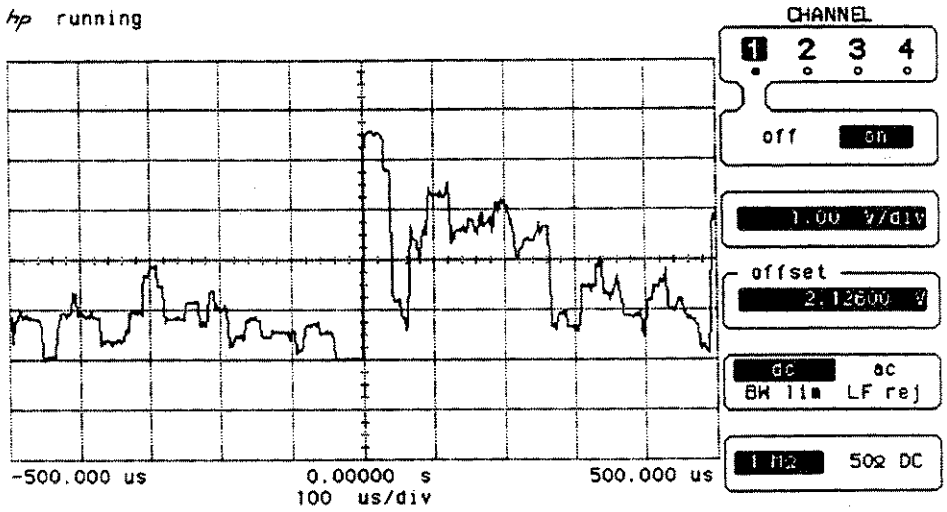


WAVEFORM L

TEST POINT: A14U3(19), MRC_REG0

COUNTER SETUP: INPUT 1, AUTO MODE, PULSED MODE

COUNTER INPUT: 1 GHZ, –10 DBM PULSED SIGNAL



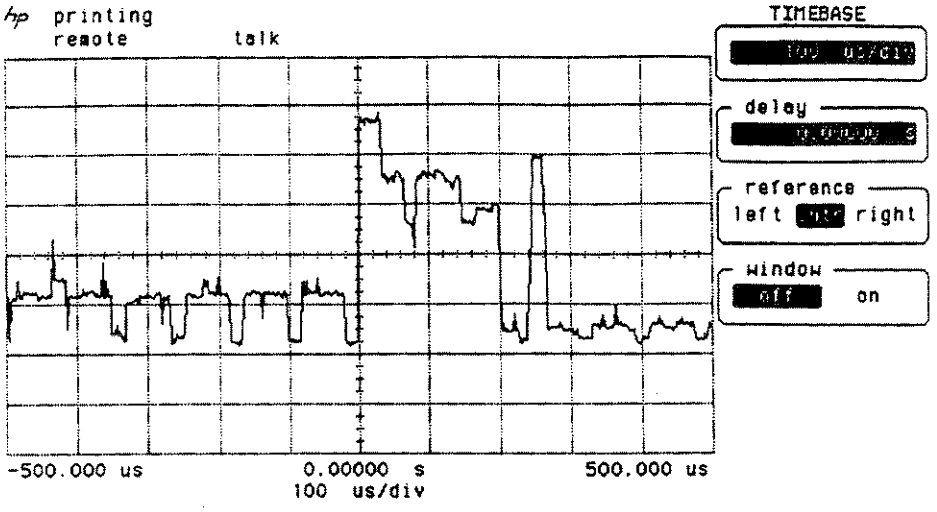
P/O Figure 5-28. A14 Waveforms

WAVEFORM M

TEST POINT: A14U3(20), MRC_REG1

COUNTER SETUP: INPUT 1, AUTO MODE, PULSED MODE

COUNTER INPUT: 1 GHZ, –10 DBM PULSED SIGNAL

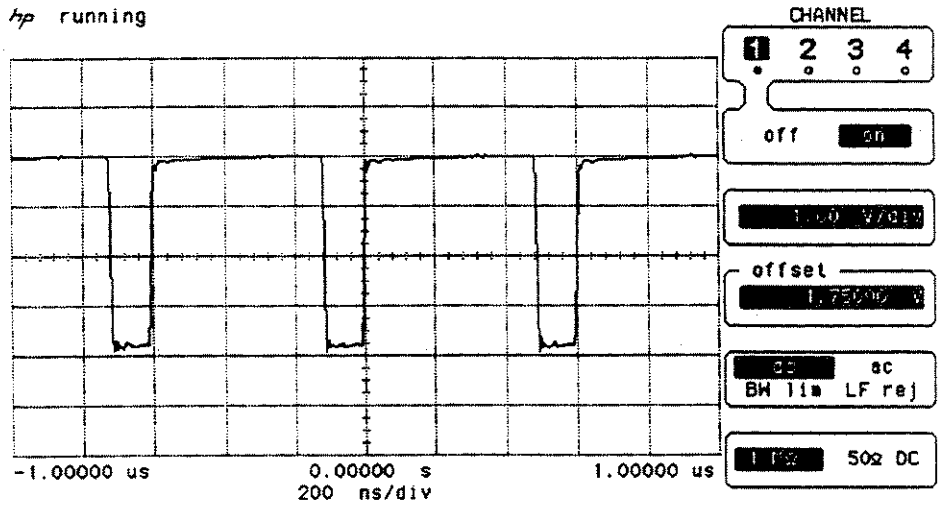


WAVEFORM N

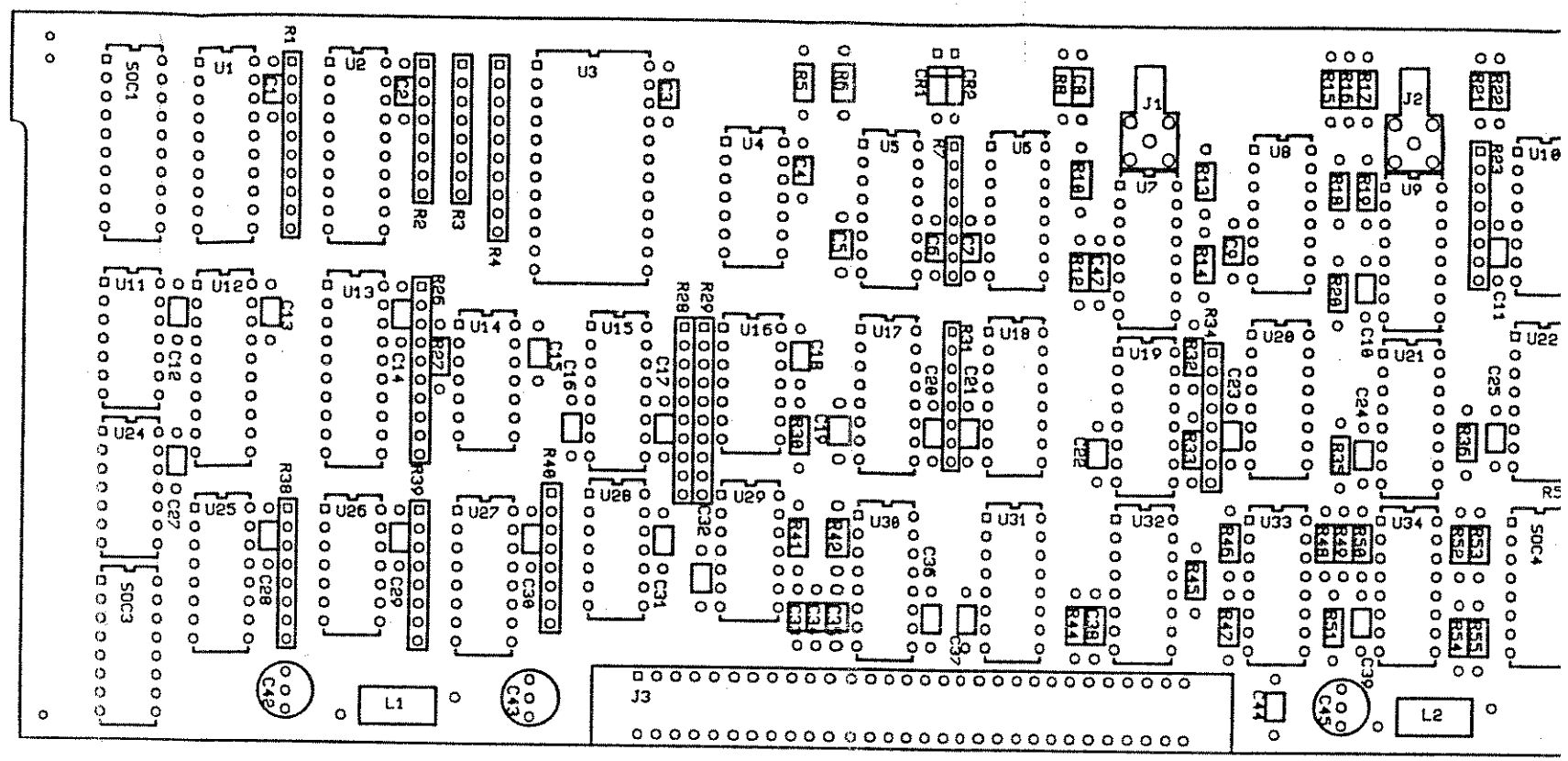
TEST POINT: A14U16(1), ENVELOPE_OUT

COUNTER SETUP: INPUT 1, AUTO MODE, PULSED MODE

COUNTER INPUT: 1 GHZ, –10 DBM PULSED SIGNAL



P/O Figure 5-28. A14 Waveforms



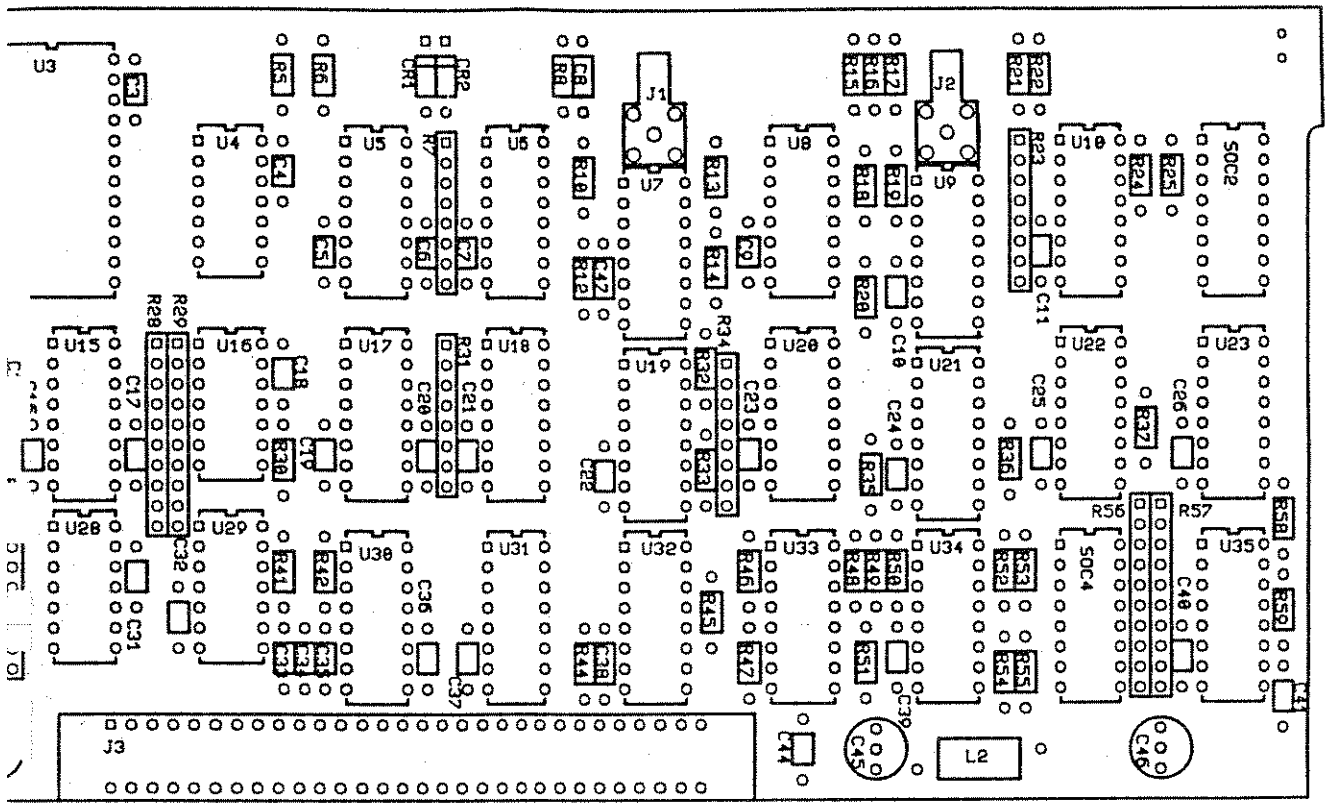
A14 SCHEMATIC DIAGRAM NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD A14 ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN FARADS, INDUCTANCE IN HENRIES.

3. ASTERISK (*) INDICATES FACTORY SELECTED COMPONENT. AVERAGE VALUE SHOWN.

4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.



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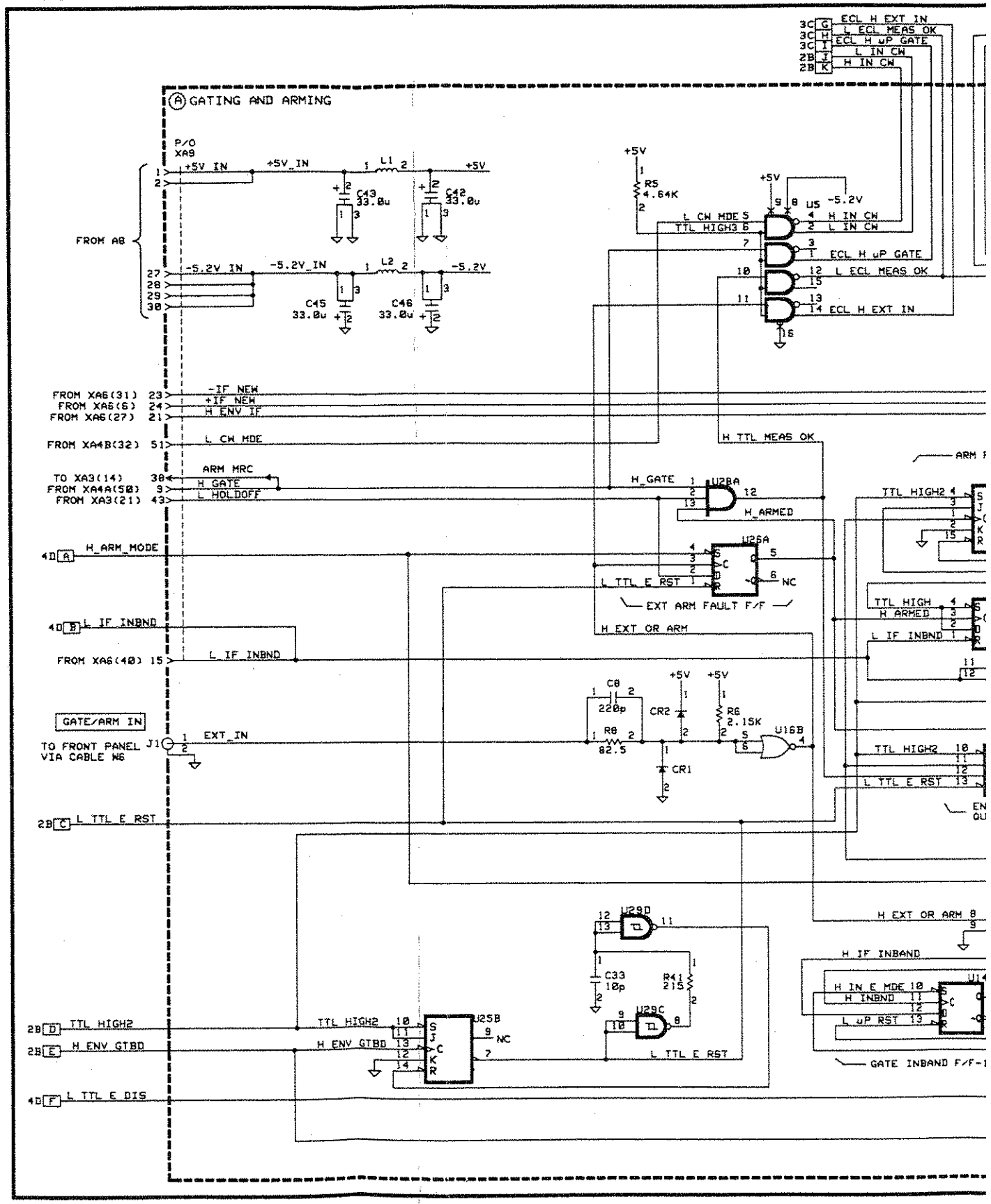
A14 GATE BOARD ASSEMBLY (05361-60009) REV.B (SHEET 1 OF 4)



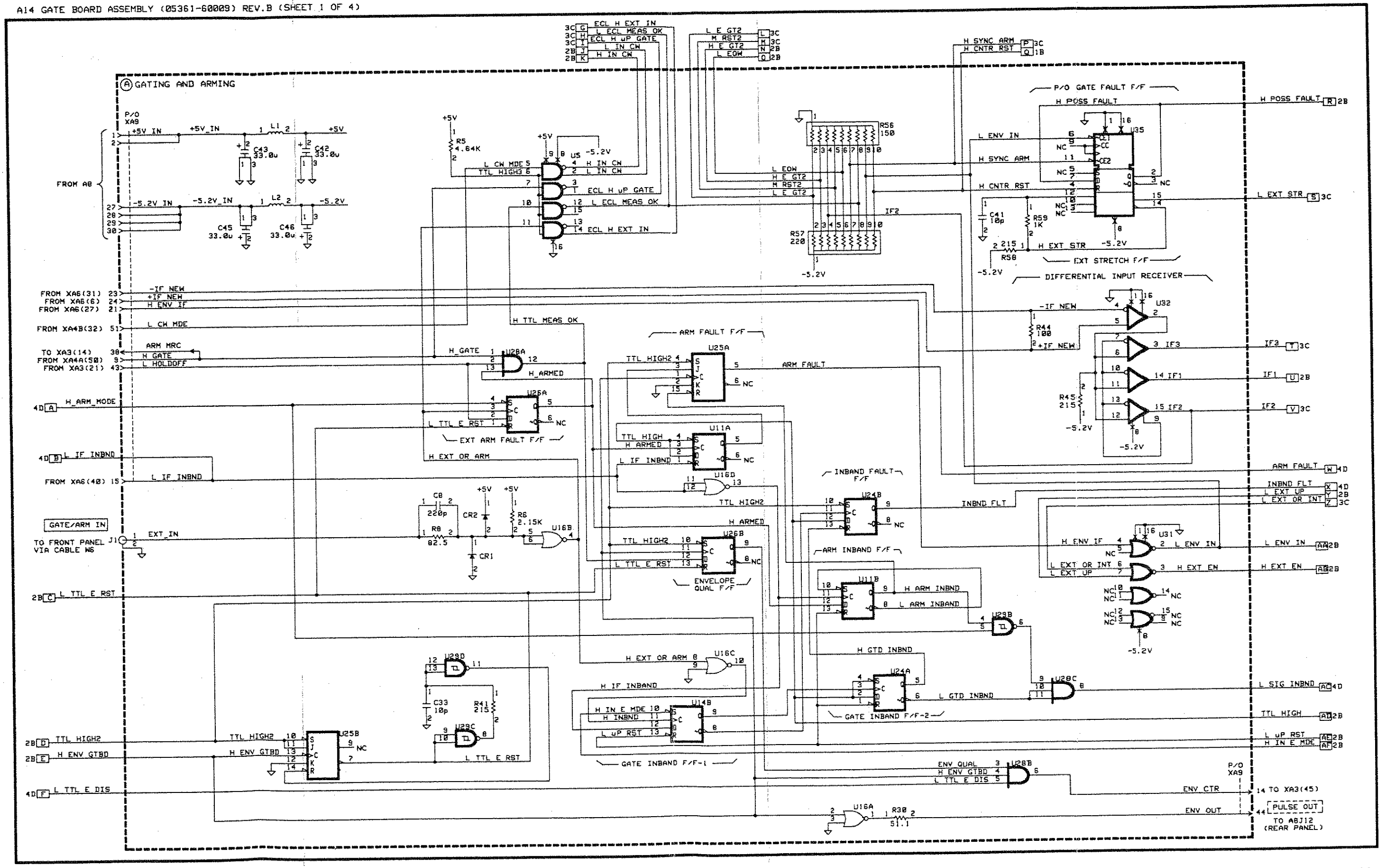
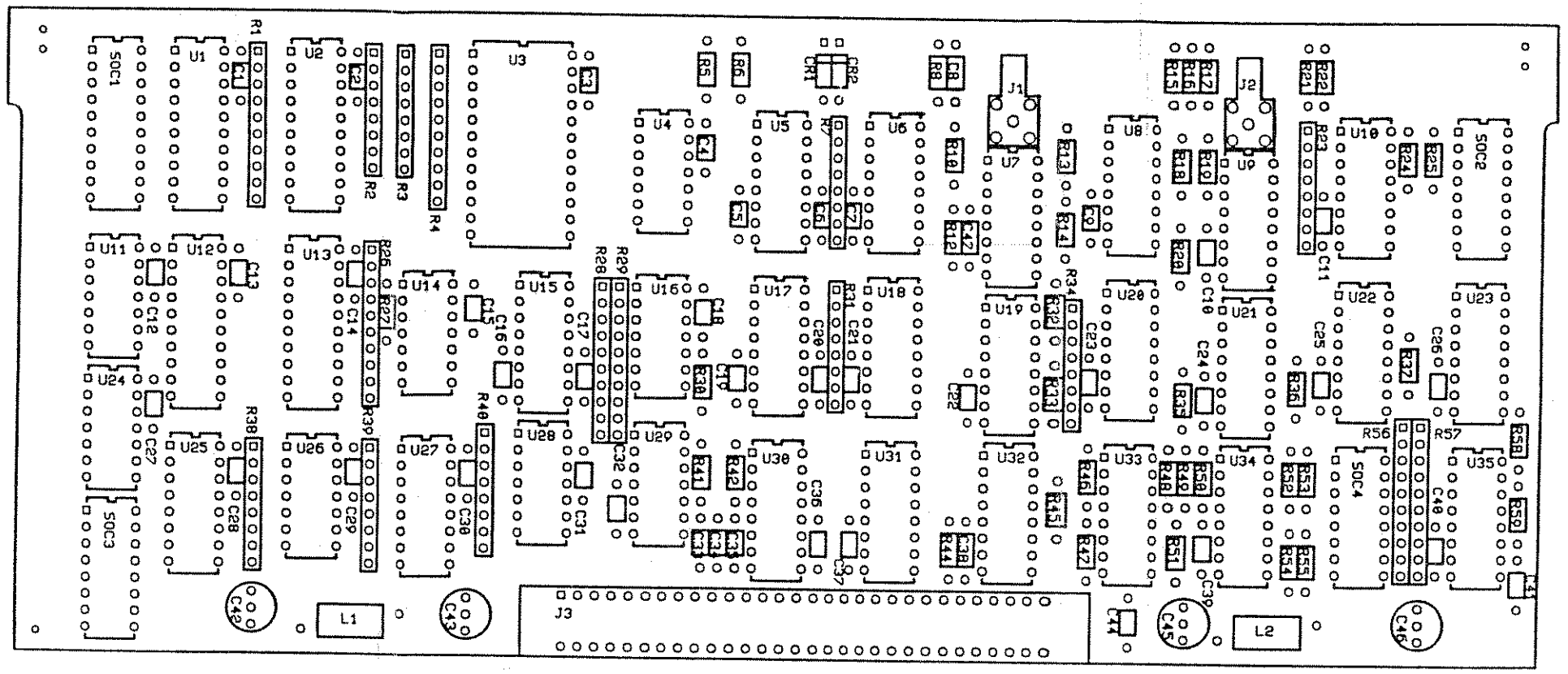


Figure 5-28. A14 Gate Board Assembly Component Locator/Schematic Diagram (Sheet 1 of 4)



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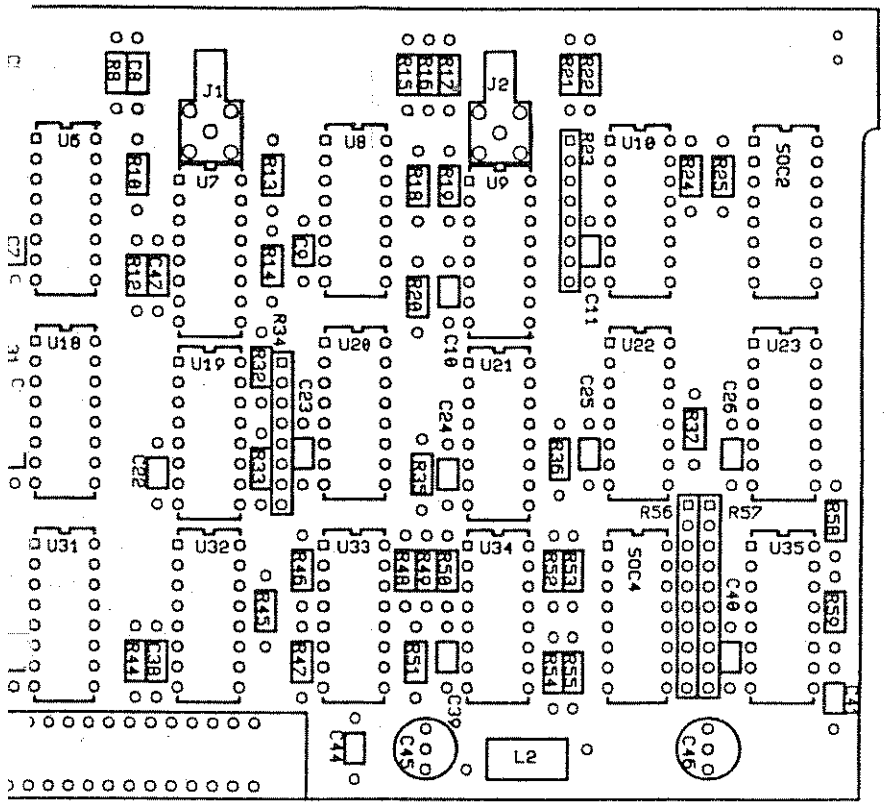
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.



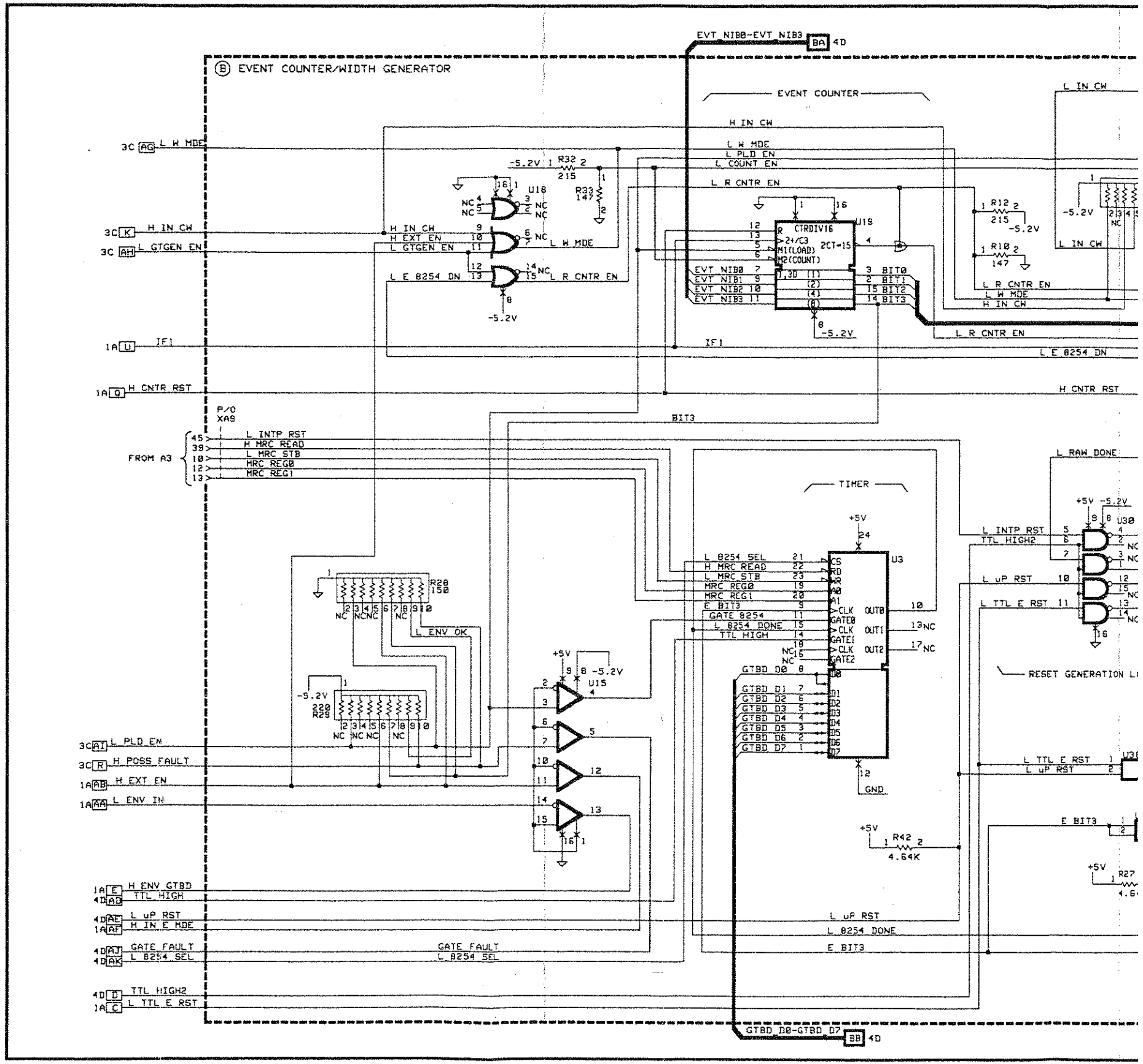
WITHIN THIS ASSEMBLY
4 ASSEMBLY NUMBER TO
E DESCRIPTION.

CATED: RESISTANCE IN
FARADS, INDUCTANCE IN

NCTORY SELECTED COM-
HOWN.

NAL INDICATES A NEGA-

A14 GATE BOARD ASSEMBLY (05361-60009) REV.B (SHEET 2 OF 4)



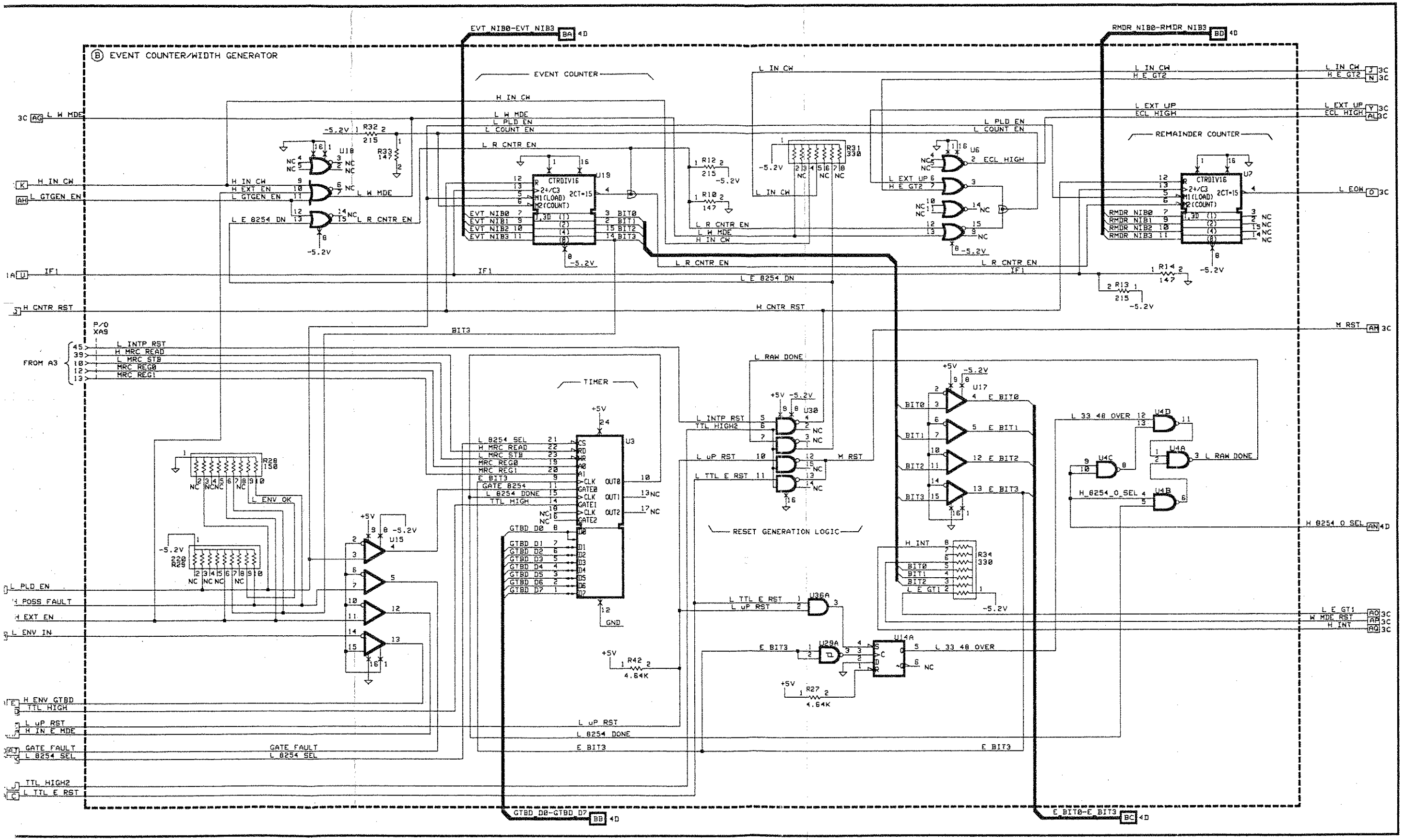


Figure 5-28. A14 Gate Board Assembly Component Locator/Schematic Diagram (Sheet 2 of 4)

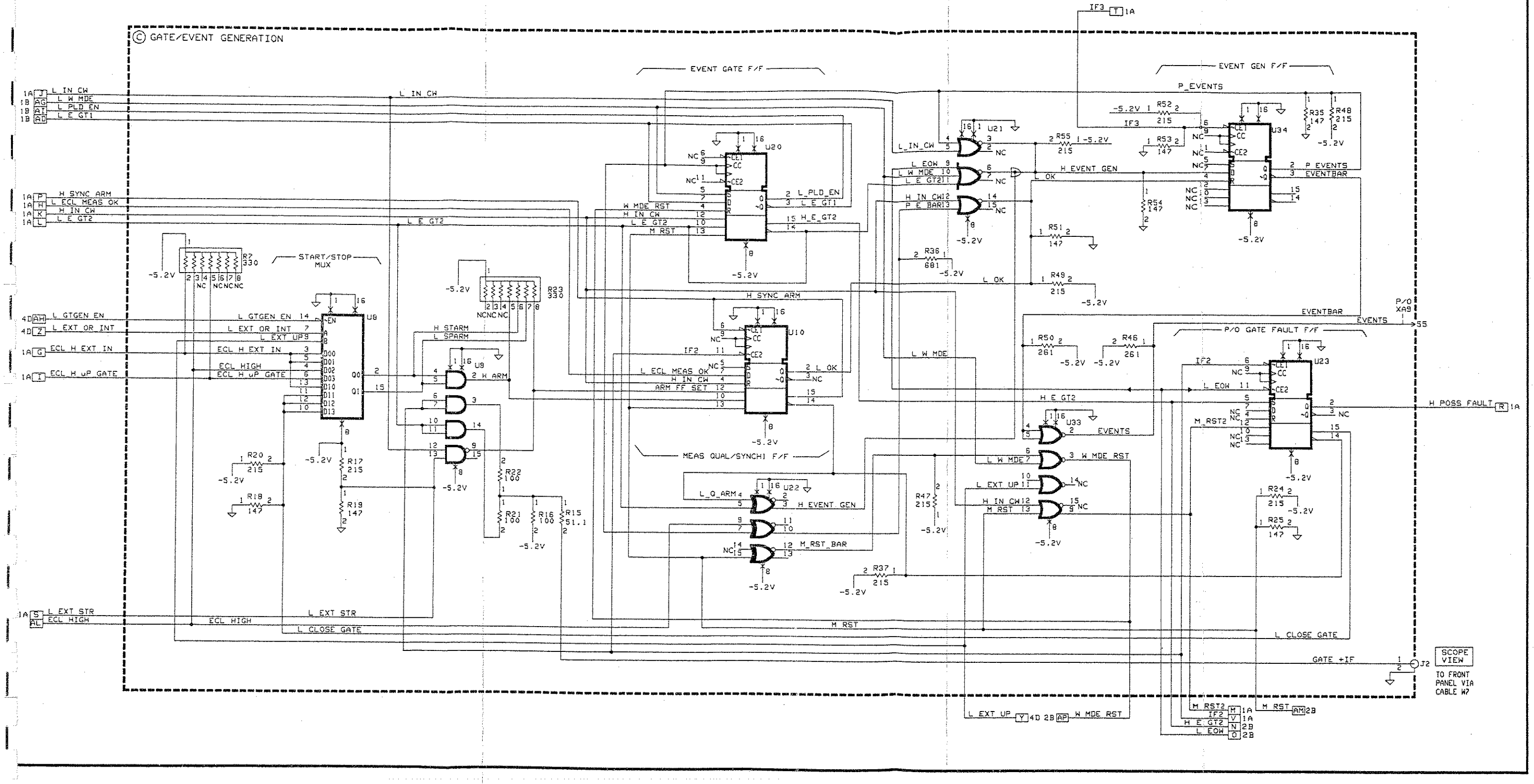
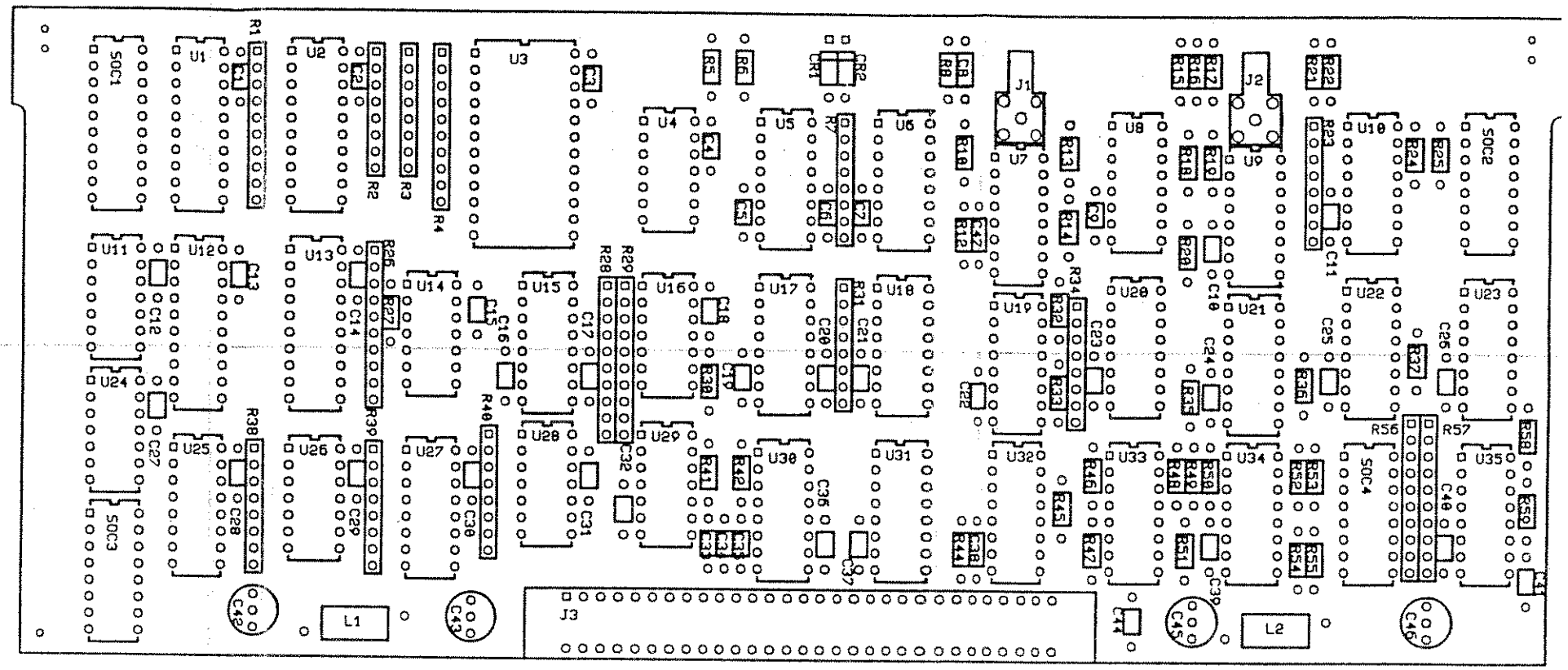


Figure 5-28. A14 Gate Board Assembly Component Locator/Schematic Diagram (Sheet 3 of 4)



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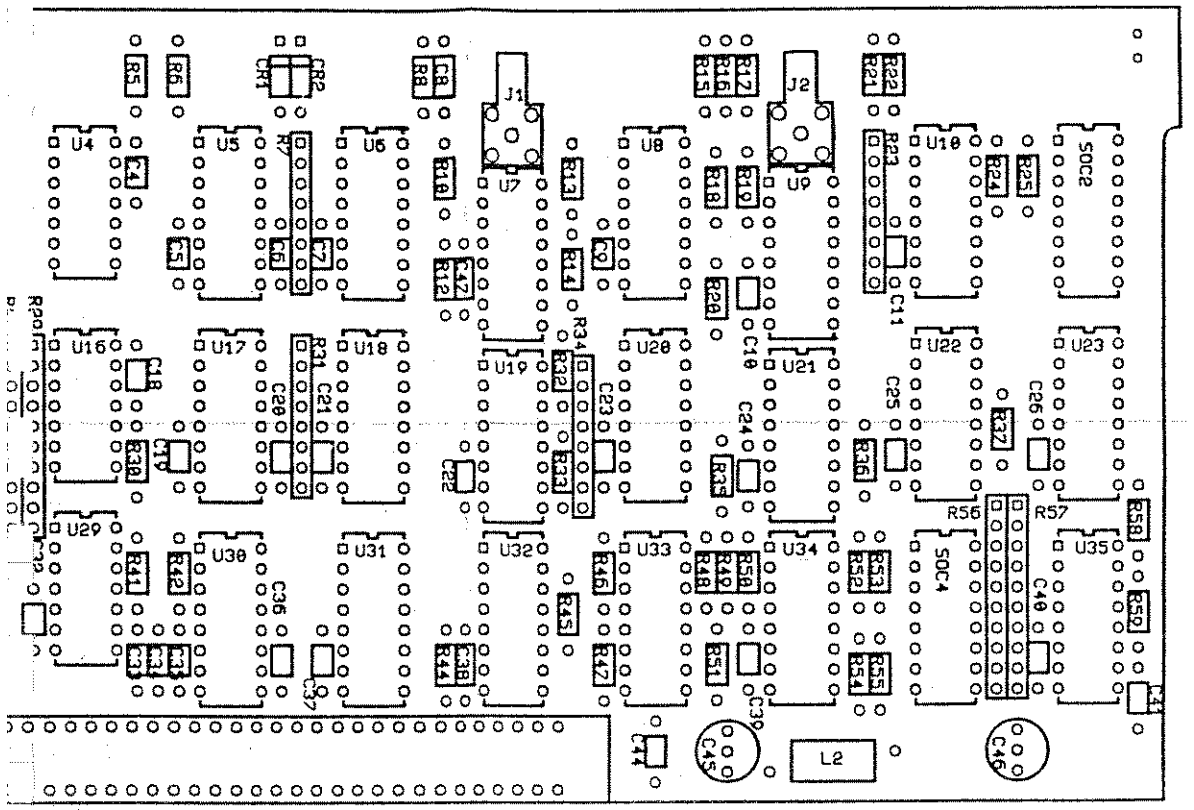
4. A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.



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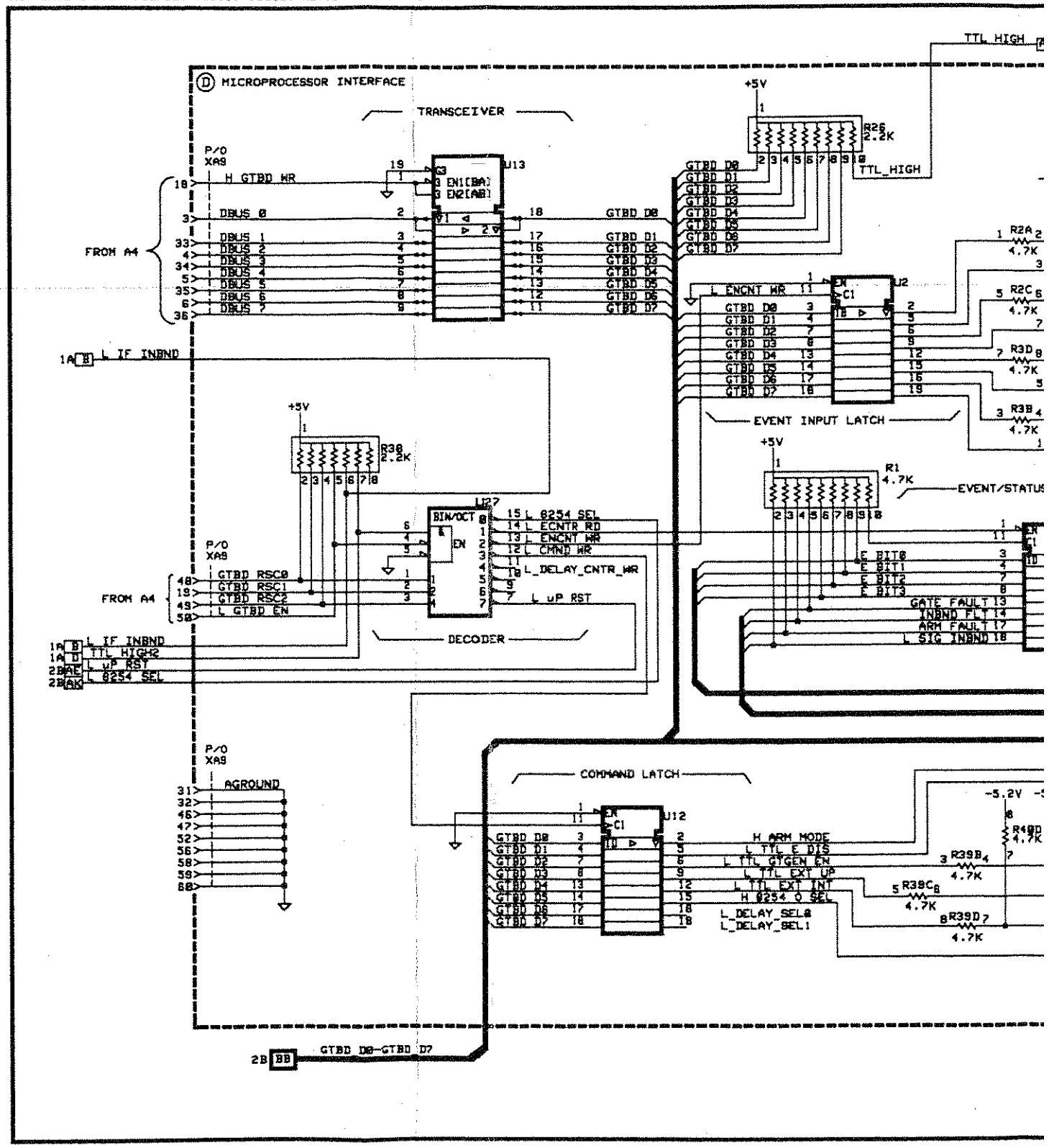
A TILDE ("~") PRECEDING A SIGNAL INDICATES A NEGATIVE-TRUE SIGNAL.

A14 GATE BOARD ASSEMBLY (05361-60009) REV.B (SHEET 4 OF 4)



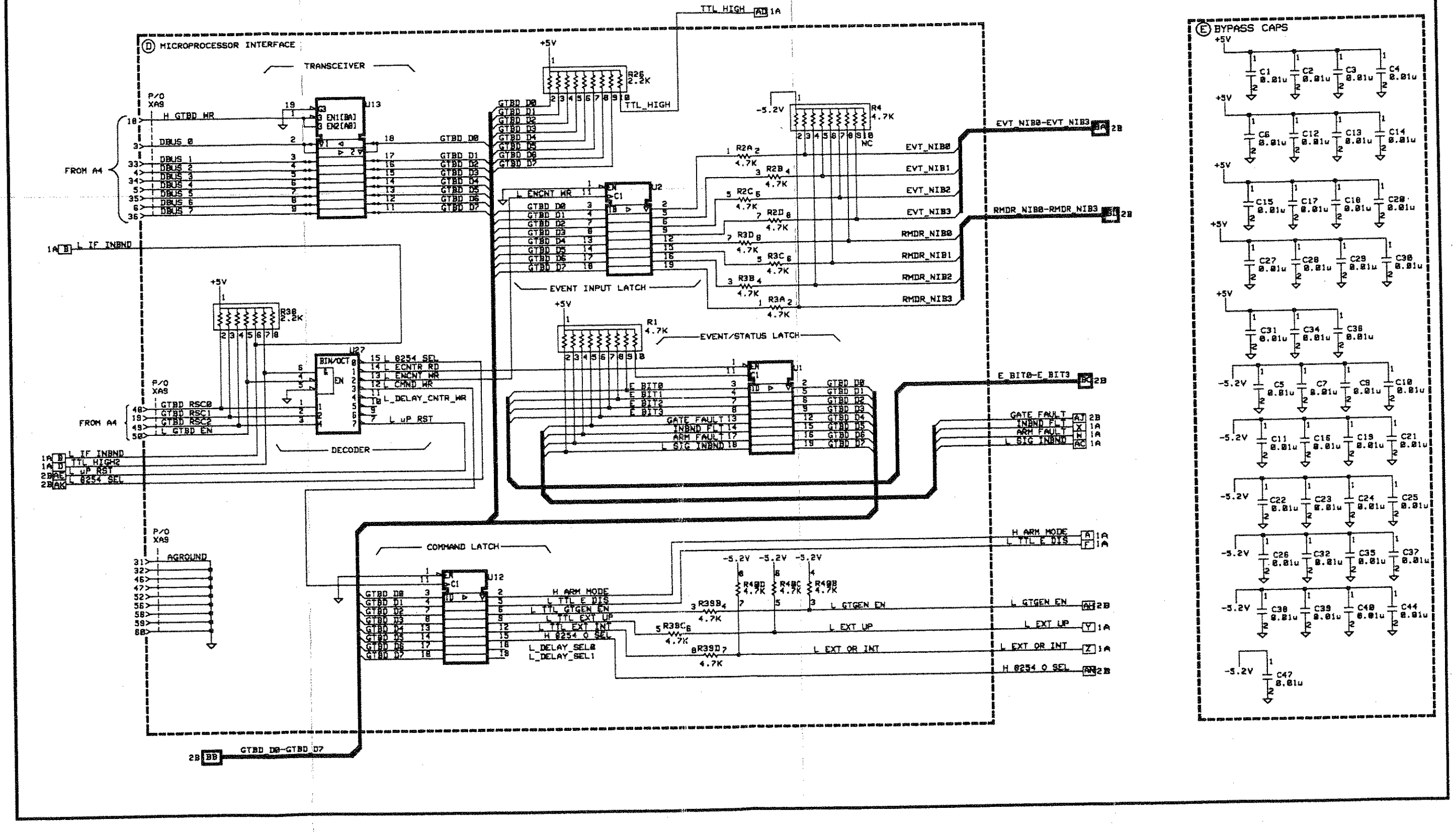


Figure 5-28. A14 Gate Board Assembly Component Locator/Schematic Diagram (Sheet 4 of 4)

APPENDIX

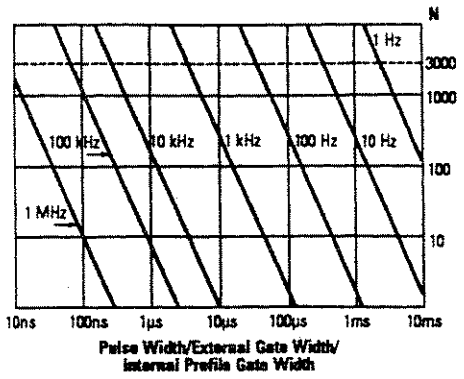
A

SPECIFICATIONS

INTRODUCTION

The Specifications[1] for the HP 5361B are described on the following pages. These specifications are the performance standards or limits against which the instrument can be tested. Perfomance test procedures for testable specifications are described Section 1 (Performance Tests). Some performance parameters are called "typical" or noted as "characteristic(s)". These values have no corresponding performance tests in Section 1. This appendix is oragnized into the following three information groups. (NOTE: Specifications[1] footnotes are on page A-4.)

Table A-1. HP 5361B Specifications



Graph 1 - Resolution; number of pulses (N) vs. pulse width/external gate width/ internal profile gate width. Gating Time = N x (PRI + 0.4 ms).**

Pulse Width	K_1	K_2ms [hi-band, opt.040]
MANUAL ACQ. (< 100 ns)	10	180
100 ns to 250 ns	1200	1700
250 ns to 500ns	250	360 [1700]
500 ns to 1.00 µs	120	360 [1700]
1.0 µs to 5.0 µs	30	360
>5.0 µs	12	360
ASSESS,PULSE/CW		780 - 1300 ms

Table 1 - Pulse Acquisition Time = (J* x K_1) x PRI** + K_2(in ms) + Assess***

* J = 1 unless signal carrier freq. is moving, then J=10.
** PRI minimum = 200 µs for equations.
*** Assess only needs to be added when a change from Pulse/CW is done.

Example: For a PRI of 1 ms, pulse width of 10µs, and a resolution set to 10 kHz, for a standard HP 5361B using automatic acquisition,
Gating Time = (3) x (1 ms + 0.4ms) =4.2ms
Acquisition Time= (1 x 12) x 1 ms + 360 ms = 372 ms;
Measurement Time = 4.2 ms + 372 ms + 200 ms = 576 ms.

INPUT SPECIFICATIONS

	Input 1 (50 Ω)	Input 2 (1 MΩ ll 70 pf)	Input 2 (50 Ω)
Freq Range	500MHz - 20, 26.5, 40 GHz	10 Hz - 80 MHz	10 MHz - 525 MHz
Sensitivity		25 mVrms	25 mVrms
0.5 - 12.4 GHz	-28 dBm		
12.4 - 20 GHz	-23 dBm		
0.5 - 26.5 GHz (opt. 026,040)	-20 dBm		
26.5 - 40 GHz (opt. 040)	dBm = 0.37 x f(in GHz) - 29.8		
Maximum Input	+7 dBm	1 Vrms	+10 dBm
Damage Level	+25 dBm	dc - 5 kHz: 250 V(dc + peak ac) >5 kHz: 5.5 Vrms + 1.25 10^{-6} Vrms/(Freq)	
Connector (Std.) (opt. 026, 040)	Type N, female 2.92 mm, male, compatible with APC 3.5 and Type A	BNC, female (with replaceable fuse).	
SWR (Typical):			
0.5 - 10 GHz	<2:1	NA	NA
10 - 20 GHz	<3:1		
20 - 26.5 GHz (opt. 026, 040)	<3:1		
26.5 - 40 GHz (opt. 040)	<3.5:1		

FREQUENCY (INPUT 1)

Automatic Acquisition:
500 MHz - 20 GHz;
500 MHz - 26.5 GHz (opt. 026, 040);
12 GHz - 40 GHz (opt. 040, high-band);
for CW and pulses > 100 ns.

Manual Acquisition:
500 MHz - 1 GHz, entered value = Input signal ± 3 MHz
1 GHz - 30 GHz, entered value = Input signal ± 20 MHz;
30 GHz - 40 GHz, entered value = Input signal ± 10 MHz;
for pulses < 100 ns, entered value = Input signal ± 3 MHz.

Least Significant Digit:
1 MHz to 1 Hz for frequency, 0.001 Hz for PRF.

Residual Stability:
1 LSD rms typical for 1 Hz resolution at 25°C, when counter and source use common 10 MHz time base or counter uses external high stability time base.

Pulse Frequency Measurements

Pulse Width (Minimum):
60 ns (< 100 ns mode, manual Acq.)[3];
100 ns (Auto Acq.).

Pulse Rep Freq:
Min (low PRF mode)- 1 Hz (0 to 30°C).
Min/Max (Default)- 50 Hz/2 MHz.

On/Off Ratio (Typical): ≥15 dB.

Maximum Video (Typical):
≥ (Signal level + 20 dB).

FM Chirp Tolerance[2]:
Manual Acq.- 50 MHz p-p (when entered value = center frequency ±1MHz).
Auto Acq.- 10 MHz p-p.

Rise/Fall time (Typical, to remain in Pulse Mode): ≤ 20 µs.

Measurement Time (Typical)[5]: Gating time + Acq. time + 200 ms (graph 1, table 1).

Resolution[4]: 1 Hz - 1 MHz (graph 2).

Accuracy[4]: Time base uncertainty (graph 4) + Gate Error (graph 3).

Table A-1. HP 5361B Specifications (Continued)

CW Frequency Measurements

AM Tolerance (Typical): ≤ 40% to 5 kHz; ≤16%, above 5 kHz.

FM Deviation (Typical, See Graph 5)[6]:
Manual Acq. (when entered value = center frequency ±1MHz) - 60 MHz p-p; 55 MHz p-p (opt. 040).
Automatic Acq.- 20 MHz p-p; 12 MHz p-p (opt. 040).

FM Rate (Maximum)[6]: 10 MHz.

Tracking Speed[7]:
Fast Acquisition Track- 800 MHz/s.
Normal FM Rate- 1 MHz/s.
Low FM Rate- 80 kHz/s.

Acquisition Time (Manual Acq.): <40 ms.

Acquisition Time (Automatic Acq.)[6]:
Fast Acquisition Track- <100 ms.
Normal FM Rate- <170 ms.
Low FM Rate- <1.3 seconds.

Gate Times (1 Hz Resolution):

500 MHz - 5.7 GHz	200 ms
5.7 GHz - 11.3 GHz	400 ms
11.3 GHz - 16.9 GHz	600 ms
16.9 GHz - 22.5 GHz	800 ms
>22.5 GHz	1000 ms

Measurement Time (Typical)[5]: Gate Time + Acquisition Time + 100 ms.

Resolution: 1 Hz - 1 MHz, selectable.

Accuracy: ±1 LSDrms ± time base uncertainty (graph 4).

PROFILE (INPUT 1)

Frequency Range (Min/Max for Y axis, see FM chirp tolerance for span):
500 MHz/20 GHz.
500 MHz/26.5 GHz (opt. 026).
500 MHz/40 GHz (opt. 040).

FM Chirp Tolerance[2] (Max span for Y axis):
Manual Acq.: 50 MHz p-p (when entered value = ±1 MHz of center frequency).
Auto Acq.: 10 MHz p-p.

Time Range (Min/Max span for X axis):
100 ns/10 ms.

Time Resolution: 1 ns.

Internal Gate Width:
Minimum: 11 to 23 ns.
Typical minimum: 14 ns.
Maximum: 10 ms.

External Gate Width (Minimum):
Manual Acq.: 20 ns.
Auto Acq.: 60 ns.

Gating/Arming:
Pulse- Internal, external arming, external gating.
CW- External gating.

Number of Data Points:
Auto Profile: up to 75.
Manual Profile: 1 to 99.

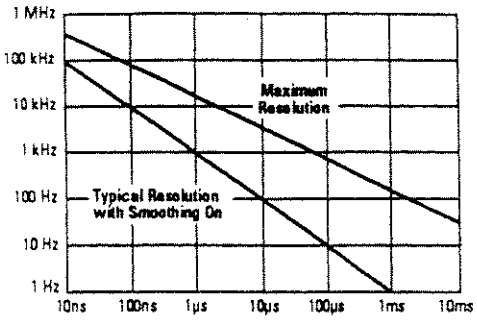
Profile Frequency Measurements

Frequency Resolution:
Selectable, 1 Hz to 1 MHz, dependent on internal profile gate width (graph 2).

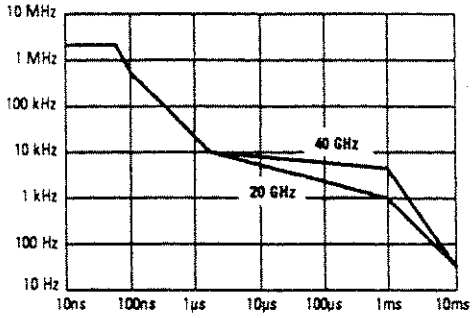
Printers Supported: ThinkJet (HP 2225A), QuietJet Plus (HP 2227B), PaintJet (HP 3630A, opt. 002).

Profile Phase Measurements

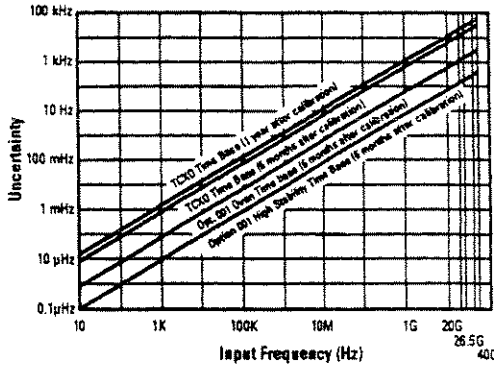
See Application Note 377-4 for details.
Computer required.



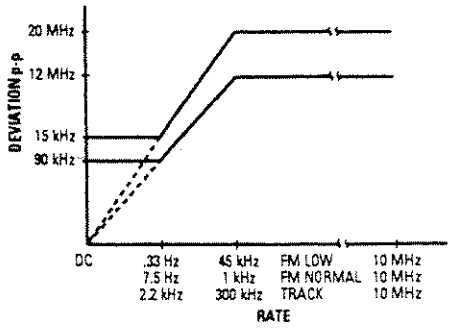
Graph 2 - Maximum resolution as a function of pulse width/external gate width/internal profile gate width.



Graph 3 - Maximum gate error as a function of pulse width/external gate width/internal profile gate width.



Graph 4 - Time base uncertainty.



Graph 5 - FM rate vs. deviation rate.

Pulse Parameters (INPUT 1): *Measurements approx. 6 dB below signal peak.*

	Pulse Width	*PRI*	*Offtime*	*PRF*
Min/Max	60 ns/10 ms	500 ns/1 s	400 ns/1 s	1 Hz/2 MHz
LSD	(PW <1 ms)- 1 ns; (PW ≥1ms)- 100 ns			to 0.001 Hz
Accuracy* (100 ave.)	± (20 ns + timebase error x Measurement) ± LSD			± (20 ns) x (PRF)^2 ± LSD ± Timebase uncertainty

* for rise/fall times ≤ 20 ns.

Table A-1. HP 5361B Specifications (Continued)

FREQUENCY (INPUT 2)

Frequency Range: 10 Hz to 525 MHz.

Mode of Operation:
50 Ω: 10 MHz to 525 MHz.
1 MΩ: 10 Hz to 80 MHz.

Sensitivity:
Full Operating Environment:
50 Ω: 10 MHz to 525MHz, 25 mVrms.
1MΩ: 10 MHz to 80 MHz, 25 mVrms.
@ 25°C (typical):
50 Ω: 10 MHz to 525 MHz, 15 mVrms.
1 MΩ: 10 Hz to 80 MHz, 15 mVrms.

Gate Time: 1/Resolution, 1ms minimum.

Resolution: selectable 1 Hz to 1 MHz.

High Resolution: 1 MΩ mode: 0.001 Hz for < 100 kHz input; 0.01 Hz for < 1 MHz input; 0.1 Hz for < 10 MHz; 1 Hz for > 10 MHz input; 1 second gate.

Accuracy: ± 1 LSD ± $\left(\frac{\text{Trigger Error}^{8} \times \text{freq.}}{0.7 \times \text{Gate Time}} \right)$ ± Time Base Uncertainty

(See Graph 3)

Impedance (nominal):
Selectable - 1 MΩ ll 70 pf, or 50Ω.

Coupling: ac.

Connector: BNC with replaceable fuse.

Maximum Input: (50 Ω) - +10 dBm; (1 MΩ) - 1 Vrms.

Damage Level: 50 Ω or 10 MΩ.
dc to 5 kHz: 250 V (dc + ac peak);
>5 kHz: 5.5 Vrms (+ 28 dBm) +1.25 X 10^{6}

TCXO TIME BASE

Crystal Frequency: 10 MHz.

Stability:
Aging Rate- <1 x 10^{-7} per month.
Short Term- <1 X 10^{-9} for one second averaging time.

Temperature: <1 X 10^{-6}, 0 - 50° C set to offset frequency at + 25° C.

Line Variation: <1 X 10^{-7} for 10% change from nominal.

Notes:

1 Specifications herein describe the instrument's warranted performance. Typical or nominal measurement characteristics are intended to provide information useful in applying the instrument, but are non-warranted performance parameters.

2 For carriers from 1 GHz to 40 GHz and chirp mode on.

3 For carriers from 1 GHz to 40 GHz.

4 Resolution is the standard deviation of the measurement error, and accuracy is the mean. This can be approximated as Gaussian.

5 AGC setting time is 0.3 to 2.5 seconds (or 3 minutes for Low PRF mode). If signal amplitude is not steady state, this must be added to the measurement time.

6 Valid for Extended Function 92 (forced CW Mode). For carriers from 1 GHz to 40 GHz.

7 These tracking speeds ensure that an incorrect answer will not be displayed. The HP 5361B will display the correct answer or no answer. Valid for Extended Function 92 (Forced CW mode).

8 Trigger Error: $\frac{\sqrt{e_i^2 + e_n^2}}{\text{Input Slew Rate in V/s at Trigger point}}$

Where e_i = Effective rms noise of counter's input channel (100 µV typical).
e_n = rms noise of the input signal for a 500 MHz bandwidth.

Table A-1. HP 5361B Specifications (Continued)

Characteristics*

GENERAL

Display: 24 character alpha-numeric LCD.

Keyboard Setup: Setup stored by STBY mode.

Self-Check: Performs internal checks and gate bias calibration.

Calibrate: Calibrates gate error at power up and when self check/cal is requested.

Lockout: Display and Keyboard, see manual.

Data Output: HP-IB to HP 350, with Ext. Function 92 and "Dump Mode"; varies with freq., resolution, and Mode.
CW- (10 kHz resolution).
Automatic Mode: 100 readings/s.
Manual Mode: 120 readings/s.
Pulse- (10 kHz res., 5 kHz PRF, and 10 ms PW).
Automatic Mode: 4 readings/s.
Manual Mode: 10 readings/s.

Sample Rate: Variable from less than 50 msec to infinite (HOLD).

Display Rate: 5/s for 1 kHz resolution, CW.

Low Emission Mode: Input 1 emissions reduced to < -70 dBm typical when sleep mode or input 2 is selected.

HP-IB: Functions and Extended Functions are programmable. Address settable from front panel. Teach/Learn programming IEEE 728 compatible command structure.

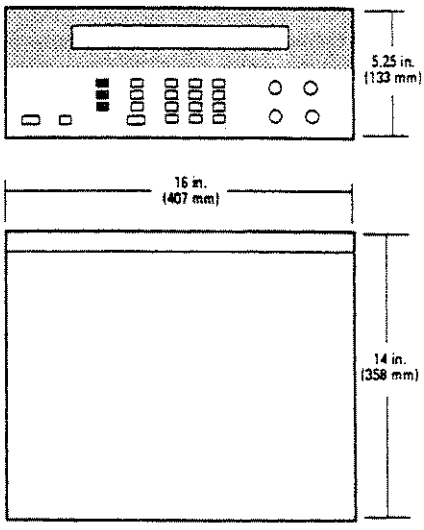
Operating Temperature: 0° C to 50° C.

Power Requirements: 100 VA Max.
Line select-
100 V (90 - 105 VAC; 47.5 - 440 Hz);
115/120 V (104-126 VAC; 47.5 - 440Hz);
220 V (198 - 231 VAC; 47.5 - 66 Hz);
230/240 V (207-252 VAC; 47.5 - 66 Hz).

Extended Functions: Set sampler LO frequency; set gate width in time; force pulse or CW mode; <100 ns pulse width mode; high resolution mode; set gate width in IF periods; and 11 settable profile parameters.

Size: 133mm H x 407 mm W x 358mm D; 5.25 in. H x 16 in. W x 14 in. D.

Weight: 11 kg (24 lbs).



Gate Modes (Input 1):
Internal Gate- Automatically gate on either CW or pulsed signals.
External Gate- A low TTL signal on the Gate/Arm Input determines when a frequency measurement is made.
External Arm- A high to low TTL edge enables a measurement on the next pulse. The edge must occur 50 ns (typical) prior to the pulse to be measured. The edge must also occur during the pulse offtime.

Math Functions: Result = (Measurement x scale) + offset.

Offset- Measurement is offset by entered value.

Scale- Measurement is multiplied by entered value.

Smooth (Input 1)- Displayed resolution is determined using exponential averaging; displays only stable digits, and increases resolution.

Level Indicator: "LEVEL", indicates AGC is leveling, check that input range is not exceeded.

IF Output: Rear panel BNC provides 30 to 110 MHz down-converted microwave signal at ~ -13 dBm into 50 Ω, ac coupled.

Scope-view: Digital version of the IF + internal gate. The pulse is represented as the IF of the down-converted pulse (nominally 300 mv p-p) with an average value of -0.8 volts. The gated portion of the signal is offset to an average value of -1.2 volts, illustrating the measurement interval.

Pulse Output: 1 to 0 volts into 50 Ω. Delay from detected pulse 15 nsec, nominal.

Ext. Gate/Arm Input: Input requires a TTL active low edge (armed) or level (gate). Input impedance is 1.5 k Ω ll 30 pf, connected to 3.3 Volts. Delay from external gate/arm edge to measurement 15 nsec.

Time Base Output: 10 MHz and 1 MHz, >2.4 V square wave ac coupled into 1 k Ω or >1.5 Vp-p into 50 Ω. Available at rear panel BNC connectors whenever the instrument has ac power connected.

External Time Base: 1, 2, 5, 10 MHz, 0.7 volts minimum to 8 V maximum p-p sine wave or square wave into >1 k Ω shunted by <30 pf. The external reference is automatically selected when a signal is present and an indicator (▼) appears in the display. TCXO power is turned off, oven heater on, oscillator signal disconnected.

* Characteristics are intended to provide information useful in applying the instrument by giving TYPICAL but nonwarranted performance parameters.

Table A-1. HP 5361B Specifications (Continued)

OPTIONAL OVEN TIME BASE, OPTION 001

Crystal Frequency: 10 MHz.

Stability:

Aging Rate- <5 x 10^{-10} per day after 24 hr warm up when off-time is < 24 hrs and aging rate is < 5 x 10^{-10} per day prior to turn off. < 5 x 10^{-10} per day in < 30 days of continuous operation for off-time >24 hrs. <1 x 10^{-7} per year for continuous operation.

Short Term- <1 x 10^{-10} for 1 second averaging time.

Temperature: <7 x 10^{-9}, 0 - 50° C.

Line Variation: <1 x 10^{-10} for 10% change from nominal.

Warm Up: <5 x 10^{-9} of final value 10 minutes after turn-on at 25° C when off-time is <24 hours and the aging rate is <5 x 10^{-10} per day prior to turn off.*

OPTIONAL INCREASED DAMAGE LEVEL, OPTION 006

Protects input 1 from damage by limiting high level signals. All specifications are the same except Input 1.

Damage Level (Pulsed):

+50 dBm (100 Watts) peak, pulse width ≤1 μs 0.001 duty cycle, typical.

Damage Level (CW):

500 MHz to 6 GHz- +39 dBm (8Watts);
6 GHz to 18 GHz- +36 dBm (4 Watts);
18 GHz to 26.5 GHz- +34.8 dBm (3 Watts).

Sensitivity (Insertion Loss): 3 dB, 500 MHz to 12.4 GHz; 4 dB, 12.4 GHz to 20 GHz ; 5 dB, 20 GHz to 26.5 GHz .

SWR: (500 MHz to 10 GHz) <2.5:1 typical; (10 GHz to 26.5 GHz) <3.5:1 typical.

OPTIONAL OVEN TIME BASE, OPTION 010

Crystal Frequency: 10 MHz.

Stability:

Aging Rate- <7 x 10^{-10} per week after 24 hr warm up when off-time is < 24 hrs and aging rate is <7 x 10^{-10} per week prior to turn off. <7 x 10^{-10} per week in <30 days of continuous operation when off-time >24 hrs. <2 x 10^{-8} per year for continuous operation.

Short Term- <1 x 10^{-10} for 1 second averaging time.

Temperature: <7 x 10^{-9}, 0 - 50° C.

Line Variation: <1 x 10^{-10} for 10% change from nominal.

Warm Up: <5 x 10^{-9} of final value 10 minutes after turn-on at 25° C when off-time is <24 hours and the aging rate is <7 x 10^{-10} per week prior to turn off.*

OPTIONAL FREQUENCY EXTENSION, OPTION 026

Frequency Range (input 1):
500 MHz - 26.5 GHz .

OPTIONAL FREQUENCY EXTENSION, OPTION 040

Frequency Range (Input 1):
500 MHz - 40 GHz .

Note: Options 006 and 700 are incompatible with Option 040.

OPTIONAL MATE PROGRAMMING CAPABILITY, OPTION 700

Built-in CIIL operating codes:
CIIL Operating Codes: FNC, SET, SRX, SRN, INX, FTH, CLS, OPN, RST, CNF, IST, STA, GAL.

MATE Interface Standard:
2806763 Rev. B.

Note: Option 040 and the profile function are incompatible with option 700.

* Final value is the frequency after 24 hours of continuous operation. An indicator (▼) appears in the display until the oven is at operating temperature.

APPENDIX

B

RECOMMENDED TEST EQUIPMENT

INTRODUCTION

The test equipment listed in *Table B-1* is recommended for use during performance tests, adjustments, and troubleshooting. Substitute test equipment may be used if it meets the critical specifications listed in the table.

Table B-1. Recommended Test Equipment

INSTRUMENT	REQUIRED CHARACTERISTICS	USE*	RECOMMENDED MODEL
Oscilloscope	275 MHz bandwidth, delayed sweep	T,A,P	HP 54201A or equivalent
Oscilloscope probe	High impedance (10:1), minimal capacitance (8-10pf)	T,A	HP 10433A or equivalent
Active probe	≥350 MHz 100:1 divide capability	T	HP 1124A or equivalent
High Impedance Oscilloscope probe	10MΩ or greater	T	HP 10432A or equivalent
Storage Oscilloscope	100 MHz bandwidth storage capability	T	HP 54201A or equivalent
Sweep Oscillator	.01-20 GHz FM modulation - 20 MHz	P	HP 8620C mainframe/ HP 86222A/B plug-in or equivalent
Synthesized Signal Generator	10 MHz to 2.5 GHz	T,A	HP 8660D mainframe/ HP 86603A plug-in
Synthesized Sweeper	10 MHz to 26.5 GHz	A,P	HP 8340B or equivalent
Synthesizer	10 Hz to 10 MHz	OV,P	HP 3325B or equivalent
Spectrum Analyzer	RF inputs from 1 MHz to 500 MHz	T,P,A	HP 8566B or equivalent
Digital Voltmeter	4½ digit	T,A	HP 3466A
Power Sensor	50 MHz to 20 GHz	A,OV,P	HP 8485A
Power Meter	50 MHz to 20 GHz	A,OV,P	HP 436A
Power Splitter	DC to 26.5 GHz	OV,P	HP 11667B
50 Ω Feedthrough	BNC male to BNC female	OV,P	HP 10100C
Fixed Attenuator	10 dB ±1dB	P	HP 8493C
Fixed Attenuator	20 dB Attenuation	A	HP 8491A Option 20
Pulse Generator	1 to 20 μs pulse width 1 to 20 μs PRI	OV,P	HP 8012B or equivalent
Time Synthesizer	1 to 20 μs pulse width 1 to 20 μs PRI	OV,P	HP 5359A or equivalent
Instrument Controller	BASIC 5.0 Control Language, HP-IB Interface Capability	OV	HP 9000 Series 300 (or equivalent)

* T = Troubleshooting OV = Operation Verification

A = Adjustments P = Full Performance Testing

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